Design and FPGA Implementation of a Low Power OFDM Transmitter for Narrow-Band IoT

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Abstract

5G technology is now globally widespread. One of the most interesting applications that this technology offers concerns the "Internet of Things", better known as IoT which gave birth to several new technologies such as the Narrow-Band IoT (NB-IoT). These technologies provide a communication standard for wide areas and its main feature is low power consumption. In this paper the design and the FPGA implementation of a low-power OFDM transmitter for NB-IoT applications is proposed. It is mainly composed of a QPSK Mapper, a 12-points IFFT and a Cyclic Prefix Module. The whole developed system has been implemented on a Xilinx Spartan-7 device and it has been characterized in terms of hardware resources, timing, and power consumption.

Keywords

5G, FPGA, OFDM, NB-IoT

1. Introduction

In these last decades, IoT is expanding into various fields allowing the creation of intelligent environments such as smart cities and smart buildings as well as autonomous vehicles [1]. This is made possible thanks to the birth of the fifth-generation technology of mobile telephony also known as 5G which has the target to obtain greater efficiency and versatility through better improved mobile device management skills, higher speed, lower latency between sent signal and available output [2, 3]. The 5G technology gives the possibility to connect a massive amount of devices [4] and having, as consequence, a huge amount of data to manage. For this purpose several communication architectures have been proposed in the literature [5]. Nevertheless, the problem of big-data generated by IoT devices, is often faced with the help of several algorithms of Artificial Intelligence (AI). Usually, for the development of intelligent environments [6, 7, 8] the IoT uses low-speed data transmission services defined LPWAN (Low-Power Wide-Area Network). The NB-IoT is an LPWAN technology proposed by 3GPP, the international standards organization [9]. The NB-IoT supports massive device connections guaranteeing ultra-low power consumption, wide area coverage and bidirectional triggering between signaling plane and data plane. The main features of this technology [10] are shown in Fig. 1 and discussed below.

Layout	Technical feature		
Physical layer	Uplink	BPSK or QPSK modulation	
		SC-FDMA	Single carrier, the subcarrier interval is 3.75 kHz and 15 kHz The transmission rate is 160 kbit/s - 200 kbit/s
			Multi carrier, the subcarrier interval is 15 kHz The transmission rate is 160 kbit/s - 250 kbit/s
	Downlink	QPSK modulation	
		OFDMA, the subcarrier interval is 15 kHz, the transmission rate is 160 kbit/s - 250 kbit/s	
Upper layer	LTE based protocol		
Core network	LTE based protocol		
BPSK: Binary phase shift keying	NB-IoT: Narrow-band internet of things		QPSK: Quadrature phase shift keying
LTE: Long-term evolution	OFDMA: Orthogonal frequency division multiple access		SC-FDMA: Single carrier frequency division multiple access

Figure 1: Main transmission features of NB-IoT.

The bandwidth of the physical layer is 180 kHz. In the down-link, it adopts Orthogonal Frequency-Division Multiplexing (OFDM) with Quadrature Phase-Shift Keying (QPSK) sub-carriers. Modem BPSK or QPSK are adopted with sub-carrier interval of 15 kHz or 3.75 kHz. To have the bandwidth of 180 kHz 12 sub-carriers are defined spaced by 15 kHz and 48 sub-carriers must be used when they are spaced by 3.75 kHz. In this paper the 12 sub-

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carriers transmission will be debated [11]. The aim of our work is the FPGA implementation of a low-power/low-area OFDM modulator for NB-IoT. Since the critical part of the transmitter is the 12-points IFFT, starting from an algorithm proposed in [12], we developed an architecture efficient in terms of power and area. OFDM numeric modulation is widely used for ADSL, DVB-T, WiFi, WiMAX transmission, and in 802.11a, 802.11n 802.11ac standards. Behind this modulation there is the use a series of orthogonal sub-carriers with different frequencies, each one carrying a part of the information. Each sub-carrier is modulated with the common BPSK or QPSK modulation. For NB-IoT OFDM, the symbol time is fixed to $T_{sy} = 66.7\mu s$. The sampling is carried out with a period of $T_{sampling} = \frac{1}{Bandwidth} = 5.5\mu s$. Two important issues in OFDM modulation are the Inter-Carrier Interference (ICI) [13] and the Inter-Symbol Interference (ISI) [14]. To overcome these problems, techniques for adding redundancy symbols such as the *Cyclic Prefix* (CP) are used [15]. The CP used in OFDM modems for NB-IoT is the "normal" cyclic prefix used for LTE transmissions. In this case, the bandwidth is so short then the CP is made of few samples since there will be a low inter-carrier interference. For LTE technologies the CP has a duration of $5.5\mu s$ which is exactly the sample time, this means it is sufficient to add only a single sample of each OFDM symbol.

2. OFDM modem with a 12-points IFFT

2.1. IFFT Butterfly Diagram

One of the characteristics that allowed OFDM modulation to develop and spread for most of the transmissions is the efficiency in its digital implementation. The output modulation is proportional to the IFFT (Inverse Fast Fourier Transform) of the input components. The structure of an IFFT-based OFDM transmitter modulator is formed of the succession of a Mapper, a block that performs the IFFT followed by one that adds the cyclic prefix [16]. The most popular FFT algorithm is the Cooley-Tukey algorithm which is based on the *Divide et impera* principle and which recursively breaks a DFT of any size N into smaller DFTs [17]. Usually this is done on samples of length equal to a power of 2 and therefore with $N = 2^m$. As discussed in the introduction, the NB-IoT requires an OFDM modulation with 12 sub-carriers. For this reason, it is required an $N = 12$ points IFFT. Since $N = 12$ N is not a power of 2, the traditional Cooley-Turkey algorithm cannot be used. To solve this issue in [12] the authors propose an architecture that uses a combination of two algorithm: the Cooley-Turkey and the Split Radix Algorithm for length 6^m IFFT realizing a custom butterfly diagram as a sequence of radix2, 4 and 3 IFFT from which the subsequent architecture will be derived (see Fig. 2)[18].

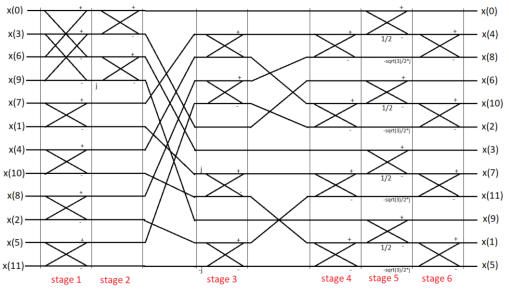

Figure 2: Butterfly diagram for the realization of a 12-point FFT complete with operations to be carried out, multiplicative coefficients and explaining all the stages.

2.2. IFFT Stage Structure

The parallel 12-points architecture shown in Fig.2 is not necessary the best choice for a NB-IoT OFDM modulator. This is due to the slow data rate of the standard,and, as consequence, there is not any necessity of parallel IFFT implementation. Parallel implementations are very useful in case of fast data rate, vice versa, in case of slow data-rate, serial architectures are preferred in order to reduce hardware resources. Let's consider that all the more IoT devices as sensor nodes acquire data serially from ADC. For this reason, starting from the architecture shown in Fig. 2 we develop a serial IFFT. Serialization has been obtained by inserting dual port RAMs between each IFFT/FFT stage. These dual port RAMs have been used to implement the double buffering (ping-pong) operation on data coming from the previous stage. According to the NB-IoT standard, the transmitter was realized by inserting a QPSK modulator at the input of the IFFT. At the output of the IFFT, another dual-port RAM implementing the double buffering technique has been inserted, to realize the cyclic prefix required by the standard. The block diagram of the proposed architecture is shown in Fig. 4. It is interesting to focus on the realization of the individual stages of the IFFT. Being a series of 2, 4 and 3-points IFFTs, each stage will have to be custom-made following a basic architecture shown in Fig. 3 [19].
Each stage consists of a dual-port RAM in which the samples are saved and at the same time two samples are read and used for the elaboration. The simultaneous reading and writing are carried out through the double buffering technique and the reading and writing addresses are saved inside a ROM. The read data are used to perform complex multiplication with the IFFT twiddle factors stored in a ROM. Finally, the samples enter an adder and

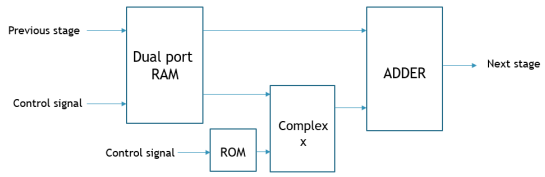

Figure 3: Base structure of a single IFFT 12pt. stage.

are serialized with a multiplexer to be saved in the next ROM. Outside this scheme, there are the control signals generated by an FSM.

3. Experimental Results

The proposed architecture shown in Fig.4 has been simulated in SIMULINK. The Fixed point analysis has been performed to size all the algebraic elements of the system (multipliers, adders, etc.). We sized the entire system to assure a certain MER (Modulation Error Ratio). In fact, the quantization error due to the truncation of algebraic operators implies an enlargement of the QPSK constellations points, this effect can be treated as MER degradation. The MER is the measure of the signal-to-noise ratio (SNR) in digital modulation applications. We targeted our system in order to have a quantization noise that introduces a MER degradation not more that 20dB. Fixed-point simulation results show that 8 bit for any multiplier and adder is sufficient to obtain the MER of 20 dB as depicted in (Fig. 5).
Considering this reduced number of bits required for the multiplications and considered that all products are performed with constant values (the IFFT twiddle factors), it is possible to avoid the use of FPGA internal DSP blocks by implementing multiplications with shift and additions. Thank to this optimization, power consumption is reduced and DSP blocks are not wasted. This latter aspect is very important because it allows preserving DSP block for other application as for example Machine-Learning and other and in general, applications demanding high-performance computing [20],[21],[22],[23],[24],[25] that, nowadays, is always more used in IoT nodes and it requires a great number of multiplications.

In this paper, we present the results obtained on the Spartan-7 xc7s6cpga196-2 FPGA that is one of the cheapest Xilinx device and, consequently, one of the most interesting for the realization of low-cost IoT nodes. The transmitter has been characterized in terms of resources utilization and power consumption that are crucial aspect for IoT nodes [26]. Power analysis has been performed initially without any Switching Activity Interchange Format File (SAIF) in order to have a coarse power consumption estimation on all the FPGAs involved in our experiments. In a second step, we perform a more accurate power consumption estimation on the xc7s6cpga196 using the SAIF files containing information about the switching activity. The system has been tested by generating at its input random 2 bit symbols. In Tab.1 and Tab.2 implementation results are shown. Such results refer to the implementation with a a timing constraints of $5.5\mu s$ that is the minimum value to respect the NB-IOT specifications.

Table 1
simulation Results

FPGA	Spartan-7 xc7s6cpga196-2
Clock period	$5.5[us]$
Frequency	$180[kHz]$
Total Power on chip	$0.018[W]$
Energy per symbol	$1.287 * 10^{-}6[J]$

Table 2
Utilization

Utilization			
Resource	***Utilization***	***Avaible***	***% Utilization***
LUT	1050	3750	28.00
LUTRAM	259	2400	10.79
FF	648	7500	8.64
IO	23	100	23.0
BUFG	1	16	6.25

In Fig.6 is shown the hierarchical power report providing dynamic power consumption information for each stage of the proposed OFDM modulator, results are shown in percentage considering the total dynamic power dissipated as 100%. The third IFFT stage is the one characterized by greater dynamic power consumption. This is an expected result as it is the stage that contains the greatest number of multiplications and consequently it is the most complex in terms of area.

3.1. Power and Energy Trend in Frequency

Because power consumption represents one of the most important aspects of IoT Nodes, the proposed OFDM transmitter has been characterized in terms of energy. Several implementations using different clock constraints have been realized. In this way, it has been possible to characterize the energy consumption for every implementation. Energy consumption has been estimated in terms of energy per OFDM symbol according to Eq 1,

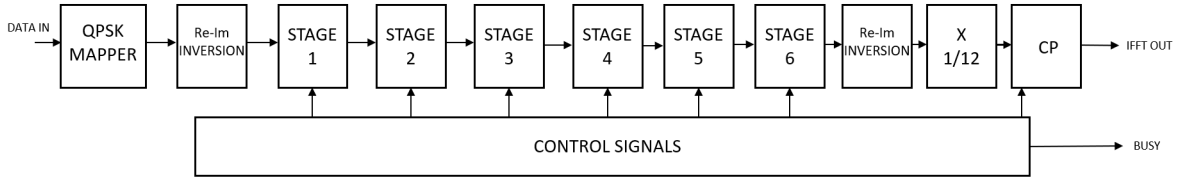

Figure 4: The proposed NB-IoT OFDM modulator.

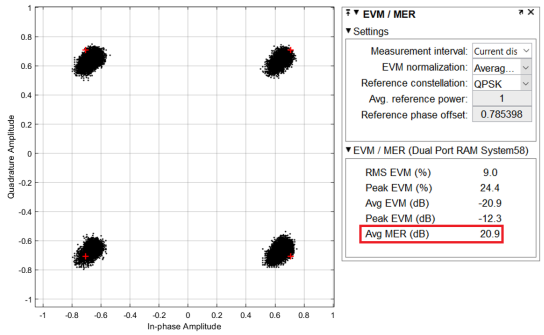

Figure 5: Obtained MER with 8-bit fixed point simulation.

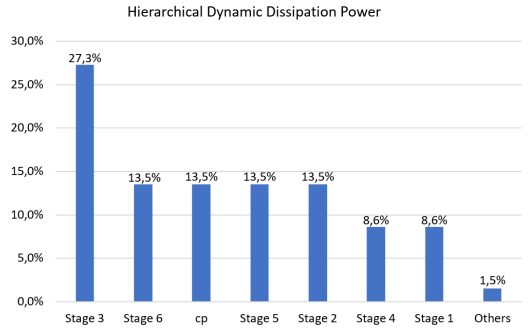

Figure 6: Hierarchical Dynamic Dissipation Power.

$$E_{sym} = P_{ave} * N * Tc \quad (1)$$

where P_{ave} is the power estimated through post-implementation simulations taking into account the real switching activities of nodes contained in the SAIF files provided to the power estimator, N is the number of clock cycles required to obtain an OFDM symbol that in our case is 13 (12 for the IFFT computation and 1 for the cyclic prefix) and finally Tc is the Clock period. The frequency range was chosen to start from the maximum frequency that allows the correct operation of the circuit, which turned out to be 125MHz, decreasing it progressively. We started from the highest frequency to observe the trend of the maximum power and energy used by the transmitter. The results obtained are shown in Tab. 3 and in the graph in Fig. 7. Results show dynamic power increasing linearly with the increasing of the frequency in accordance with Eq. 2.

$$P_{dyn} = a * C * f * V_{DD}^2 \quad (2)$$

where a is the switching activity, C is the switching capacitance, f is the clock frequency and V_{DD} the supply voltage.
Note that at varying of clock frequency, the energy per OFDM-symbol remains about the same. This aspect suggests that the same architecture is synthesized by the tool without the necessity to introduce/duplicate new hardware for reaching high frequencies.

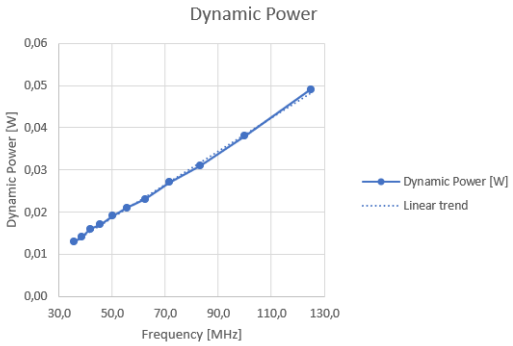

Figure 7: Dynamic Power trend.

4. Conclusion

The paper proposes a low-power FPGA implementation of an NB-IoT OFDM transmitter. The proposed architecture has been developed in VHDL and implemented on a Xilinx FPGA. Results are provided in terms of utilization resources and power consumption. For what concerns

Table 3
Power and Energy Trend in Frequency

Clk Frequency	Power (tot)	Dynamic Power	Sym. Energy
$35.71MHz$	$0.032W$	$0.013W$	$4.732 * 10^-9J$
$41.67MHz$	$0.034W$	$0.016W$	$4.992 * 10^-9J$
$50MHz$	$0.037W$	$0.019W$	$4.94 * 10^-9J$
$62.50MHz$	$0.042W$	$0.023W$	$4.784 * 10^-9J$
$83.33MHz$	$0.05W$	$0.031W$	$4.836 * 10^-9J$
$100MHz$	$0.056W$	$0.038W$	$4.94 * 10^-9J$
$125MHz$	$0.068W$	$0.049W$	$5.096 * 10^-9J$

this latter, power characterization has been provided taking into account the energy dissipated for an OFDM symbol transmission. Results show a very reduced utilization of resources and power consumption. These two aspects are very important for IoT nodes that are characterized by strict energy consumption requirements and low cost .

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