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Bilevel Alarm Monitoring Multiplexer

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BILEVEL ALARM MONITORING MULTIPLEXER

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ABSTRACT

This report describes the operation of the Bilevel Alarm Monitoring Multiplexer used in the Adaptive Intrusion Data System (AIDS) to transfer and control alarm signals being sent to the Nova 2 computer, the Memory Controlled Data Processor, and its own integral Display Panel. The multiplexer can handle 48 alarm channels and format the alarms into binary formats compatible with the destination of the alarm data.

BILEVEL ALARM MONITORING MULTIPLEXER

Summary

The Bilevel Alarm Monitoring Muliplexer is designed to interface the Adaptive Intrusion Data System (AIDS) to incoming alarms from intrusion sensors being operationally tested in the field. The chassis will accept up to 48 alarm channels, register their occurrence on its own display and transmit them to the Memory Controlled Data Processor (MCDP) for inclusion in the data stream, and to the Nova 2 System Controller for sequence initiation. The Nova 2 will type the alarm channel number and the time of the occurrence on the Silent 700 teletype. The multiplexer contains camera control and windowing circuitry to allow properly timed alarms connected to that circuitry to trigger a relay which in turn is used to open shutters on film cameras. An audible tone generator is mounted on the rear of the chassis. The tone generator is activated by the presence of a sensor alarm signal and remains on until the latches are reset. The tone generator can be disabled if the operator does not desire to use this feature.

The front panel of the multiplexer chassis is shown in Figure 1. The panel displays 48 light- emitting diodes (LED) which are activated whenever an alarm triggers the circuitry. The LED's are arranged in groups of six lights which correspond to the manner in which the channels will be placed into the output data stream of the MCDP. Groupings of twelve indicate the way the Nova 2 receives the data. A front panel switch permits selection of either direct or latch modes. In the direct mode, the lights will be activated only by the presence of a signal on an input line. By utilizing the direct mode, the operator can scan the LED panel and determine if any line is being held high. He can also time the period of an alarm sensor pulse, if the pulse is long enough for this type of visual determination.

Figure 1. Front Panel

In the latch mode, whenever a channel is activated, the light will come on and would stay lit until the reset button is pushed. The reset button clears all latches and turns off all LED's.

Mechanical Description

The Bilevel Alarm Monitoring Multiplexer is built into a standard 19" chassis with a 3-1/2" front panel. The arrangement of the electricial components inside the chassis can be seen in Figure 2. The logic circuitry is built on the one 180 integrated circuit (IC) socket Augat board. The board is a multi-layer board with the top and bottom portions of the board being a ground plane. A power plane is sandwiched in the center of the board. Pins 16 of the sockets are common to the power plane and Pins 8 are common to the ground planes. The sockets are arranged in groups of 30. When an operator views the chassis from the top, standing at the front panel side, he will see groups labeled A through E, proceeding from left to right, respectively. Each socket inside the group is numbered from 1 to 30. Designation of IC's thus can be identified by the nomenclature such as

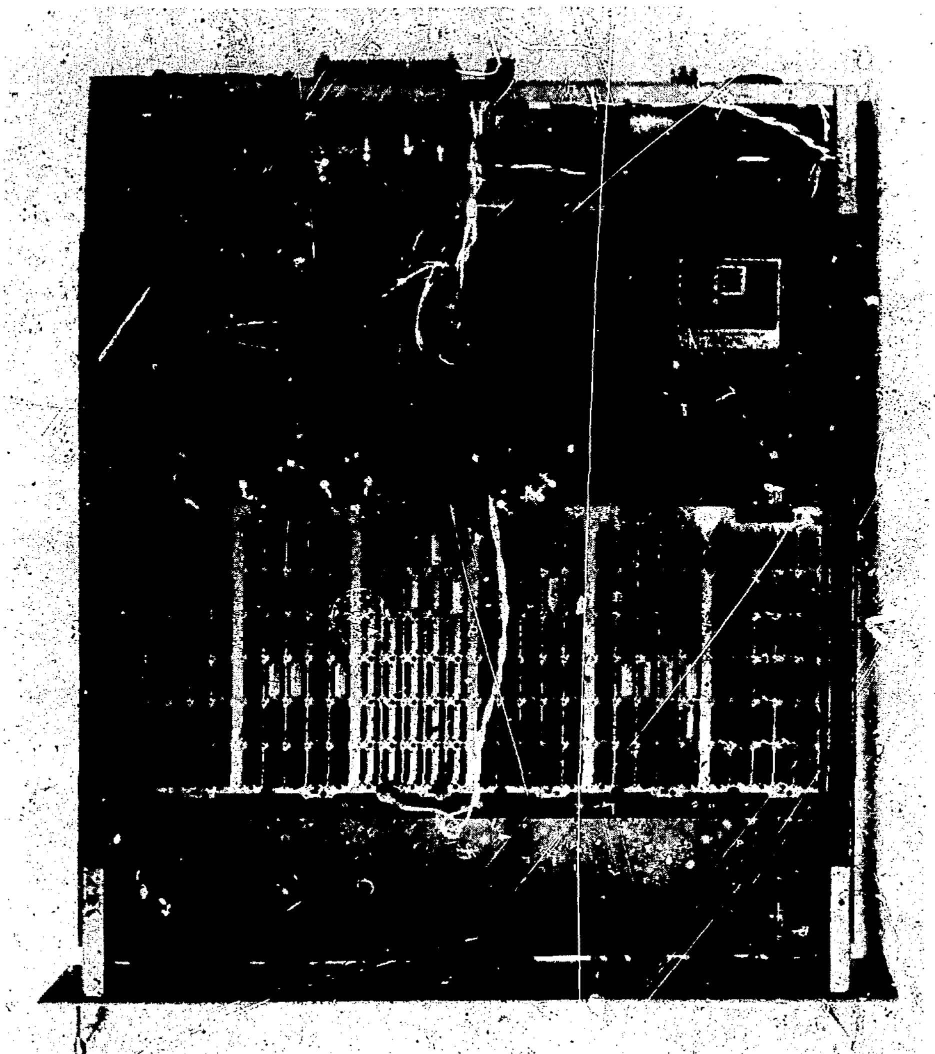

Figure 2. Top View

A20 or E30, indicating the group and socket where a given IC is installed. Connections to the outside world are made from the board via the 12 connectors located at the rear of the board. Power is supplied separately via a twisted cable running from a Lamda ABA-LOS-Y-5-1 power supply. A small modular Semiconductor Circuits power supply furnishes the voltage for the front panel light. Also mounted with that power supply is a driver transistor for the Sonalert tone generator.

The rear of the chassis is shown in Figure 3. It contains the AC power connector and five flat ribbon connectors labeled J1 through J4. J1 is an alarm input connector. J2 is a connector for the cable going to the Nova 2 computer. J3 connector transfers signals between the chassis circuitry and the Memory Controlled Data Processor. J4 connector provides inputs and outputs for the camera control circuitry. The signals to the electrical counters for counting camera exposures come out of the J5 connector. The switch present on the rear panel disables the Sonalert that is installed in the rear panel.

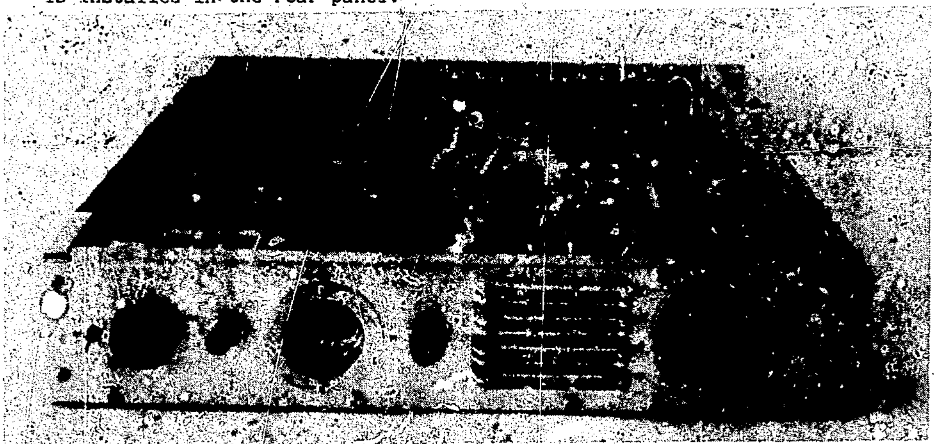

Figure 3. Rear of Chassis

Nova 2 Interface

The Nova 2 computer uses the information available in the Bilevel Alarm Monitoring Multiplexer to determine when an alarm occurs. An alarm signal on a line will set a flip-flop latch indicating the occurrence of a particular alarm. The Nova 2 can read the latches to ascertain which alarm has occured. The interface to accomplish this task is done via a MDB computer interface board in the Nova 2 computer. This MDB board accepts signals from the Nova software and translates them to signals which will be recognized and operated upon by the alarm monitoring chassis. The Nova 2 codes for the alarm monitoring multiplexer are summarized in Table I. The device code is a 27_8 code for the Nova.

There are four main functions accomplished through the Nova interface. The first one is a DOA output command with an indicated code on the 16-bit output bus asking for a designated 12-bit group of bilevel information. The chassis receives this command, decodes the request, and places the 12-bits on the data bus which is in turn latched into the input registers on the MDB board. Next, the Nova may output a DIA command which will cause the data to be shifted from the storage latches in the MDB board onto the Nova bus. A complete transfer of all the bilevels can be accomplished in four DOA, DIA commands with the proper bilevel word indication. The Nova issues two other commands to the alarm monitoring chassis. These commands are an IOPLS pulse which will clear all of the data laches that have received alarm signals from the outside world. The second is a "Clear" pulse issued to clear the interrupt circuitry in the alarm monitoring chassis.

Functional Electrical Diagram

The bilevel alarm monitoring chassis contains two sets of latches which are used to indicate the presence or occurrence of an intrusion alarm (Fig. 4). The signal from the alarm system is buffered from the outside world through a 10 K resistor into the input of a C-MOS inverter gate. The C-MOS inverter gate is protected by a 12 volt zener and referenced to ground through a 2.2 megohm resistor. This gives the bilevel alarm

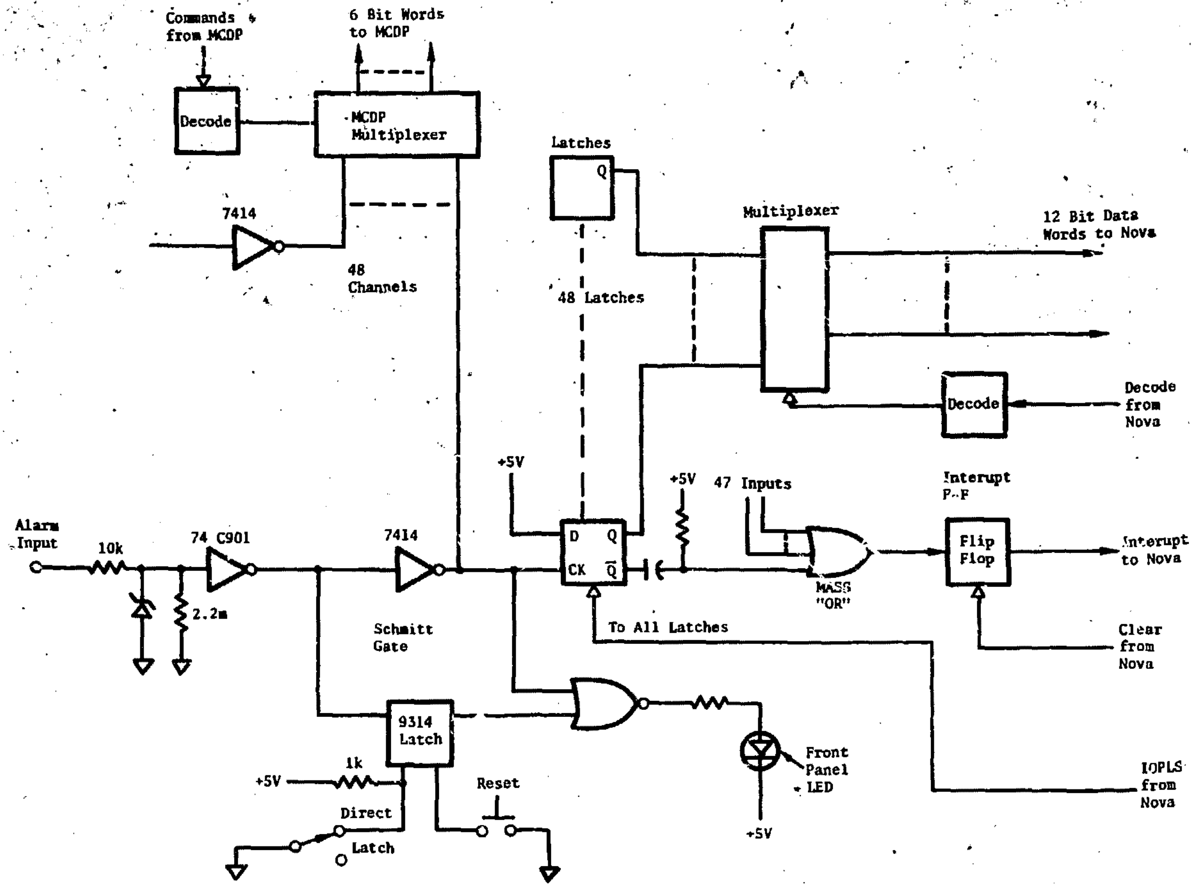

Figure 4. Bi-Level Alarm Monitoring Multiplexer Functional Diagram

monitoring signal lines a nominal 2.2 megohm input impedance until the input voltage exceeds the threshold of the 12 volt zener. The output of the C-MOS gate 74C901 is fed to two separate latching systems. One output goes to a 9314 latch. Whenever the input signal on the alarm lines goes high, it will be translated to a low going signal by the first inverter and applied to the 9314. This will set the latch in the 9314 to a permanent high condition if the enable lines are pulled high for the 9314. The output from the 9314 is fed to a "NOR" gate which upon having a high going logic signal appled to it will cause its output to go low and furnish a ground for a front panel LED. The data contained on the alarm information will remain in the 9314 latch until the latch is reset. All latches are simultaneously reset by the reset button on the front panel. If the latch is disabled by grounding the enable line and the system is put into the direct mode, then a signal on the input of the 9314 will not be stored. The LED will be lit only by the input signal passing through a Schmitt gate to the "NOR" gate LED driver. In the mode labeled "direct," the LED will remain lit only as long as an alarm signal remains high on the input to the bilevel alarm monitoring chassis. The latching system is used by the operator to determine whether an alarm has occurred momentarily when he was not present. By using the direct mode, an alarm line can be directly observed.

The second set of latches consists of a group of SN7474 flip-flops. The incoming signal that has been shaped up by Schmitt inverter gate is applied to the clock input of the flip-flop. With the "D" input tied high the edge of the alarm signal will clock a "1" into the output. Any additional transitions on the flip-flop lines will be ignored until the flip-flop is reset. If, by chance, the flip-flop input signal goes high and stays high, it will not present a permanent "1" to the output since the input requires a transition in order to clock a "1" into the "Q" output even after it has been cleared. This arrangement provides a lock-out feature for any alarm lines that go high and remain high. The output of the flip-flops is fed to a group of multiplex gates which may be interrogated by a signal from the Nova 2 computer. The "Q" output of the flip-flops is tied through a capacitor resistor network to the input of a large "OR" gate. The transition of the "Q" output of the flip-flop causes a pulse to be generated and sent through the large "OR" gate to set a flip-flop. This flip-flop sends an interrupt that can be recognized by the Nova computer. The computer in turn can issue a clear command to remove this interrupt at any time. This feature was originally designed into the system to generate an interrupt signal to be fed to the Nova 2 whenever an alarm occurred. However, it is not utilized in the "run" mode of the program since some software constraints made it difficult to implement in the real-time "run" situation. Instead the Nova 2 continually samples all of the outputs of the gates in the bilevel alarm monitoring chassis and with this information decides when an alarm has occured.

The Nova 2 interrogates the stored latches consisting of the 7474 flip-flops from a decode network through the multiplexer. Twelve bits of information are strobed into the Nova at each request for date. After the latches have been read, the Nova 2 will issue an IOPLS pulse to clear the latches. The interrogation routine occurs about every 50 milliseconds so that the Nova 2 is constantly looking for the occurrence of new alarms in the bilevel alarm monitoring chassis. After an alarm has occurred, the Nova 2 becomes busy performing a multitude of tasks associated with the data collection. It will now stretch its interrogation time to approximately 1 second when it will determine if any new alarms have occurred in the previous second. If they have, it will take action to continue to collect data for an additional time period. If no new alarms have occurred it will sample again in one second. The Nova continues its one second interrogation routine until the time period of collecting and recording data on tape has been completed when it will revert to the 50 millisecond interrogation cycle.

The outputs of the 7414 Schmitt gates are routed to the Memory Controlled Data Processor (MCDP) multiplexer. Upon command from the MCDP, the status of the alarm lines will be transferred to the MCDP for inclusion into the MCDP data output. Groups of 4 six bit words are transferred to the MCDP. Line status is not dependent upon any transitions, and the data transferred is the actual "high" or "low" condition of the alarm signal lines. Table II shows the organization of the bilevel words and the order in which they are transferred from the Bilevel Multiplex to the MCDP.

TABLE II

Channel Organization of AIDS

Bilevel Words

		MSB			LSB	
Channel Code		6_8			0_8	
1	1	0	0	0	0	
		Channel Numbers				
1st word	1	2	3	4	5	6
2nd word	7	8	9	10	11	12
3rd word	13	14	15	16	17	18
4th word	19	20	21	22	23	24
Channel Code		6_8			1_8	
		Channel Numbers				
1st word	25	26	27	28	29	30
2nd word	31	32	33	34	35	36
3rd word	37	38	39	40	41	42
4th word	43	44	45	46	47	48