

thick strip detectors (about 20 pF capacitance load per strip) and six ABCD readout chips were built and tested [2] using both the test setup and the H8 beam at CERN. A set of test setup measurements was taken before detectors were connected and subsequently for the complete module. Fig. 2 shows the noise increase from about 900 el rms up to 1600 el rms after connecting the detector, which is close to the expected value.

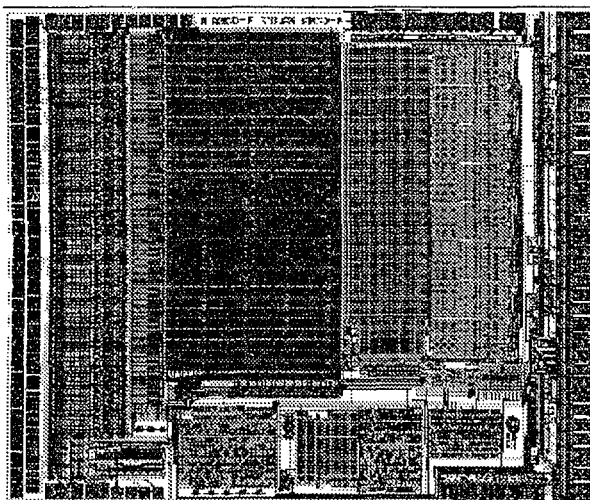


Fig. 1: Layout of the ABCD chip.

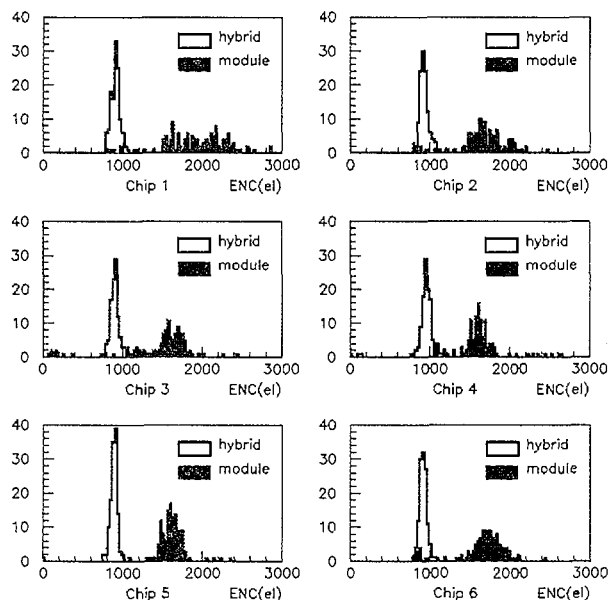


Fig. 2: Distribution of noise without (hybrid) and with detectors connected (module).

The performed tests have proven the full digital functionality of the prototype, however uniformity of some analogue parameters across the chip, in particular of the discriminator offset, has to be improved. The design of the chip has been optimised to meet all the ATLAS specifications. The new batch of chips is expected to be manufactured in the first months of 1999.

References:

- [1] W. Dąbrowski et al., (J. Kapłon, R. Szczygieł, M. Wolter - from INP), "The ABCD binary read-out chip for silicon strip detectors in the ATLAS silicon tracker", presented at IV Workshop on Electronics for LHC Experiments, Rome September 98, CERN/LHCC/98-36 30 October 98, p. 175;
- [2] D. Ferrere et al., (J. Kapłon, R. Szczygieł, M. Wolter - from INP), "Test on ABCD Chips", ATLAS int. note ATL-INDET-98-217.

High Speed Data Transmission Design

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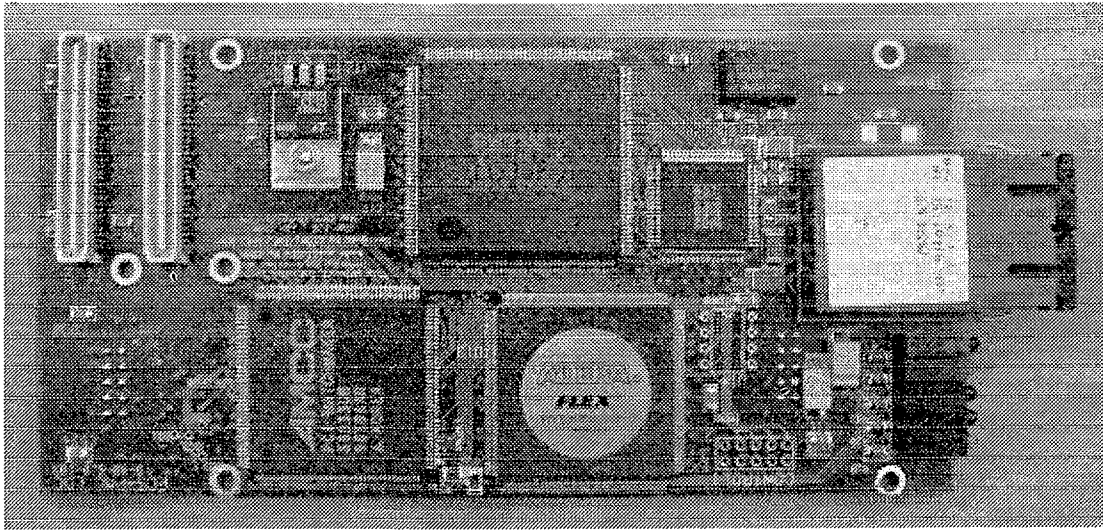
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An optical 1 Gbit/s link has been suggested as a medium to transfer the data between front-end electronics and read-out systems in ATLAS at LHC. It was also proposed to have the S-Link as a standard defining a connector for this kind of transmission. Although the mechanical standard of a link hasn't been chosen yet, there are a few ongoing projects which develop designs for these purposes. One of them is the Fiber Channel Slink destination module realized as a PCI mezzanine card (FCS-PMC). The card is a merger of 2 existing modules: Fiber_Channel_Slink [1] and Slink_to_PMC [2] modules and has been designed in collaboration of our Institute with KFKI Budapest and CERN. The primary goal of the project is to produce the PMC card, which can easily be installed on commercially

available VME crate controllers, as the most of the test read-out setups is built in this standard. Equally important, the secondary goal is to investigate a possible incorporation of a time critical and demanding part of the high speed link design into local, front-end electronics designs.



The FCS-PMC module itself consists of 2 independent logical parts: the Fiber Channel Slink part and the PCI/PMC part. The first one contains duplex optical transceiver, data serializer, encoder/decoder and 10k30 Altera chip. This part converts Fiber Channel compatible serial data into/from parallel 32 bit wide Slink data. The second part contains FIFO, 7032S Altera chip and PCI coupler and exchange the Slink data between the FCS-PMC and a host computer over the PCI bus. All components are assembled on 2 sides of the 8 layer PCB (see the photograph). Actually, the first prototype of the module is under tests.

S-LINK test software, written under Windows95 system consists of two parts. The first one (SPS - "transmitter") controls the PCI-to-S-LINK interface, the second one (SSP- "receiver") serves the S-LINK-to-PCI unit.

The software consists of a *VXD driver*, operating in the Ring 0 of the Win95 system, for fast control of the hardware, a *DLL library*, acting as a bridge between the VXD driver and high level language applications, and a *Win32 application*, equipped with Graphical Interface for easy manipulation of the test program. A Win32 part has been developed using the Visual Basic and it is dedicated to the S-LINK tests only. DLLs and VXD's present a reusable code which can be used as a base for development of other S-LINK applications.

References:

1. [http://www.rmki.kfki.hu/detector/S-Link/;](http://www.rmki.kfki.hu/detector/S-Link/)
2. [http://www.cern.ch/HSI/s-link/devices/slink-pmc/.](http://www.cern.ch/HSI/s-link/devices/slink-pmc/)



Designing of Silicon Strip Detectors for ATLAS

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The ATLAS Silicon Tracker will contain several thousand of silicon strip detectors. Such big quantity requires few potential vendors of detectors. One of them is CSEM (Centre Suisse d'Electronique et de Microtechnique) in Neuchatel, Switzerland. Our group has established the cooperation with CSEM since 1996. Our task is to design the set of masks for photolithography required for detector processing at CSEM.

Since each factory has its own specific technology ATLAS Collaboration prepares only generic technical specification for detectors. Detailed problems of design must be resolved by designer according to specific "design rules".