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IPNO 99-01

A Full-scale prototype for the tracking chambers of the ALICE muon spectrometer Part II- Electronics: Preamplifier, Read-out prototype

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Abstract

A full scale prototype of one module of the first tracking station has already been contructed. It will be equipped with the new read-out electronics proposed for the final chambers. Before integration of the whole chain, tests have been carried out on the individual components in discrete circuit prototypes. In this report the different parts of the chain are described, together with the tests performed. The final version with integrated circuits is then described.

Acknowledgements

This realisation has been possible thanks to the effort of many collaborators at the IPN. Among them, we are particularly grateful to:

- D. Desveaux, D. Rougier, P. Guilland and S. Royer circuits who helped in the realisation of the circuit designs.

- S. Pré who essentially did most of the cabling and to the team who helped supply the basic materials

The collaboration with the R&D detection team has been very fruitful and we duly thank this team for their contribution.

We would like to thank F. Piuz for many helpful discussions and J.C. Santiard for providing the GASSIPLEX modules and for the subsequent modifications he made following our desires. Without the help of P. Martinengo, A. Di Mauro and the CERN DAQ team, the in-beam tests would not have been so efficient.

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1. INTRODUCTION

The performance specifications for the ALICE dimuon tracking arm are as follow [1]:

- a spatial resolution of less than 100 μm per plane in the bending plane of the spectrometer and less than 2 mm in the non-bending plane.
- an average thickness below 2 to 3% of one radiation length per plane.
- the capacity to work for particle densities up to 3.10^{-2} cm^{-2}.
- a read-out time not exceeding 50 μs to allow the measurement of Pb-Pb minimum bias events while keeping losses to less than 10% [2].
- excellent reliability as access to the will be difficult during beam operating times. Consequently the breakdown of an individual detector component should interfere as little as possible with the overall detector performance.

In this report the detector under study is a Cathode Pad Chamber (CPC). The pad lengths vary as a function of the particle density in such a way that the detector occupation rate stays constant [3]. For the first tracking station the pad dimensions vary from 5x7.5 mm^2 in the center to 5x30 mm^2 at the edge.

The choice of detector with this particular geometry has several implications for the associated electronics implantation, and are as follows:

1- the length of read-out lines from the receptive pad surface to the preamplifier input must be minimal in order to keep added capacitive noise to a minimum. The overall spatial resolution is strongly dependent on the S/N ratio and so the preamplifier should be mounted on-board as close to the pads as possible.

2- the smaller pads at the center of the detector implies a high density of read-out electronics on the supporting printed circuit board. At the same time the density of holes to allow the feed through of the kapton cables from the pads to the preamplifier is maximum. Consequently, the space available for the transit of low voltage supplies and command signals to and from the detector is very limited [4].

3- in order to maintain a good reliability , long multiplexed preamplifier chains are highly undesirable as the breakdown of a single channel can perturb, or lead to the loss of, all the signals transiting through the chain. Longer chains also lead to longer sequential read-out times, this is also undesirable.

4- the transport of weak analog signals over relatively long distances is a difficult task which would not be simplified by the expected intense electromagnetic radiation. This would lead to increased noise picking on the signals. This situation will therefore to be avoided.

In order to test the first detector configuration, a prototype (ALICE2) was constructed and tested. The main aim of the tests was to validate the proposed read-out method using discretised electronics circuits (with numerisation, pededstal subtraction and zero suppression

carried out directly on the back of the detector) before going on to the next step of integrating the whole read-out chain on a single board.

The first problem resolved was the implantation of a high density of electronics over the smallest pad area at the center of the detector. Small sized circuits designed for the read-out of 64 analog signals from the pads were used successfully. This circuit named GAS64, is discussed in greater detail in chapter 2 and appendix 1.

Again due to the restricted space available, the GAS64 circuits were daisy chained so that a maximum of 512 channels could be read-out efficiently. The PCB is discussed in detail in chapter 3.2. This approach which constitutes an intermediate solution was successfully implemented and ensures the feasibility of the project should more ambitious solutions be unsuccessful.

In parallel, using the same detector, new electronics were implemented that provided read-out of analog signals, coding, pedestal subtraction, zero suppression and digital read-out. This system make use of the latest technology in circuit miniaturisation (naked chips, LCA *(Logical Cell Array)*, MCM *(Multi Chips Module)*, etc...) once the individual components have been validated and optimised. The tasks carried out by the individual parts have already been successfully tested on discrete component boards, without worrying about the overall circuit dimensions. The circuit, called NULOC (Numérisation LOCale) is described in detail in chapter 4. The development of the final circuits for the ALICE acquisition interface is still being carried out (for the SIU *(Source Interface Unit)*, DDL *(Detector Data Link)*, DIU *(Destination Interface Unit)*) and so a provisional circuit, provided by LAL *(Laboratoire de l'accélérateur Linéaire)*, called SPAC *(Serial Protocol for the Atlas Calorimeter)* was used.

The data acquisition system being developed for ALICE (named DATE) was used during the tests and is described in chapter 5.

This reports ends with a description of the next steps foreseen for the near future and addresses the modification of the GASSIPLEX circuitry and the manufacturing of a first MCM.

2. THE PREAMPLIFIER

2.1 The chip and its characteristics.

The GASSIPLEX [5-6] preamplifier developed at CERN has been used in the CPC studies. It is well adapted, give or take a few minor modifications, to the general characteristics of the CPC analog signals. It has a weak electronic noise and, is suitable for the charge integration and takes into account the delay on the trigger signal. This preamplifier, designed for use with either silicon or gaseous detectors, is currently undergoing further development. Recent technology will allow ultra-thin circuits (0.7 μm technology) to be made. However the microchips available during the tests described in this report are of the older 1.5 μm technology.

The preamplifier will not be described in detail, it is sufficient to underline that the GASSIPLEX module is an integrated circuit that works in asynchronous mode and continuously analyses the charge collected from the detector pads. It is composed of a charge preamplifier, a first order filter, a shaping amplifier and an analog memory where each signal amplitude is memorised (TRACK function) on reception of a HOLD signal. The working principle is given in figure $n^0 1$.

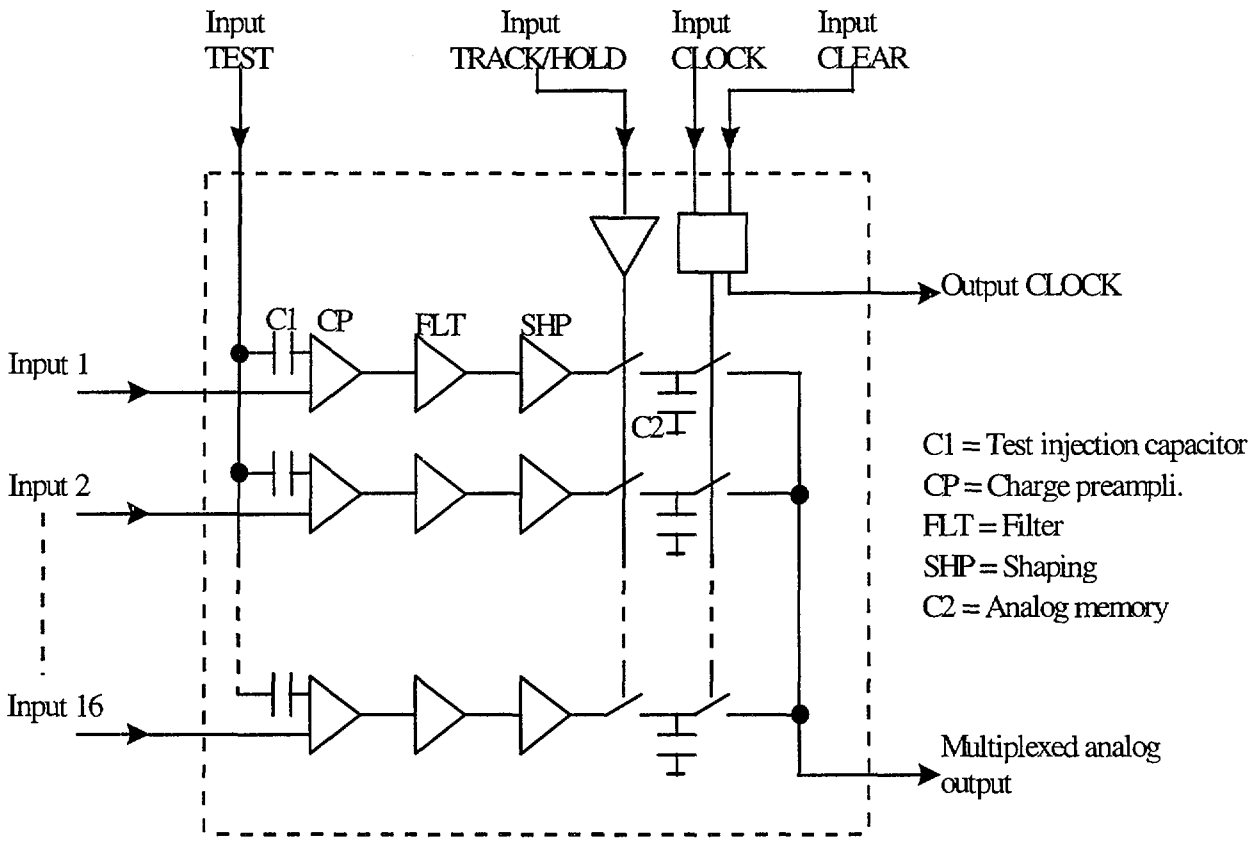


Figure 1. Working principle of a GASSIPLEX circuit

The stored charges are then sequentially read-out and coded by an external circuit. The read-out rate is controlled by a CLOCK signal and in our case was provided by the C-RAMS *(CAEN Read-out Analog Multiplexed System)* circuit. After reading all the data, the system is then released and cleared. The cycle starts again as the HOLD (memorise) signal passes to a track (observe) state. A diagram of the relative timing of the different phases is given in figure $n^0 2$.

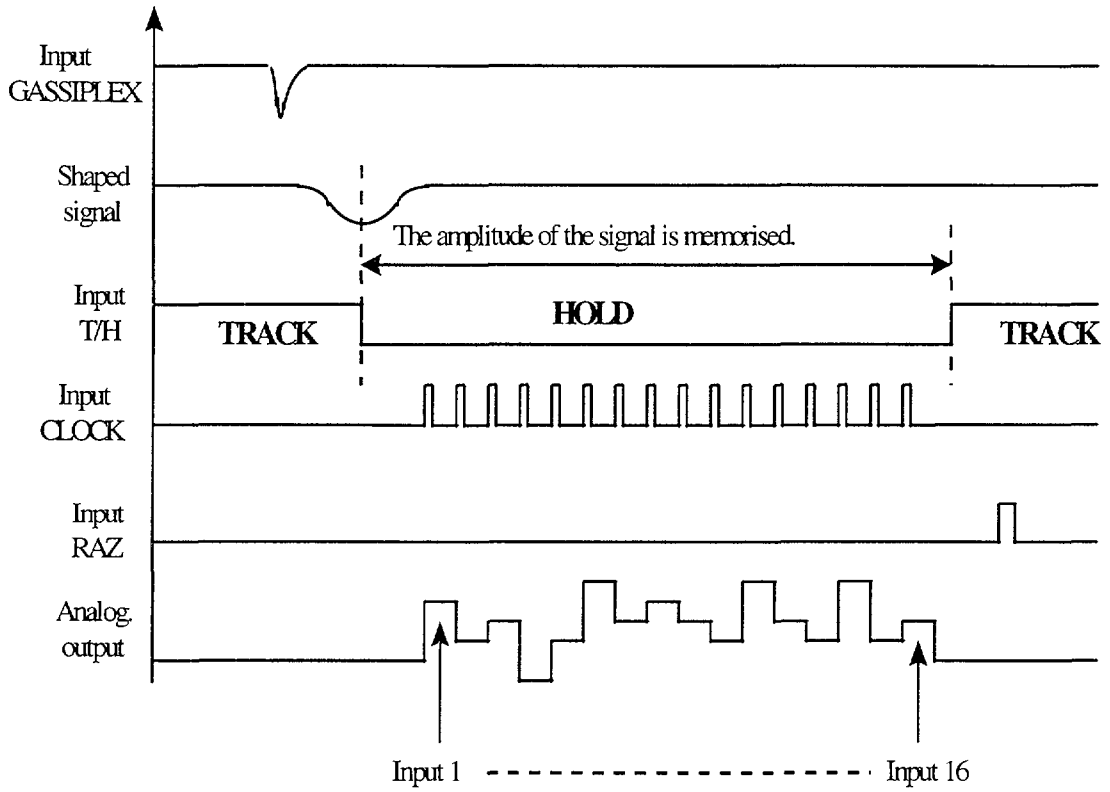


Figure 2. Relative timing of the GASSIPLEX functions

Charge injection on the test input allows to calibrate each of the 16 channels. A more detailed description of the GASSIPLEX functions can be found in reference [7].

The principal characteristics of the 1.5 µm GASSIPLEX measured by J.C. SANTIARD are given below:

- number of channels	16
- noise at 0 pF	650 e^- rms
- noise gradient	15 e^-/pF
- output range	0 to 2 V
- linear dynamic range	-75 à 150 fC
- sensitivity/gain	12.5 mV/fC
- peaking time	from 450 to 650 ns
- baseline restoration	<0.5% in 3 µs

- temperature coefficient	0.1 mV/^{0}C (for 500 ns peaking time)
- multiplexing frequency	15 MHz maximum
- power consumption	8mW/channel

The GASSIPLEX chips are easily daisy chained up to a maximum of 2048 channels (128 GASSIPLEX). The read-out process is authorised through a single line that transits all the modules, but the cost of a long daisy chain is increased read-out time and reduced reliability. To read-out in daisy chain mode all that is required is the transmission of the CLOCK signal from one circuit to the next and to send the same number of clocks as there are channels to be read (see figure n^{0}3).

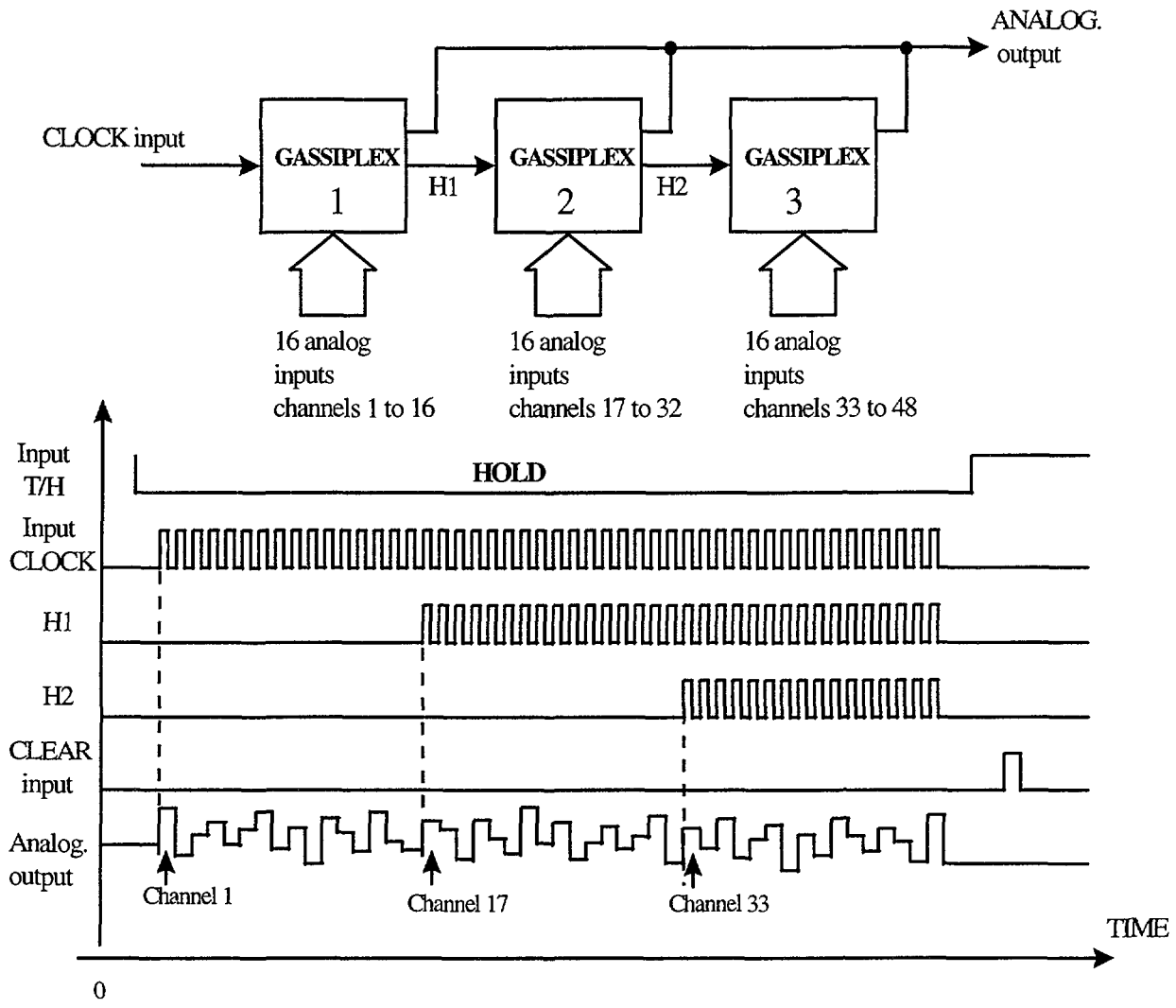


Figure 3- Daisy chain working mode

2.2 GAS64 Implantation

This electronic board (schematized in Figure $n^0$4) has to meet 4 requirements:

- demonstrate a high reliability for analog read-out in the standard daisy chain mode with reduced circuit dimensions that allow to populate the high density zone of the detector.

- necessity to use an output impedance adaptator (provided by the amplifier) for the transmission of signals via a coaxial cable.

- be flexible enough to allow different electronic solutions to be tested, namely the more evolved solution of local numerisation (NULOC).

- to be easily implemented on the ALICE2 prototype.

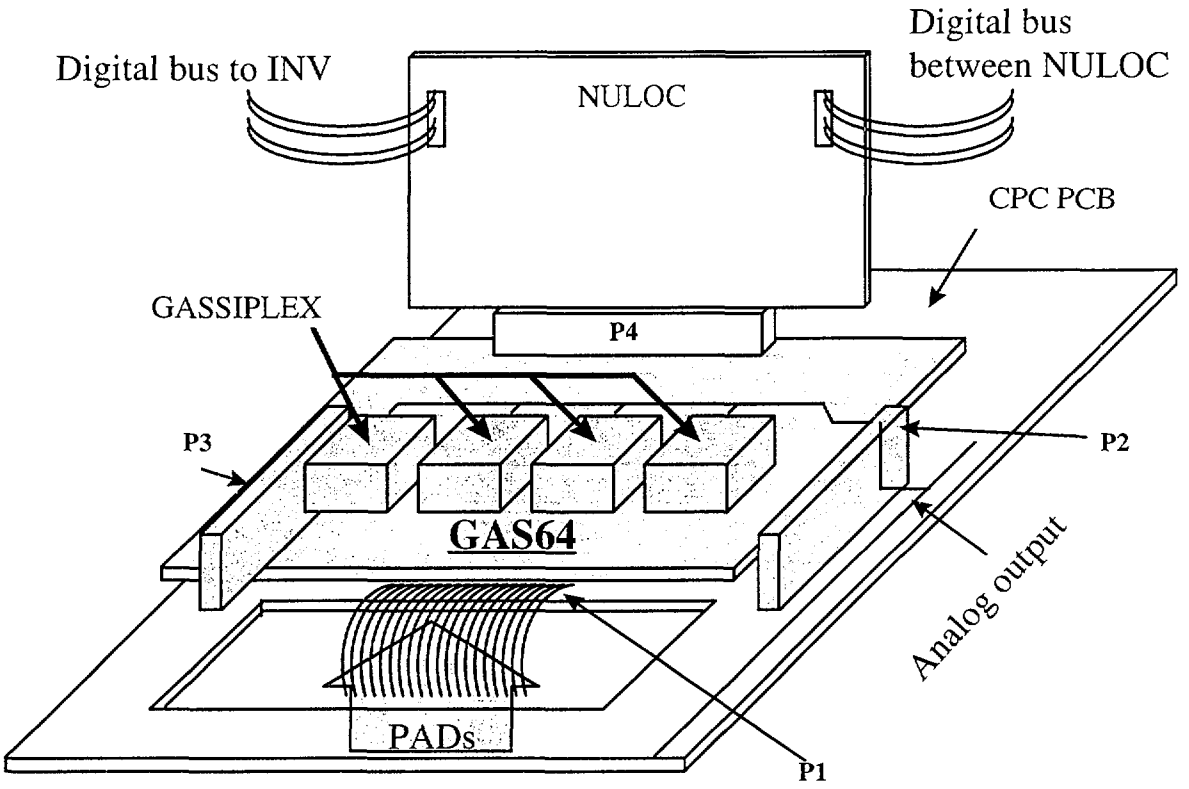


figure 4. GAS64 schema

The GAS64 contains the following elements:

- 4 ceramic encapsulated 1.5 µm GASSIPLEX modules and the associated circuitry required for their use. There are therefore 64 analog channels input to one GAS64 board.

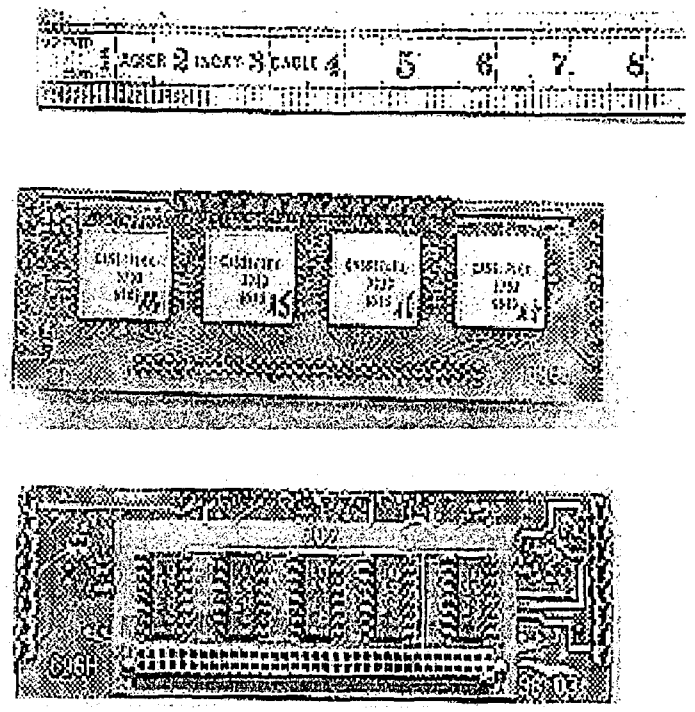
- one 70 pin connector (P1) that provides the liaison with the pads via a kapton cable.

- two 8 pin connectors (P2 and P3) that ensure the connexion with the chamber's PCB. They provide access to the voltage supplies and allow the command signals to be transmitted.

- a 14 pin connector (P4) that connects the GAS64 to NULOC or an analog buffer.

Several GAS64 circuits were also designed with implanted sparking protection. A complementary study has yet to be carried out to test the efficiency and requirements of these protections. This will be done by purposefully provoking discharges in the detector.

Photograph n^0 1 shows the two sides of the GAS64 circuit.



Photograph 1- A view of the two sides of the GAS64 circuit with the GASSIPLEX (above) and the implanted sparking protection on the back face (below). The scale is approximately 1.

Implantation and cabling details are given in Appendix 1.

2.3 First experimental results

A total of 40 GAS64 circuits were made and tested in the laboratory. The electronic noise and pedestal value of each channel was measured before connexion to the detector. In the following, the results for 18 of the GAS64 circuits are discussed.

2.3.1 Electronic noise

- *Noise Levels*: The GASSIPLEX output amplitudes are coded by the CAEN V550 ADC module (C-RAMS). These ADC's code linearly on 10 bits and were used over a range of

0 to 1500 mV, giving 1.465 mV/channel over 1024 channels. The read-out frequency was fixed at 500 kHz (which is 10 times less than the maximum possible frequency of the ADC's and 20 times less than the maximum GASSIPLEX frequency).

In figure $n^0 5$ the average noise value measured for 1152 channels is shown. The values reflect the noise on the GASSIPLEX+ADC chain. The scale is in elementary ADC units.

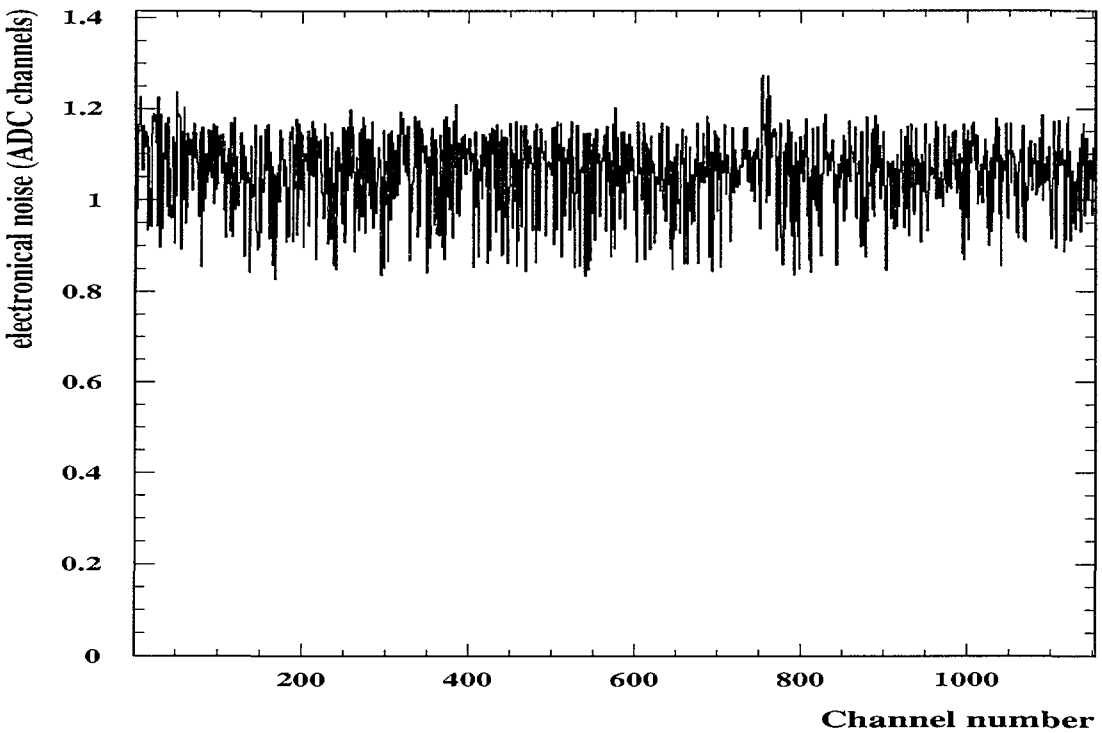


Figure 5. Measured electronic noise in ADC channels as a function of the channel number.

It can be seen that the average noise level is within a range of 0.85 to 1.2 ADC channels and that there is an excellent homogeneity between the different channels. In figure $n^0 6$, the projection of the noise levels is shown and gives the frequency of each noise value. The average noise level corresponds to 1.056 elementary ADC channels i.e. 1.55 mV. Given a GASSIPLEX sensitivity of 12.5 mV/fC and an output buffer gain of 0.96, the average electronic noise is estimated to be:

$$1.056\ (1.45/0.96)\ .\ (6250/12.5) \cong 800 \text{ electrons}$$

- *Noise dispersion:* Again, looking at figure 5, the width of the noise distribution is roughly σ=0.09 channels i.e. around 0.125 mV

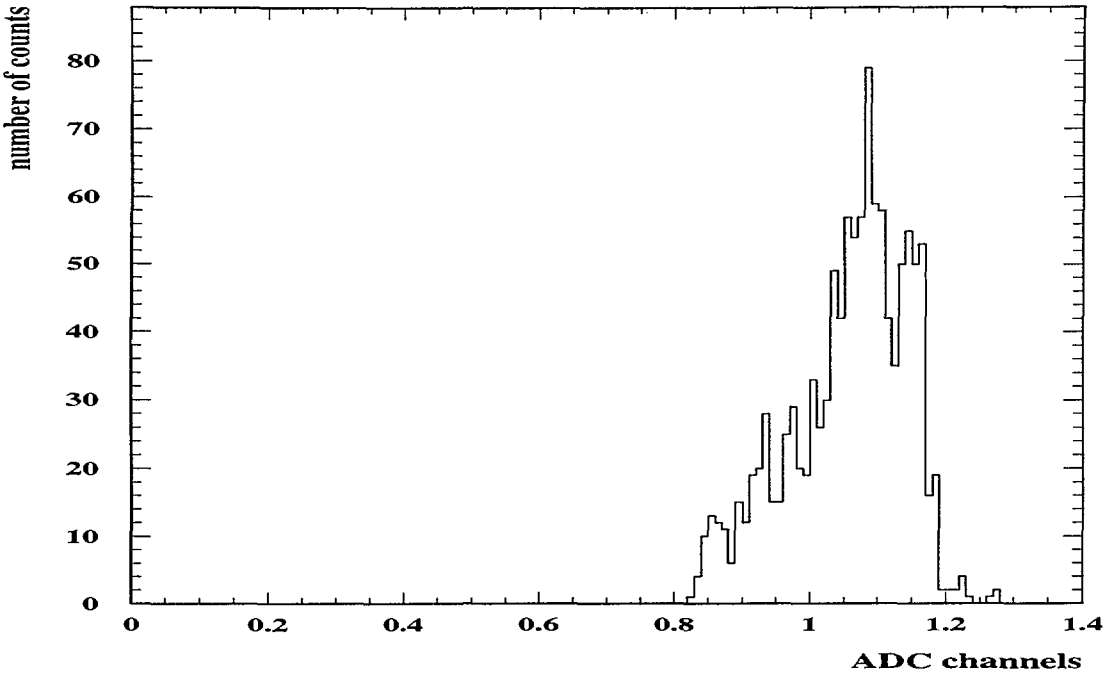


Figure 6: Distribution of the measured electronic noise

2.3.2 Pedestals.

Pedestals values are set by the use of a variable potentiometer that is common to all channels of a given GAS64. All pedestals must lie in the negative range of values as it is the input polarity required for the ADC. Large discrepancies between pedestal values on any given GAS64 board leads to the loss of dynamical range. The overall effective coding range will lie between the ADC value of the highest pedestal measurement and the ADC value of the channel that saturates the quickest. Large pedestal and gain disparities can therefore lead to drastically reduced dynamical ranges. Individual discrepancies between GAS64 boards can be minimised by adapting the resistance of the pedestal voltage line. All GASSIPLEX chips are first regrouped into 4 pedestal classes. Only chips from the same group are mounted on the same GAS64. The GAS64 boards are then adapted in order to obtain a maximal homogeneity in the pedestal values. The four pedestal classes are as follows:

- from 0 to 20 mV
- from 20 to 50 mV
- from 50 to 110 mV
- above 110 mV

and are associated with 4 resistance values.

Figure $n^0 7$ shows the average pedestal value after selection, measured for 18 GAS64 boards as a function of the channel number. The projection of this figure, as shown in figure $n^0 8$ allows to quantify the pedestal distribution over all the channels, and consequently, to estimate the overall effective ADC dynamical range.

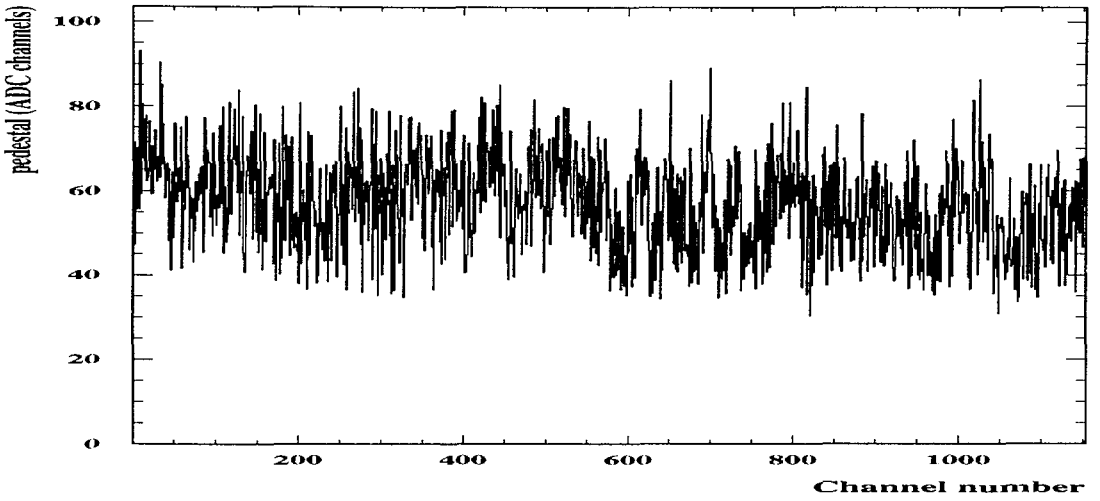


Figure 7: pedestal values versus the channel number

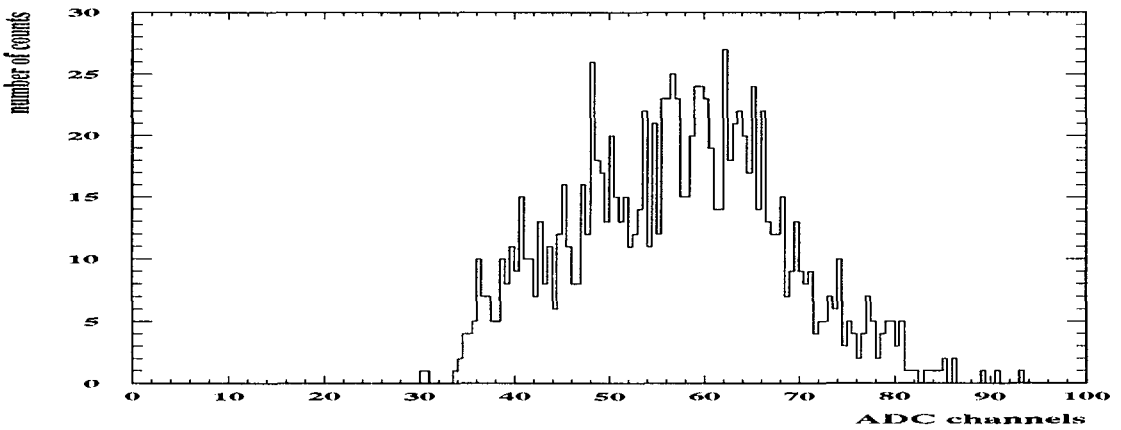


Figure 8: pedestal distribution

2.3.3 Linearity

The linearity of each channel is measured by injection of a signal on the test lines of each GASSIPLEX module. Roughly seven different amplitudes are injected using a passive attenuator and the measured output ADC values are recorded. It is important to note that although the test capacitors are of high precision, they are not all of equal value and so the precision of the calibration measurements is difficult to evaluate. Due to the way in which the GASSIPLEX modules are implanted there is also a noticeable difference in the perceived

effective gain for certain GASSIPLEX channels. The injected charge transits through the module going from the 16th channel to the first. The 16th channel systematically shows a higher a higher effective gain as there is some parasitic pickup between this channel and the injected charge itself. The injected charges vary between 0V and 1300 mV approximately. It is important to note that in the 0V measurement the input to the passive attenuator is unplugged, as opposed to the GASSIPLEX input, in order to maintain the same impedance on the test line. A typical set of calibration curves for 512 channels is shown in figure n^0 9

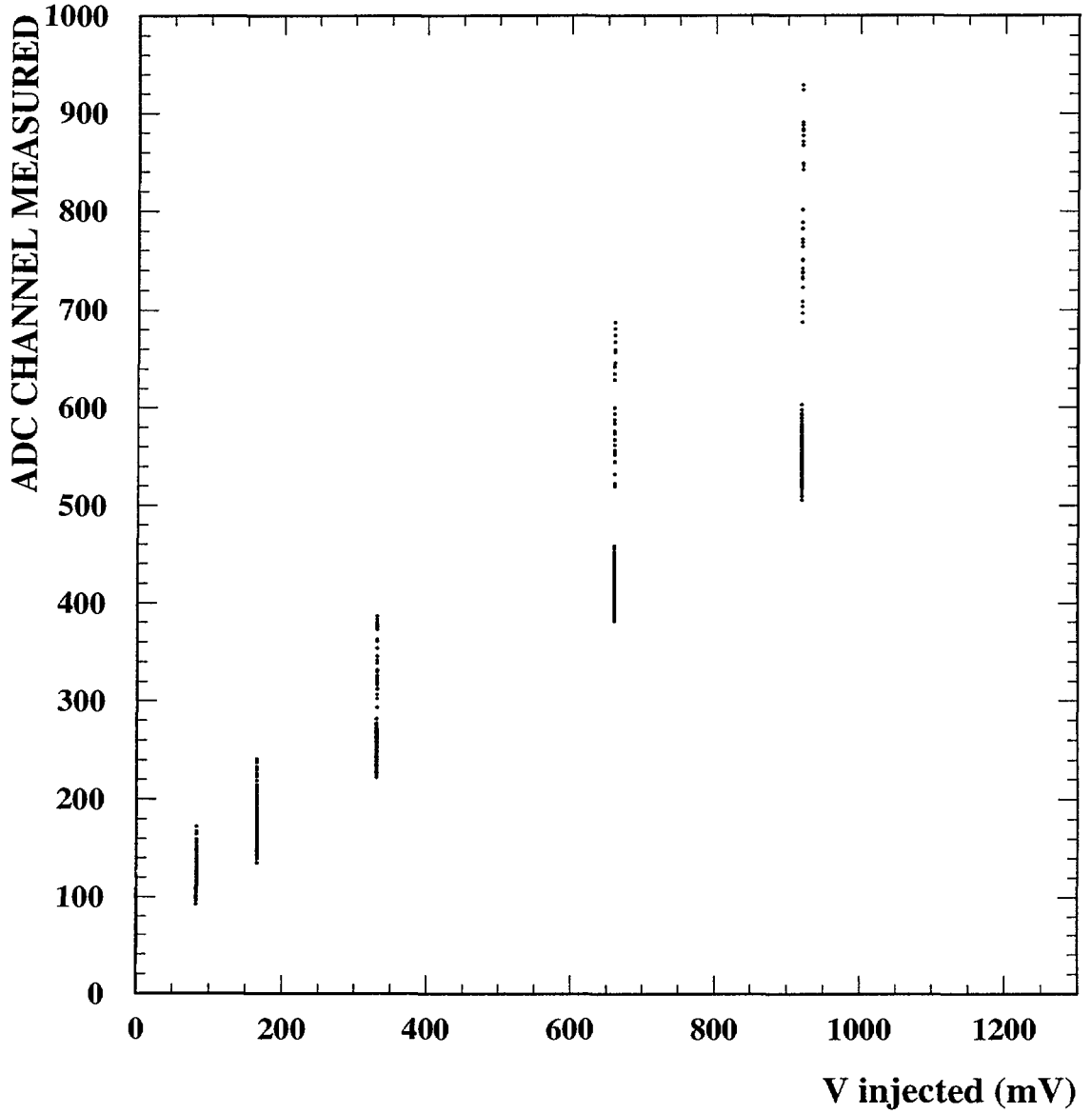


Figure 9:

Each individual channel is fitted by a straight line:
ADC channel = effective Gain x $V_{injected}$ + pedestal

In a given chain of GASSIPLEX modules, the channel that saturates the quickest is noted and is used for software cuts in the offline analysis. The 0V measurement is not included in the fit as it corresponds to the pedestal measurement. Instead, using the straight line fit, the pedestal measurement is calculated and compared to the equivalent measurement taken on-line during

the data acquisition. In all the tests carried out so far the predicted pedestal values and experimental values correspond to within the measured noise levels. This confirms that the calibration configuration is comparable to the data taking setup. In figure n^0 10. The calibrated GASSIPLEX effective gain are shown for 512 channels. The gain values correspond to the slope of the straight line from the individual fits. Figure n^0 11 shows the gain distribution values and figure n^0 12 shows the difference between the calculated and experimental pedestal values per channel. Finally, figure n^0 13 displays the distribution of the values, shown in figure n^0 12. It is worth noting that the distribution peaks at ~1.2 ADC channels, this is the experimental level measured. One in every 16 channels shows an apparent higher gain than the average values. This is due to pickup on the test injection line for the 16^{th} channel of every GASSIPLEX as previously discussed. This problem will be rectified in future versions.

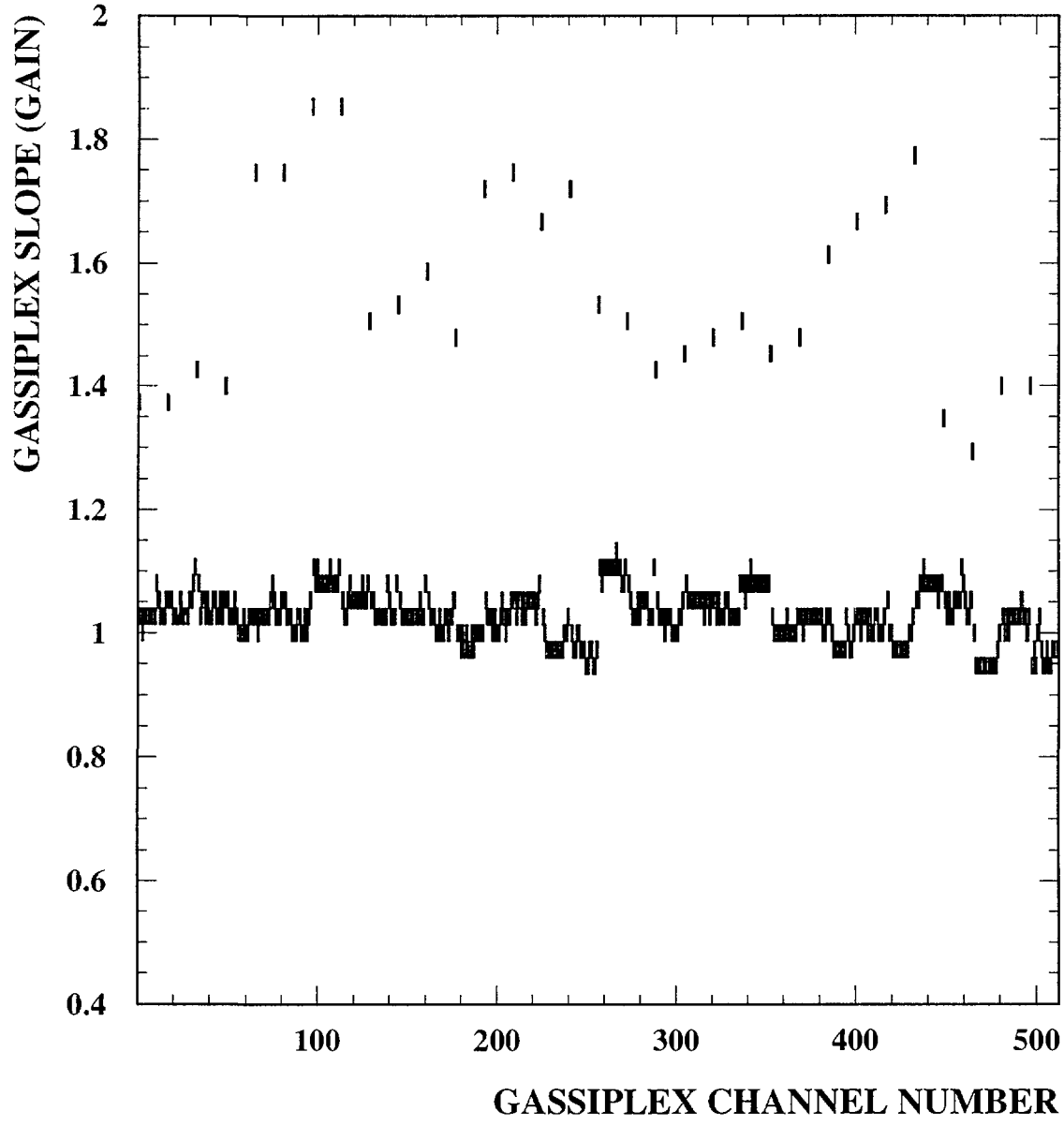


Figure 10

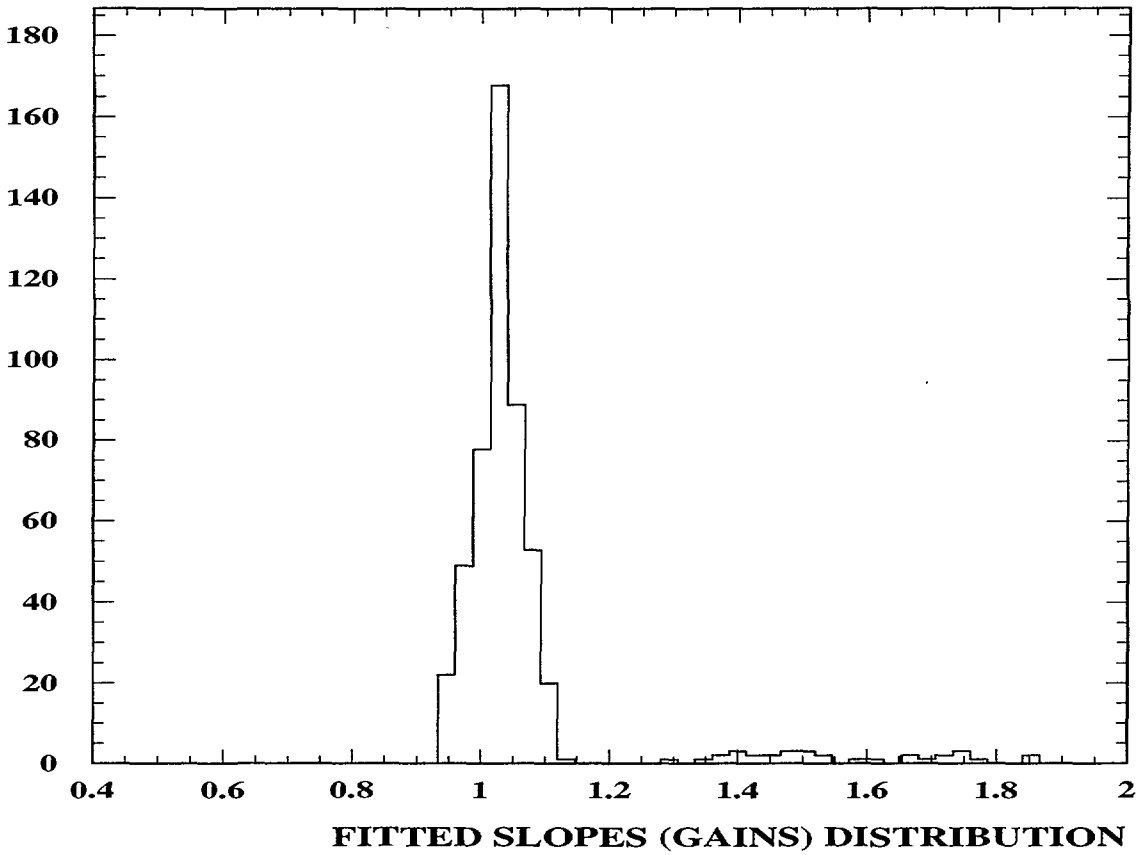


Figure 11:

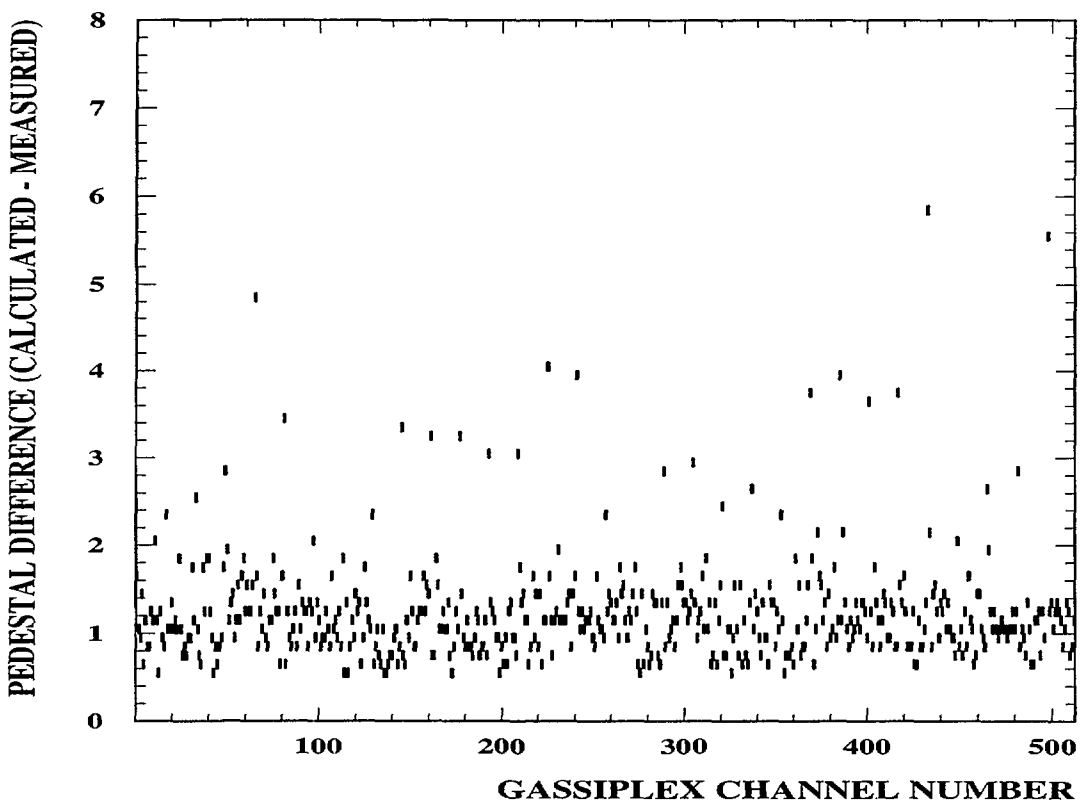


Figure 12:

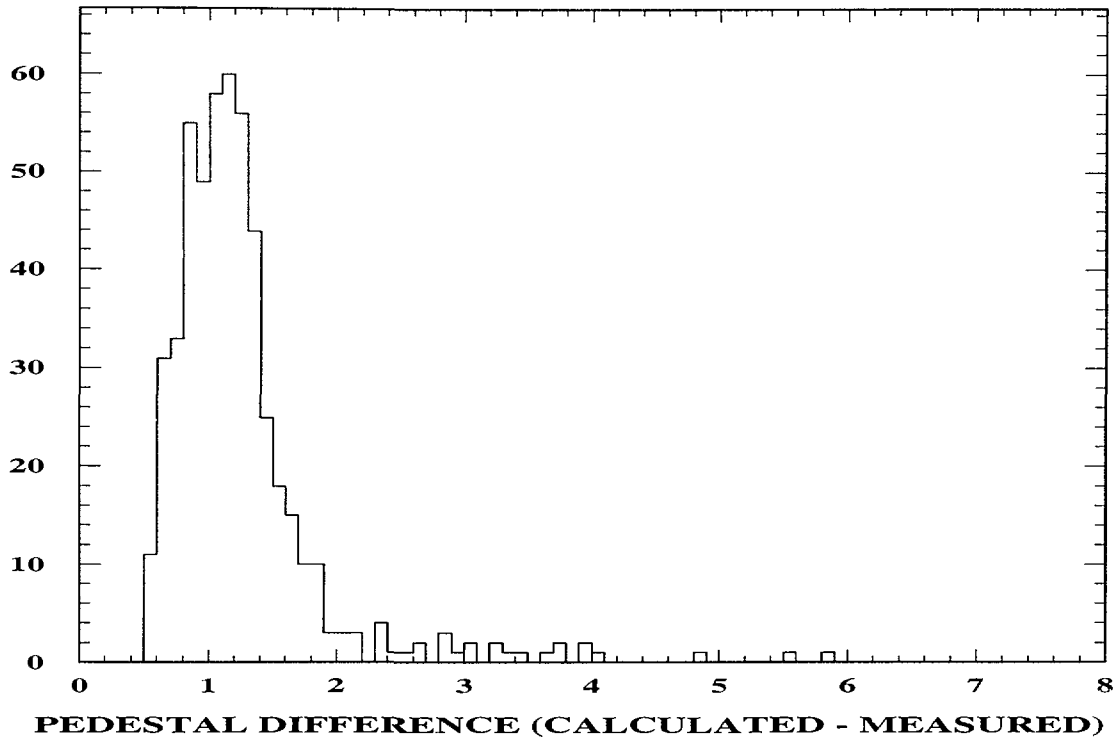


Figure 13

2.3.4 Gains

Due to the fact that the value of the test-line capacitor per GASSIPLEX module is difficult to determine, it is not possible to obtain a precise gain value. However, using reasonable assumptions, a gain of roughly 12 mV/fC is estimated and compares well with the manufacturer's specifications,

3. PCB

3.1 PLAC (Plan d'Alimentation et de Contrôle , Implanted Voltage Supplies and Control Signals)

The GAS64 modules are plugged into a printed circuit board (PCB). This board should allow the distribution of the low-level voltages required to drive the GASSIPLEX chips, allow the transit of control commands and provide the interface for the output analog levels from the detector to the ADC coders. A prototype PCB (PLAC) was designed with the aim of studying potential problems arising from the implantation method and possible voltage drops on the supply lines. The transit of low-level signals through the analog daisy chain and possible sources of cross-talk in the board were also investigated.

The prototype PLAC specifications are as follows:

- an overall surface of 100x34 cm^2
- double sided PCB
- FR4 PCB material
- thickness of the Cu layer = 17.8 μm

In designing the PLAC circuits, it became apparent that the surface available for implanting the control and analog signal lines was insufficient. This problem is due to a conflict between the high density of channels to be treated (and so requiring larger surfaces for the supporting circuitry) and the increased number of holes to be cut in the PCB to allow the feedthrough of signals from the detector. Consequently, a maximum of 4 GASSIPLEX chips were daisy-chained (GAS64) (to avoid the loss of too much information should one chain break down) and 30 circuit lines per column (in the high density zone) were implanted. Several solutions were envisaged for the ALICE2 PCB design:

- a multilayered board with a large surface area (100x40 cm^2). This solution required the use of thicker Cu (0.105 mm) and insulating (1.4 mm) layers, a condition imposed by the manufacturers. The resulting board is too thick for our needs and is also prohibitively expensive as it is a non-standard design.

- a multilayered board with an intermediate surface area (50x50 cm^2). This leads to a board of acceptable thickness (70 μm Cu and 0.9 mm FR4) but would require too many delicate inter-connections between individual boards. The price range is also too high due to numerous steps required in the manufacturing process.

- double sided PCB with mixed inter-connection printed circuit-cables. This entails the soldering of micro (or pico) cables directly onto the detector circuits. This would require complex mounting techniques that would be incompatible with the on-site construction and would also give unreliable results.

- double sided PCB with micro (or pico) cables interfaced with connectors. This solution would lead to a large amount of extra material being used and is therefore unsuitable. The cost of a large number of connectors also puts this solution outwith our price range.

In order to minimise the number of implanted tracks, it was decided that all information should be treated locally on the detector and the final PCB was designed with this in mind.

Voltage distribution and evaluation of the track width.

- voltage supply: 3.5V
- current on the track: 3.15 A
- track resistance ≤ 0.022 Ω
- track length: 100 cm
- conductor temperature: 35^0C

Using the UTEC 93.703 standard, the track width *l* can be evaluated as a function of *f*, *e* and *r*. Taking e= 17 μm (track thickness) and r= 0.3 mΩ/10 mm, the standard curves give a track width of 15 mm + 20% that is, 18 mm . We assume a maximal width of 20 mm for the longest voltage supply rails.

Signal organization and line adaptation
Given the surface available for these lines and the engraving specifications (chosen by the manufacturer), these rails are fixed at a width of 0.3 mm. With an insulator 0.37 mm thick, the impedance, Z_0 of a track is 60 Ω. The sortance of the CMOS buffers do not allow line adaptation under low impedance given the signal pulse rise times (~20ns) and length of the rails. The choice was therefore not to adapt the T/H and clear lines and restrict the number of GAS64 modules to 8 per T/H line. The clock lines are adapted by an RC circuit and the CAL_IN (test) lines are adapted to 50 Ω.

3.2 ALICE 2 PCB

This prototype was constructed for ¼ of the TC1 tracking chamber. The radius is of 915 mm and constitutes an active surface of 0,63m^2 per plane. In order to find a happy medium between the amount of work required for this development and the available time, it was decided that only one of the two active cathodes would be fully implemented. The cathode plane is composed of three different geometrical zones where pads are of: 5x7.5 mm^2, 5x15 mm^2, 5x30 mm^2. This leads to a total of 9866 elementary channels. Output signals are regrouped into packets of 64 (with a few exceptions) and are accessed via 9 cm long kapton cables.

The PCB has the 155 sockets required for the GAS64 plug-in modules, the rails necessary for the voltage supplies, control signals and output analog signals. The total PCB thickness is 0.4 mm with 17.5 µm copper rails, and 3 PCB boards were required to cover the whole detector surface (indicated by the dashed lines in figure n^0 14).

In order to study the most conservative solution, where the output analog signals are coded by C-RAMS ADC's at a distance, 8 GAS64 modules were daisy-chained (that is 512 channels per ouput line). The GAS64 modules are symbolically represented by grey shaded rectangles in figure n^0 14. The arrow heads show the positions of the analog read-out buffers.

The implanted line widths and lengths were deduced from the PLAC tests as were the line adaptator requirements and expected loads.

The more adventurous (and reasonable) solution of coding locally was also tested using the same PCB. The interconnection of the NULOC and INV modules was done through flat cables

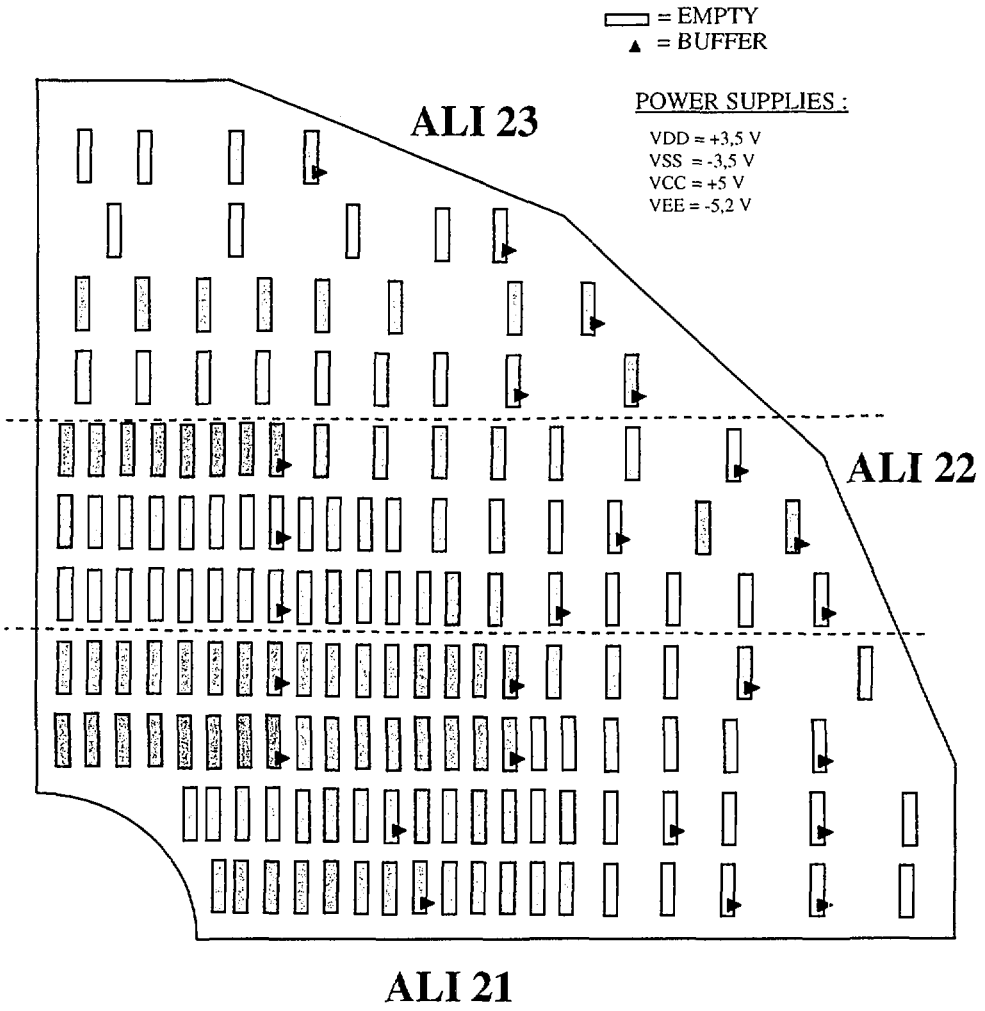


Figure 14

4. LOCAL DATA READOUT AND CODING SYSTEM

4.1 Introduction

In this version the data are digitized and analysed (pedestal subtraction and zero suppression) locally. Locally means directly on the back plane of the detector. Two electronic cards were realised for these tests : The NULOC card (NUmerisation LOCale) and the INV card (Interface Nuloc VME). The co-ordination of this ensemble was provided by a specially designed PATCH protocol (Protocol for Alice Tracking CHambers)(see appendix 2.1). During the data taking period this system was not fully tested due to lack of time. It has however been successfully tested in the laboratory.

4.2 Description of the data analysis chain.

The NULOC card is connected to socket P4 (see figure n^0 4) of the GAS64 module. In this card the output analog signals are coded on 12-bit ADC, pedestals are subtracted and zero suppression is carried out. These functions are implanted in an LCA module (see appendix 2.2 for further details).

The INV card provides two main functions :

- the control of the PATCH bus

- the interface to the serial port, SPAC

As can be seen in figure n^0 15, the INV card is composed of 3 parts :

- 1 DSP SHARC 21062 used for its interrupt and ALU functions. Use is also made of its fast serial port « link port »

- 1 CPLD (Complex Programmable Logic Device) that treats the SPAC communication protocol with the VME.

- 1 LCA that allows the formatting and interfacing of the DSP with the CPLD.

A detailed description of this card is given in Annex 3.

4.3 The PATCH protocol.

PATCH provides the protocol with which data from the NULOC modules are read (in slave mode) and uploads the parameters required for their numerical treatment. It co-ordinates a 2-way bus that operates on a Single Master- N-Slaves basis. This protocol was developed for the Link Port bus implanted in the ADSP2106 (Analog Devices). The user program can be written in machine code or C.
A detailed description of this protocol is given in Appendix 4

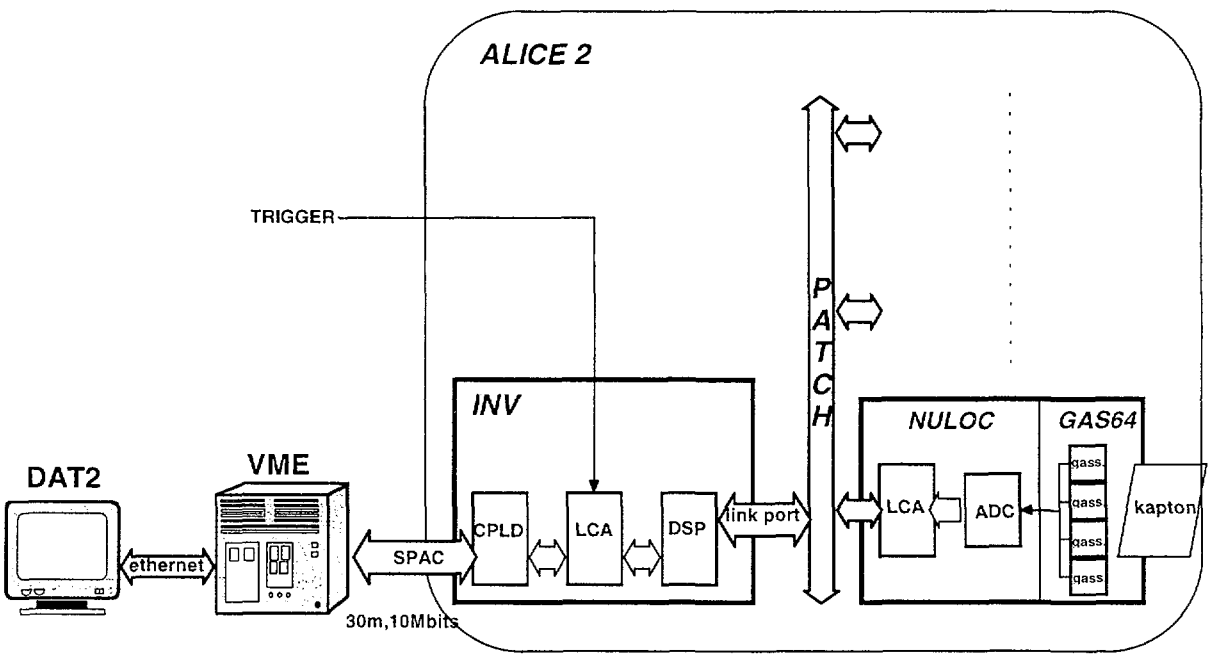


Figure 15. Chaîne de traitement

5. Data Acquisition System (DAQ) for the ALICE Prototype tests

5.1 General DAQ Architecture

The basic DAQ architecture is based on high-speed parallel network links. These links connect the data sources to their destinations via a switching network. Such a highly parallel architecture allows greater flexibility and modularity. This system is described in detail in the ALICE Technical Proposal.

ALICE DAQ Architecture

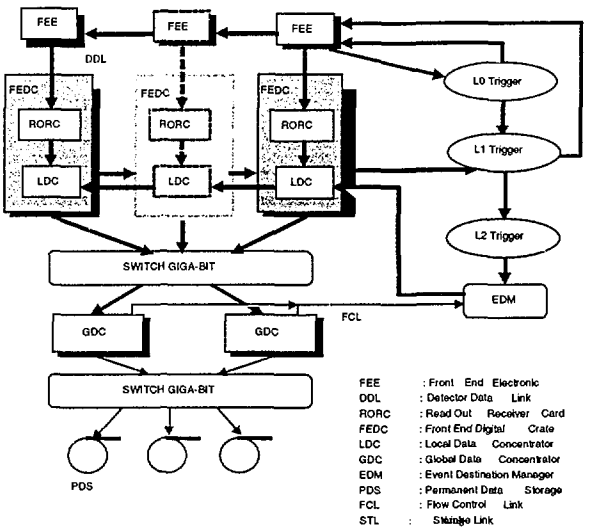


Figure 16

5.2 The DATE Software Package.

DATE is a software package that allows data acquisition within a distributed multiprocessor environment. Figure n^{0}17 gives a schematical view of the Run Control and LDC architectures.

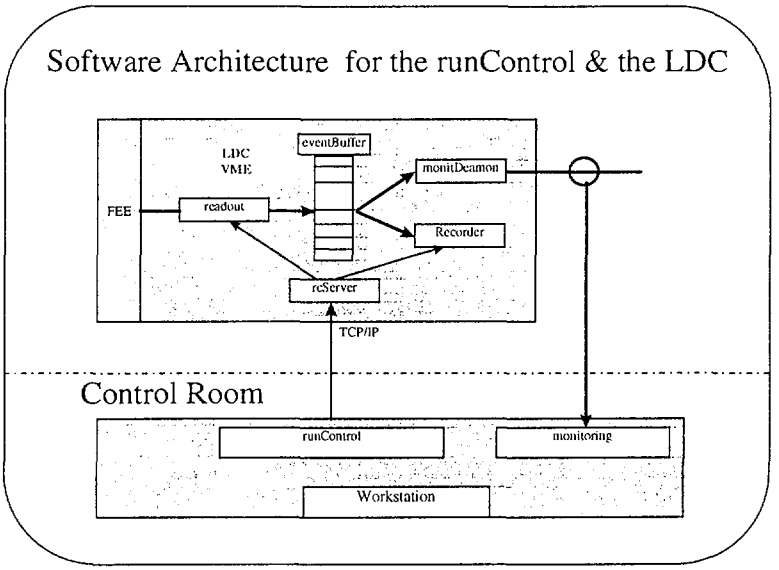


Figure 17

The main DATE functions may be resumed as follows :

- Programmation and read-out of the front-end electronics
- Event monitoring
- Run control
- Data reading
- View of the run status
- Run Book keeping

The Readout system

This is carried out in each LDC and goes through the following phases :

1. Waits for activation by the trigger
2. Reads out the front-end electronics (FEE)
3. Fills a circular buffer with the data

The FEE is programmable via the read List function and is under the control of the user. The ***read List*** is inserted into the ***readout*** architecture. The ***read List*** used in a recent experiment is given :

Event Structure (file ***event.h***)

```
struct eventHeaderStruct {
  long  size;                   /* size of event in Bytes  */
  unsigned long  magic;         /* magic number used for consistency check */
  unsigned long  type;          /* event type */
  unsigned long  headLen;       /* size of header in bytes */
  unsigned long  runNb;         /* run number */
  unsigned long  burstNb;       /* burst number */
  unsigned long  nbInRun;       /* event number in run */
```

```
  unsigned long  nbInBurst;       /* event number in burst */
  unsigned long  triggerNb;       /* trigger number for this detector */
  unsigned long  fileSeqNb;       /* File sequence number for multifiles run */
  detectorIdType detectorId[MASK_LENGTH];   /* detector identification */
  unsigned long  time;            /* Time in seconds since 0.00 GMT 1.1.1970 */
  unsigned long  usec;            /* microseconds */
  unsigned long  errorCode;
  unsigned long  deadTime;
  unsigned long  deadTimeusec;
};

struct eventStruct {
   struct eventHeaderStruct eventHeader;
   unsigned short rawData[1];
};
```

Event Monitoring An analysis program can ask for events to be provided from any of the authorised network computers. On the LDC a daemon named ***mpDeamon*** provides this function.

Run control. The control is ensured by the ***runControl*** process. This is a centralised process which connects all the processors used by the DAQ and which in turn, runs a daemon called ***rcServer***. The graphics for the run control is written in tcl-tk.

Data recording. A process called ***recorder*** empties the circular buffer that was filled by the ***readout*** process. The ***recorder*** sends the data to a TCP/IP socket.

View of the Run status. All DAQ processes can have output messages depending on their status. One processor is designated to receive these messages. The ***infoDeamon*** runs on this machine.

Run Book Keeping. The ***bookkeeping*** process allows all run information to be saved to hard disk. A program called ***statsBrowser*** allows the interactive exploitation of these files.

5.3 DAQ implementation during the test beams

Figure n^0 18 shows the schematical layout of the test-beam acquisition.

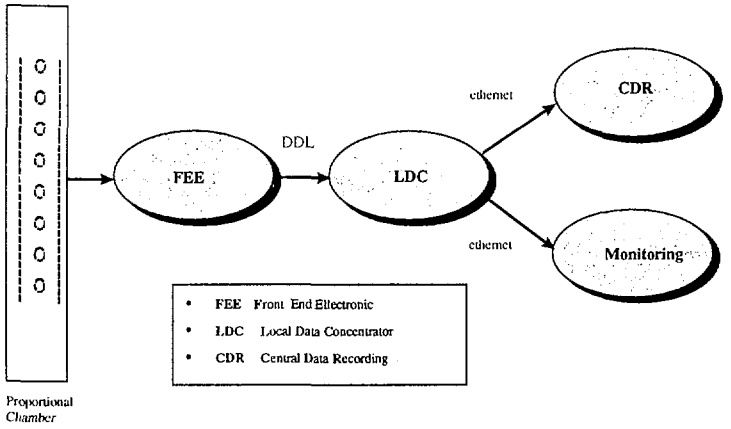


Figure 18: schematical layout

The detector prototype is described in details in chapter 3.2. Here we recall the relevant DAQ information as being the 9866 elementary channels to be readout.

In the following the relevant information for the coding methods are given.

1. **Acquisition with digitisation in a VME.** The multiplexed analog signals are input to the C-RAM ADC's in the VME (CAEN V550). Sequencing of the data is provided by the CAEN V551 VME module.

   Caen V550 : 2 blocks with 2048 channels input. Coding on a 10-bit ADC with a 200ns conversion time. Pedestal subtraction and threshold functions are used.

   Caen V551 :provides the clock for the GASSIPLEX sequencing at a frequency chosen between 0.5 and 5 MHz.

The layout of the electronic crates and network links is given in figure n^0 19.

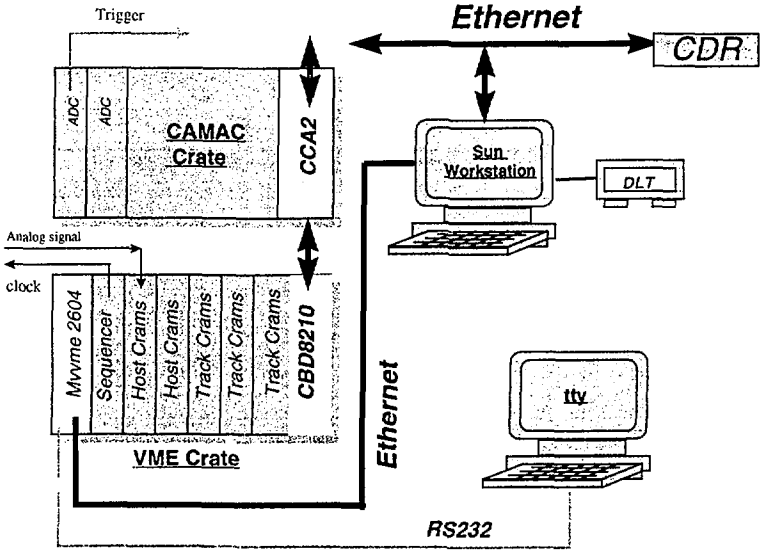


Figure 19:

In this experiment a total of 4 C-RAMS modules were used where :

5 blocks were dedicated to the 768 channels tracking system
2 blocks of 768 channels were used for the chamber prototype

The readout + dead time was 1.4 ms. A scintillator telescope was used for the trigger logic that provided a LAM on a CAMAC ADC.

2. Acquisition with Local Digitization

The general layout of this system is shown in figure n^0 20 . In this case the digitization is realised in the FEE by the NULOC card.

The NULOC functions :

- Buffering
- Digitization (12-bit ADC), 700 ns per channel
- Pedestal subtraction, threshold levels, zero suppression
- 1 Nuloc for 64 channels
- Data transfer through a link port on the DSP

The DSP functions :

- NULOC data readout
- Data compression

The FEE<->LDC communication

The connection between these two parts is realised through a SPAC module that was developed for this purpose by the LAL, Orsay. This module allows a serial transmission of 10 Mbits/s between a master and slave module. This is a temporary solution and will be replaced by the DDL modules (SIU-DIU) developed at CERN for the ALICE acquisition system.

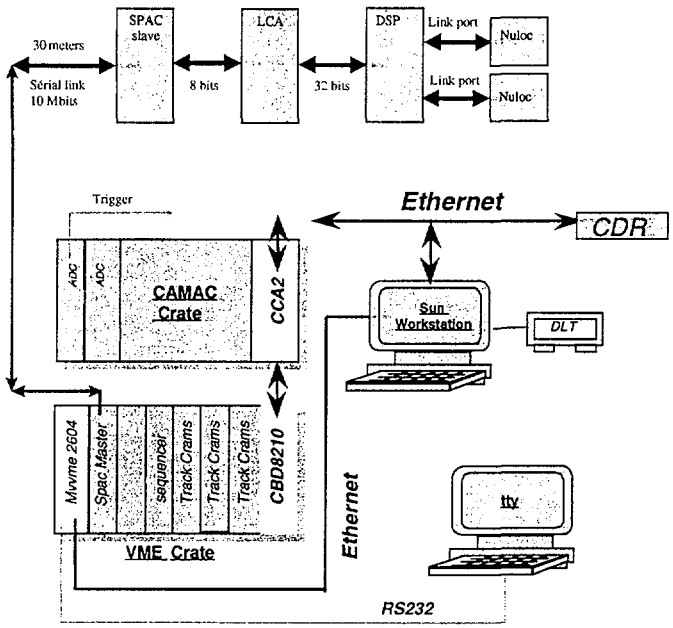


Figure 20:

SOFTWARE PACKAGES USED FOR THE PROTOTYPE TESTS

Calculation of the pedestal values

The ***cramsped*** program evaluates the average pedestal value from N measurements for each channel. This program gives 2 output files

1. a histogram file that can be studied with ***PAW***
2. a parameter file, ***crams.ped***, that is uploaded to the FEE at the beginning of the next run. This file contains the pedestal values to be subtracted on-line.

The acquisition routines

There are 4 main routines :

1. ***armHw()*** which ensures the initialisation of the FEE.
2. ***eventArrived()*** which returns a non-zero value when there is an event to be read out. This routine works on a ***polling*** basis on the ADC that gives the trigger LAM.
3. ***readEvent()*** reads the individual coded channels and constructs the event.
4. ***disArmHw()*** realises the end of the procedure

Data concerning the experimental configuration is written in the ***config.dat*** file.

Start/End of Run utilities

At the beginning or end of a run it is possible to execute script files or programs.

Start of Run:

1. ***SOR.commands*** contains the script commands to be executed
2. ***SOR.files*** contains executable programs

End of Run

1. ***EOR.commands*** contains the script commands to be executed
2. ***EOR.files*** contains executable programs

The monitoring software

This package is written in FORTRAN and uses the libraries that allow events to be obtained from any authorised networked machine. The graphical display uses the HIGZ package via the PAW libraries. In the near future the on-line graphical display will be provided the object oriented (OO) ROOT package.

Run control configuration

The run control process is configured via the parameter written in the ***runControl.config*** [1] file.

The HPSS Data recording package

The CERN HPSS package was installed on the acquisition machine and assumed the task of transferring the data files to the Central Data Recording System. This package is automatically activated at the end of a run and so the local disk is merely used as an intermediate buffer.

Utilities

eventDump() allows the visualisation of the content of an event

tarraw() provides the commands for saving data to a DLT.

[1] See the DATE v3 User's Guide [8]

6. NEAR FUTURE

6.1 A Multi Chip Module (MCM)

A feasibility study for the manufacturing of an MCM prototype is in progress. The main aims are to verify the mechanical qualities (eg. planarity) and thermal aspects of such a module and to see if such a module can be reliably made by local industries.

The circuit design is the same as that used for the GAS64 and NULOC modules that have already been described in appendix 1 and 2.2. It is important to note that the overall circuit characteristics (speed, power consumption, etc...) do not correspond to the definitive version as they are strongly dependent on the choice of the individual components available on today's market.

With the exception of the input protections, this MCM will fulfill all the definitive functions, the analog signal treatment and the numerical digitization.

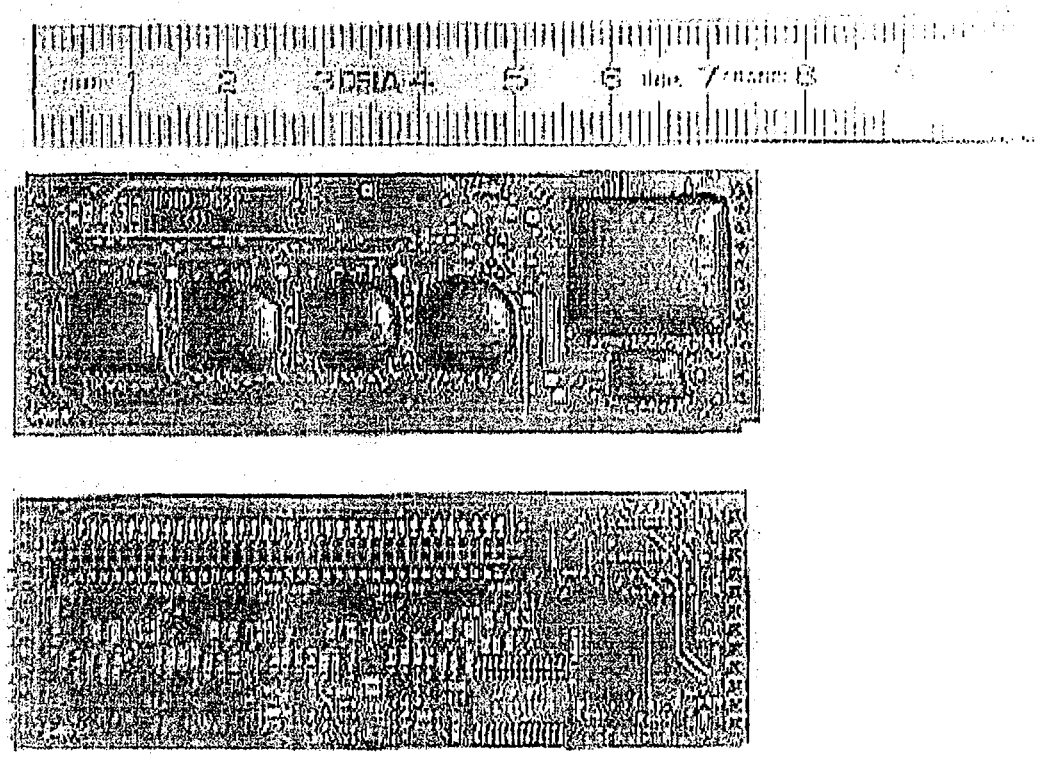
On this prototype the LCA (Logical Cell Array) will be programmable in order to optimize the logic architecture that deals with the digitization.

All parameters for threshold levels, pedestal values and channel identification numbers will be uploaded via the 2-way DSP Serial Link Port.

MCM specifications :

- surface dimensions 27x75 mm^2
- PCB thickness 0.5 mm
- insulating layer FR4
- cabling technology : wire bonding on one side and CMS on the other
- radiation lengths:
  - -PCB: 0.166%
  - components: 0.13%
  - total : 0.3%
- power consumption 13 mW/voie
- notation for active components:

- 4 GASSIPLEX 1.5 µm	die	CERN
- 1 LCA XC4010	die	XILINK
- 1 driver 54 ABT16245	die	Texas Instruments
- 1 buffer LT 1360	SMT	Linear Technology
- 1 ADC LTC14156	SMT	Linear Technology
- 2 TMM.112.03.SS connectors		SAMTEC
- 1 SFM. 135.L2.S.D connector		SAMTEC



Upgrade of the MCM specifications

The realisation of a second prototype is foreseen for the end of 1999 with the following upgrades :

- the 0.7 μm GASSIPLEX will be implanted
- a new coder that runs at 2.5 MHz will be used with no noteable increase in the power consumption
- the use of a 32 MHz clock implanted in the LCA should allow coded data to be extracted in under 50 μs. The comprimise between the speed and power consumption will be made following the physics requirements.
- the handling of the CLOCK-IN for the GASSIPLEX chips will be individualised and controlled by the coding sequencer on the LCA. This will minimise potential problems related to long analog chains and will allow a greater modularity in the number of analog channels to be treated (32, 48 or 64). This last option implies that if, for a given geometry, only 32 channels are required, then the other 32 GASSIPLEX channels will not be cabled-up. In this case the 70 pin connector will be replaced by a smaller 35 pin connector.

6.2 Realisation of an MCM

In order to construct this MCM an investigation of the available technologies was necessary. The procedure for this was as follows :

- construction of the MCM specifications with a certain degree of liberty but also several strong constraints.
- the creation of a list of prospective MCM manufacturers in France and abroad
- the presentation of the specifications to 15 of these companies
- a meeting with interested companies to discuss the diverse production techniques possible and a factory visit with specialists in order to evaluate the available facilities.

Ten companies declared an interest in this project, and ranged from well-known groups such as IBM, BULL, DASSAULT, MATRA, THOMSON to smaller industrial enterprises. It is worth pointing out that some of the American industries recommended several of the French groups as being more competent in this domain.

These meetings resulted in several technical propositions with a very wide range of cost estimates ! This allowed to see a panorama of the different MCM solutions proposed on today's market.

The technical proposals :

All the companies converged on a MCM-L realisation, ie. on a printed circuit board support. The other possibility, which was unanimously rejected, was the MCM-C which used a ceramic support. This was seen by all as being too expensive and would lead to a resulting thickness that would not be within the specification limits.

Several MCM-L propositions were made and vary depending on the manufacturer's know-how :

- the use of SMT components and wire bonding (die directly bonded on to the support).

- TAB and SMT

- TAB, SMT and wire bonding

- wire bonding on support connected via BGA on support and SMT.

Finally the first solution was retained as it presents several advantages, namely, it is :

- easy to realise

- is in keeping with all the specifications

- is affordable in terms of cost/channel

- is well adapted to the testing process and allows easy access to the GASSIPLEX chips.

Concerning the choice of the company for the prototype manufacturing, the cost estimate was naturally the determining factor after all technical conditions had been fulfilled. Certain technical processes are only available in the larger enterprises as the specialised techniques are also expensive. Even though MATRA and THOMSON made excellent propositions, the HCM company (from La Rochelle- France) was chosen. This company is specialised, since 1980, in the treatment and points testing under of micro-chips. More recently, it is specialised in MCM-L and C technology. An added bonus is that HCM is able to encapsulate the implanted GASSIPLEX chips.

Ten prototypes are currently under construction.

Definitive solution.

The MCM's will be implanted on the outer PCB layer of the detector. This PCB will provide the voltage distributions, the T/H and CAL_IN rails, the readout bus and 3 rails to allow the download of values of the LCA if so required. The MCM readout will be via the Link Port of a DSP. 6 DSP's will be sufficient for the readout of one side of a chamber ie. 40,000 elementary channels in the case of station 1.

Two electronic cards, each containing 6 DSP modules will be used in the data read-out system. One card will be placed at the top outer edge of the detector, and the other at the lower edge (see figure n^{0}21). One set of DSP's will read-out a semi-circular area on each side of the detector. In this way the GASSIPLEX to DSP distances are minimised, and the full detector can be read-out on 12 DSP's. With this architecture 2 DDL's are required per detector. A supplementary feature of the DSP is that data can be stored in temporary buffers that in turn can be read-out at the desired rate.

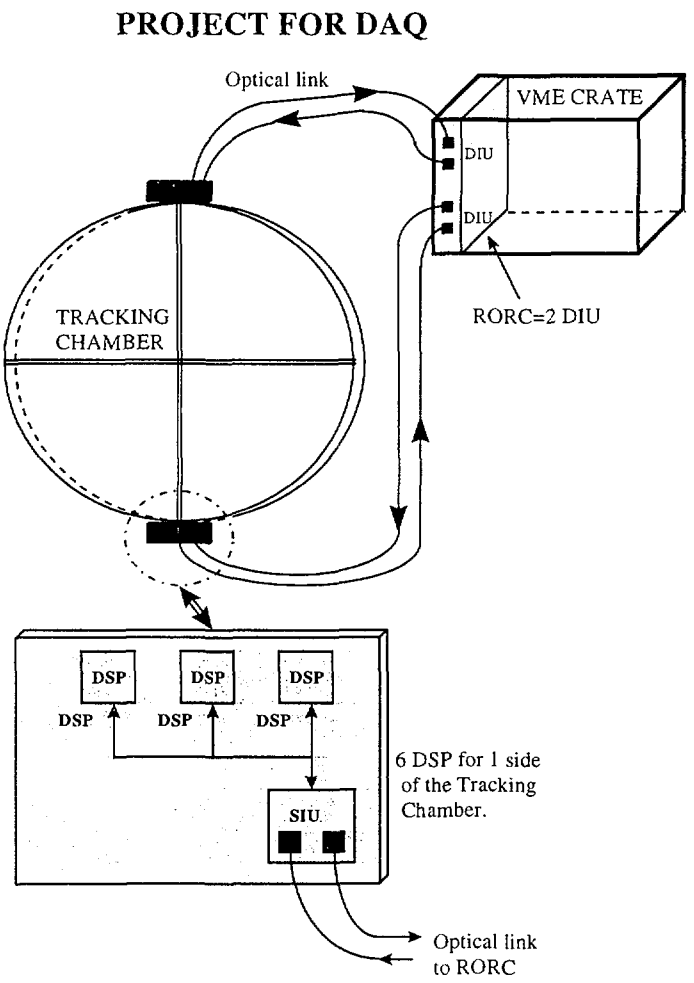


Figure 21:

APPENDIX 1

Two types of wiring were used to allow the analog output to be treated by either the C-RAMS coders or the NULOC card. Details of the wiring will be discussed in the following text and in appendix 2.2.

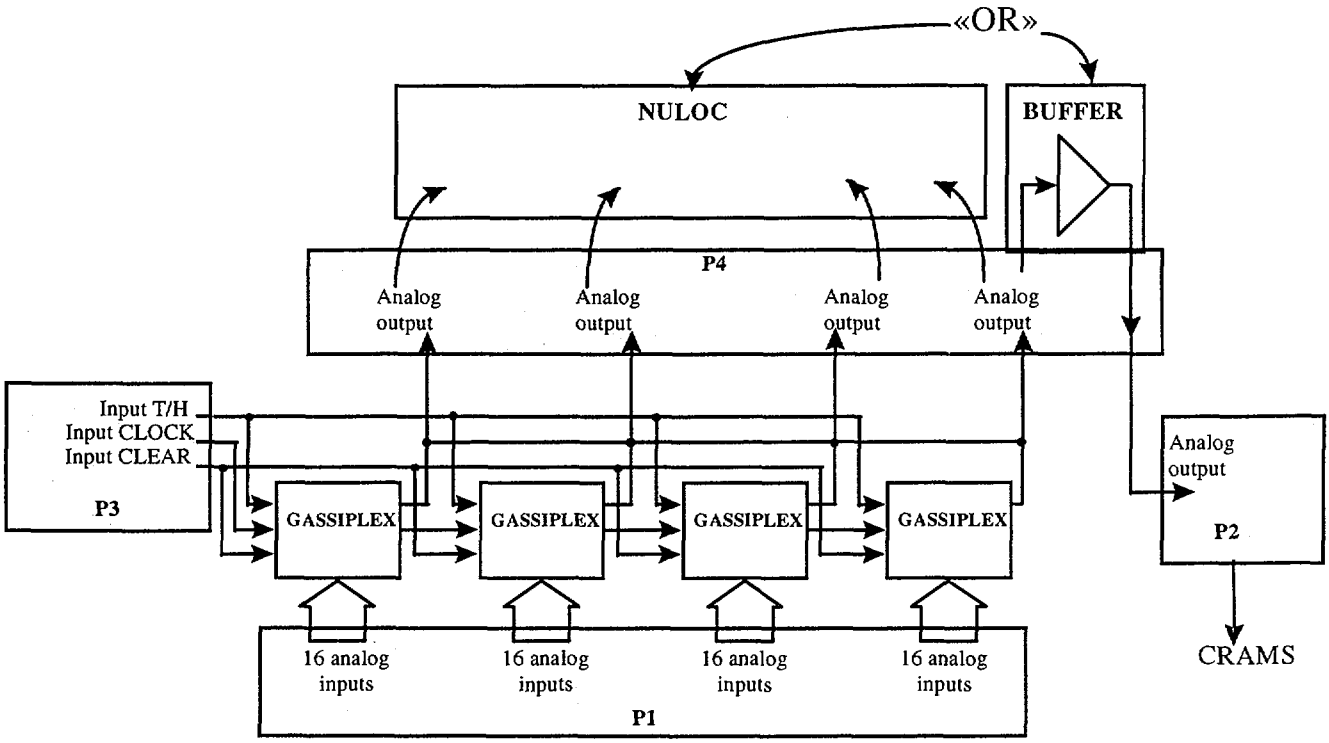
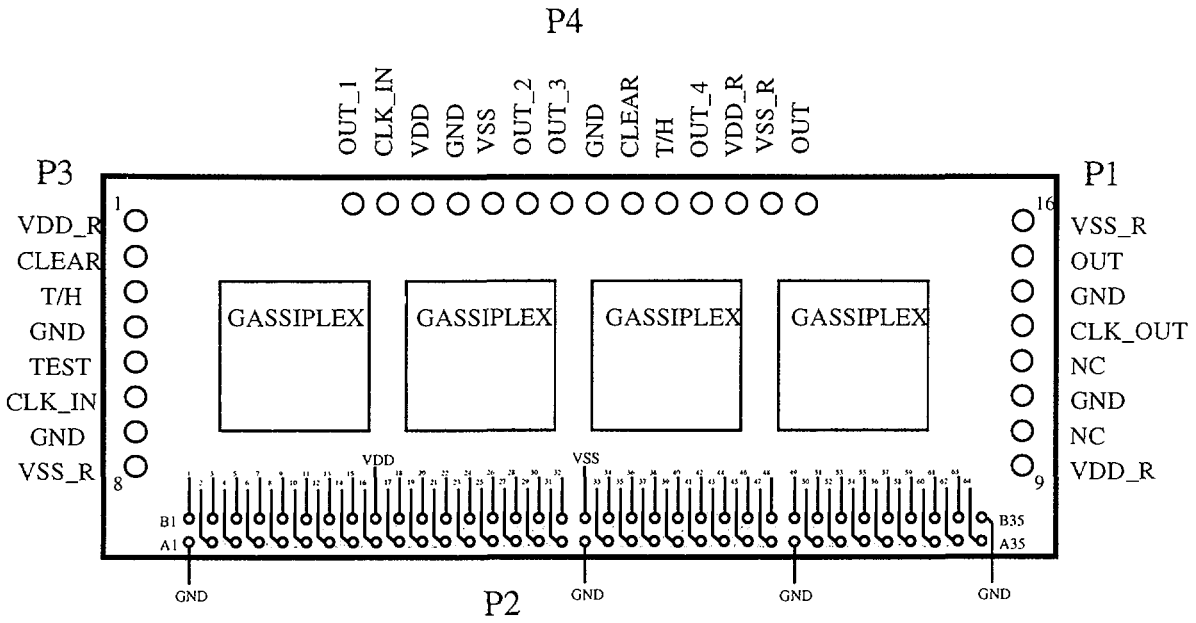


Figure 22:

The general layout showing the NULOC and C-RAMS options is shown in figure n^0 22. Details describing the attributions of the GAS64 connections are given in figure n^0 23. The overall circuit dimensions are 25x75 mm^2 and is composed of 0.4 mm FR4 with 4 Cu layers , each 17 μm thick. In order to see if the overall board thickness could be reduced, some circuits contained a ground plane based on a grid structure. This technique reduces the quantity of Cu used in the ground plane by 40% and produces no noteable effect on the experimental noise levels.

VIEW OF TOP SIDE



NC= non connected

Figure 23:

CONNECTORS P2 & P3

Inputs :

CLEAR = GASSIPLEX clearing. High level 0V, low level -3.5V. Works on an active high level. Width= 200 ns.

T /H = Track/Hold. High level +3.5V, low level -3.5V. Hold works on an active low level. Signal width is variable and is closen as a function of the number of read-out channels.

CLK_IN = Clock signal for multiplexing the 64 channels of one GAS64 module. High level = 0V, low level -3.5V. Works on an active high level. Signal width variable from 50 to 500 ns.

TEST = square analog signal.

Outputs :

OUT = multiplexed analog output.

CLK_OUT = Clock signal after its transit through the GAS64 module.

CONNECTOR P4

Inputs :

-Signals coming from the NULOC card and going to the GAS64 module.

CLEAR = same as for P2 and P3.

CLK_IN = as above (see connectors P2&P3)

-Signals coming from the analog buffer and going to the GAS64.

OUT = analog buffer output.

Outputs :

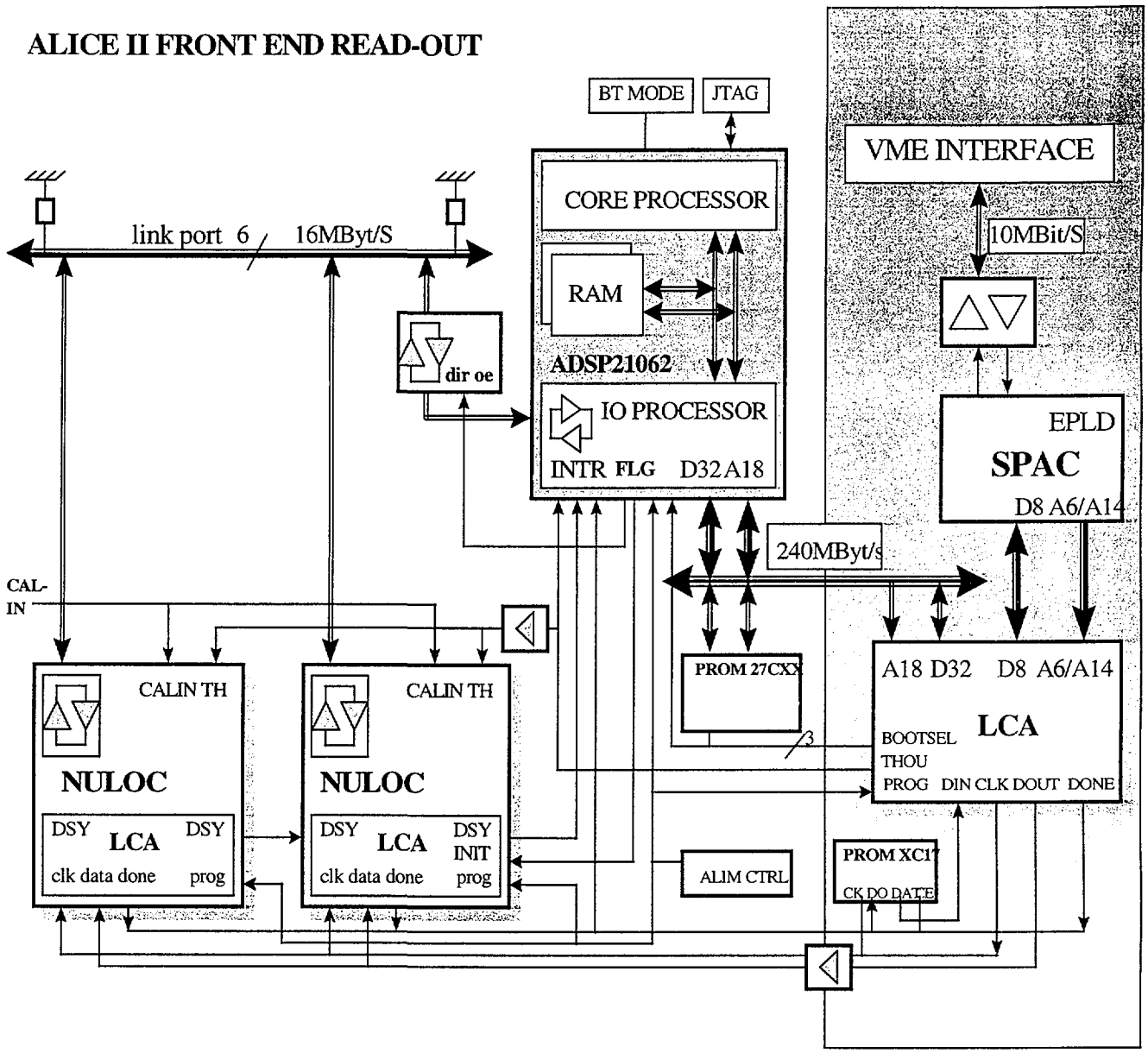
OUT_1 = multiplexed analog output of the 1st GASSIPLEX chip.
OUT_2 = multiplexed analog output of the 2nd GASSIPLEX chip.
OUT_3 = multiplexed analog output of the 3rd GASSIPLEX chip.
OUT_4 = multiplexed analog output of the 4th GASSIPLEX chip.
OUT = summed analog output to the NULOC card or the analog buffer.

VOLTAGE SUPPLIES: The card voltage supplies are provided via the 8 pin connectors, on pin VDD_R and VSS_R. On the 14 pin connector, connectors VDD_R and VDD are strapped, as are VSS_R and VSS. If a non-negligible voltage drop* is observed on VDD_R et VSS_R, it is possible to include a voltage regulator on the 14 pin connector. This should be done between pins VDD_R / VDD and VSS_R / VSS respectively. It is only necessary to connect pins VDD_R and VSS_R to the external voltage supplies.

* Voltage loss can be significant over longer track lengths.

VDD_R = +3,5V
VSS_R = -3,5V
GND = 0V

APPENDIX2.1


ALICE II FRONT END READ-OUT
BT MODE
JTAG
VME INTERFACE
CORE PROCESSOR
RAM
ADSP21062
IO PROCESSOR
INTR FLG D32 A18
link port 6
16MByt/S
dir oe
10MBit/S
EPLD
SPAC
D8 A6/A14
240MByt/s
CAL-
IN
CALIN TH
NULOC
DSY
LCA
DSY
clk data done
prog
INIT
PROM 27CXX
A18 D32 D8 A6/A14
LCA
BOOTSEL
THOU
PROG DIN CLK DOUT DONE
ALIM CTRL
PROM XC1
CK DO DATE

APPENDIX 2.2

The NULOC daughter card

Functions:

This daughter card was realised in order to test the idea of local digitization (NUmérisation LOCale) and data transfer on the detector. It plugs in directly to the GAS64 modules.

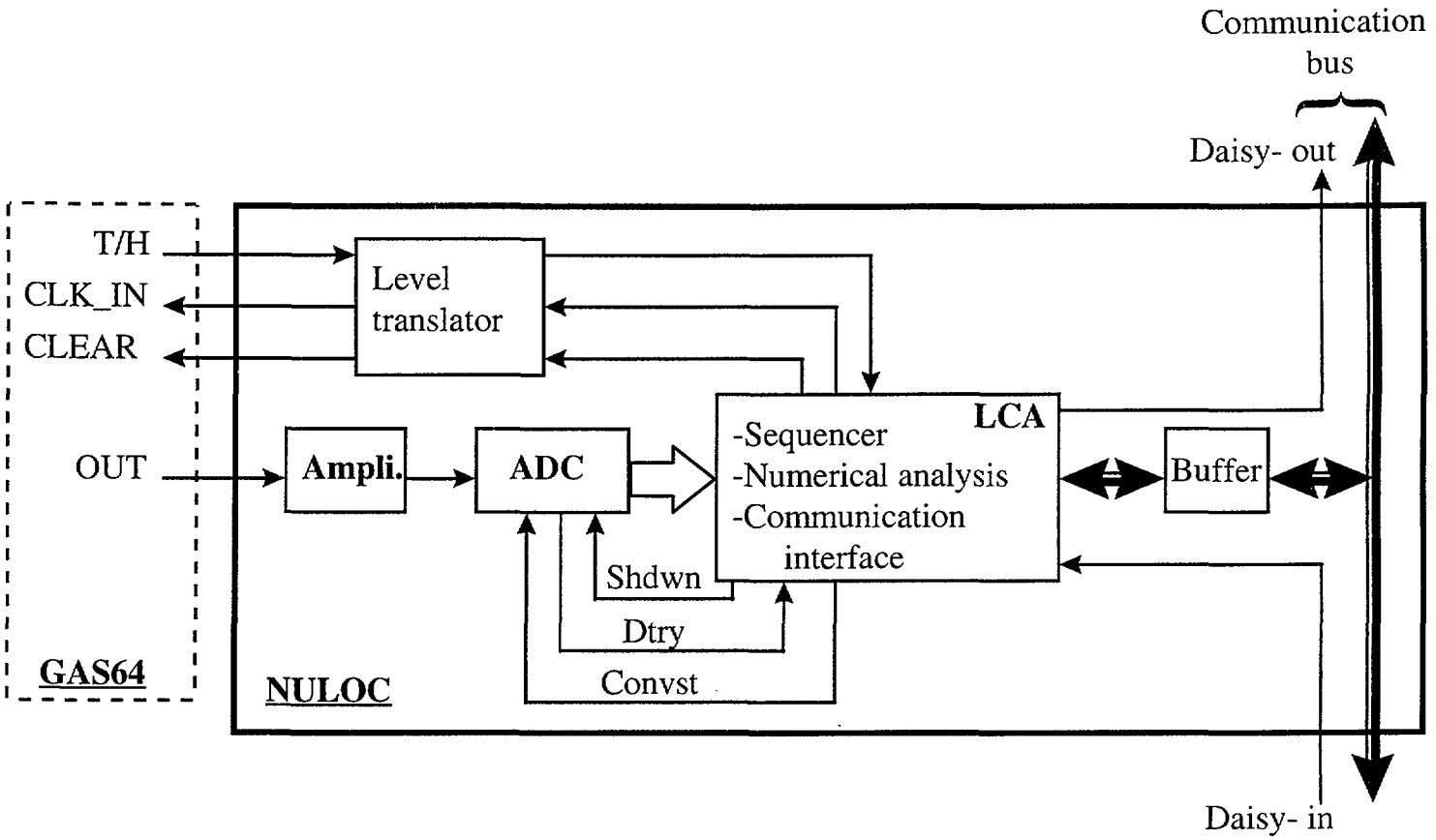


Figure 24:

A digitization cycle starts on the doward going edge of the T/H signal. The GASSIPLEX chips go into HOLD mode. The NULOC sequencer generates a CLK_IN signal that is sent to the GAS64 module. The multiplexed analog outputs arrive in phase with the CLK_OUT signal. The first channel that receives the CLK_IN will be the first channel present at the multiplexed output. The output signal is already adapted to the ADC input through the impedance characteristics of the filtering amplifier.

After stabilization of the analog signal, the sequencer starts the conversion cycle (Convst signal). At the end of this cycle a "Data Ready" (Dtry) signal is generated by the ADC and informs the sequencer that the data are now available for transfer. To resume, the coding sequence is as follows:
A CLK_IN is generated after every DTRY signal. Next, a CONVST signal is sent to the ADC. This is repeated another 63 times. On the rising front of the T/H signal the GASSIPLEX are put into TRACK mode and the sequencer generates a CLEAR signal for the GASSIPLEX modules.
This scheme corresponds to the coding and numerical treatment for the 64 channels of one GAS64 module. The data transfer to the acquisition system is carried out via the communication bus.

The numerical treatment and communication bus are described in detail in appendix 4.

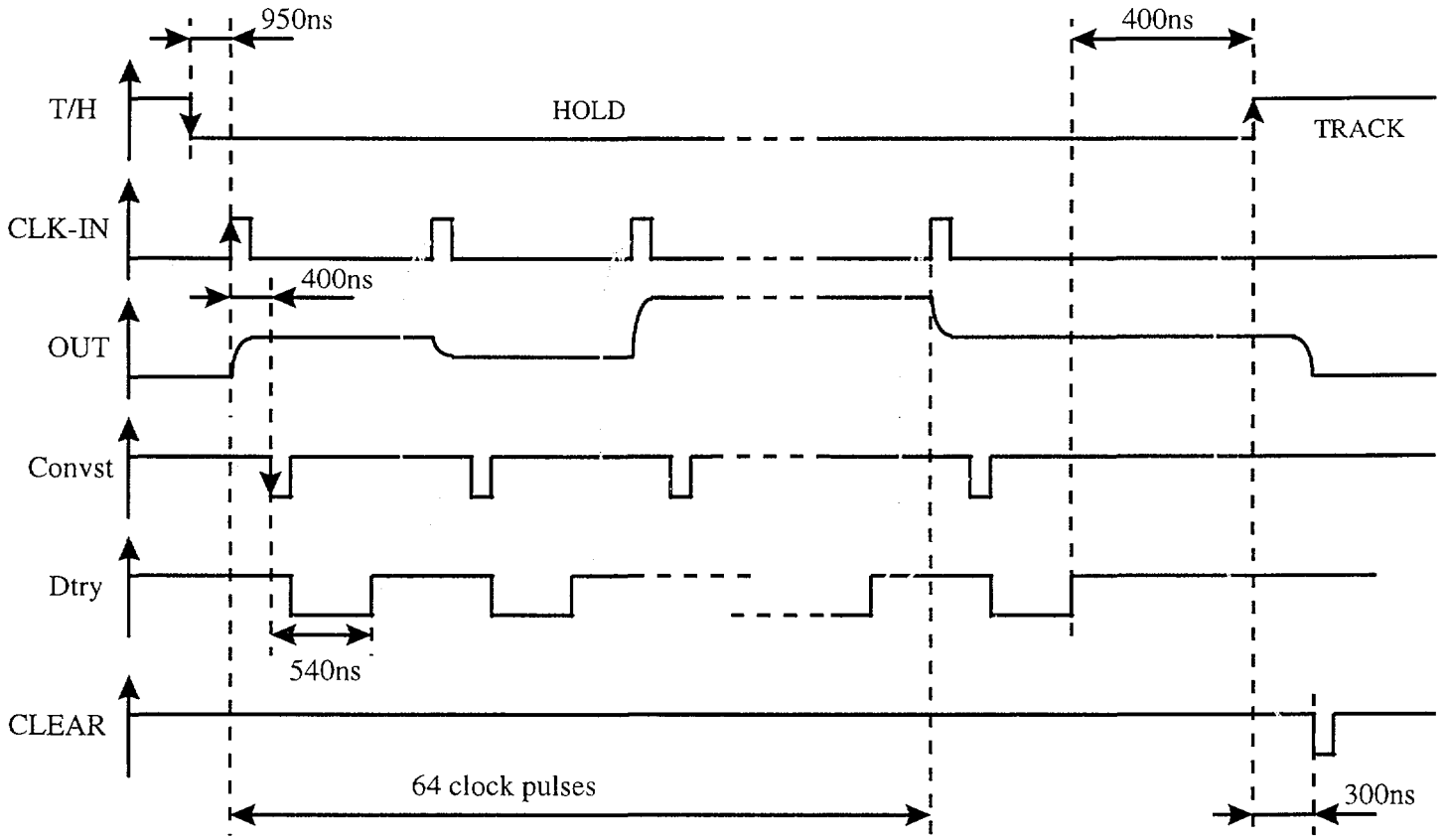


Figure 25:

Some important points concerning the overall scheme could be noted, namely:

- the DTRY signal received at the end of a complete coding cycle is used to start a new cycle. This implies that the time taken for a coding sequence is directly tied to the working rate of the ADC.

- a "shutdown" signal (SHDWN) allows the ADC to be put into a resting mode. This limits the power consumption outwith the coding periods.

- there is no external reference level required for the ADC, it uses its own internal 4096mV level.

- the clock pulses required for the NULOC card are provided via an internal oscillator implanted in the LCA circuitry. This avoids to use of an external high rate clock that could have interferd with the other signals.

Several logical signal translations are required in order to render the GASSIPLEX chips and the LCA circuits compatible. They are as follows:

CLEAR (LCA) => CLEAR (Gassiplex)
TTL => 0V / -3,5V
CLK-IN (LCA) => CLK-IN (Gassiplex)
TTL => 0V / -3,5V
T/H (LCA) <= T/H (Gassiplex)
TTL <= +3,5V / -3,5V

Implanted Technology:

- Amplifier: reference LT1360 by Linear Technology ; SMT encapsulation: SO8.
- ADC : reference LTC1415 by Linear Technology ; SMT encapsulation: SO24. Conversion time = 700 ns, precision 12 bits. Parallel data outputs.
- Sequencer : allows numerical treatment and provides the communication interface. Integrated in the LCA, reference XC4010E by XILINX, SMT encapsulation: PLCC84.
- The +5V voltage supply is provided via the communication bus.

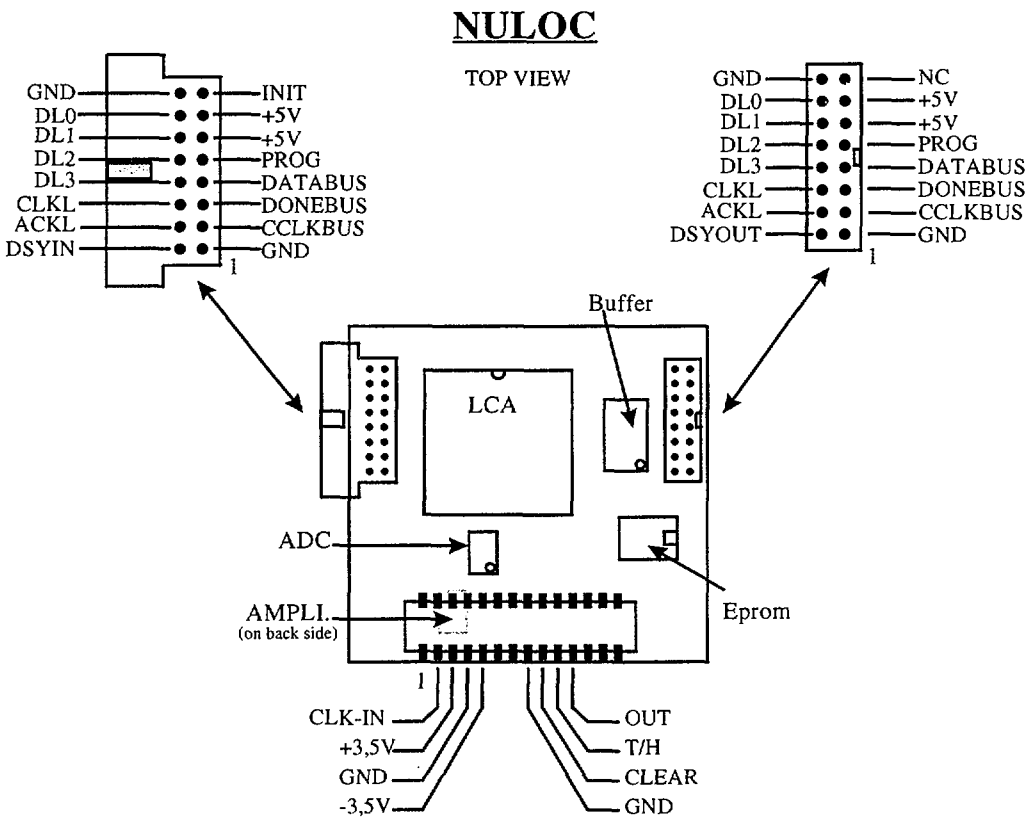


Figure 26:

APPENDIX 3

The Nuloc-VME Interface (INV)

This electronics card fulfills two functions:

- the control of the PATCH bus.
- provides the interface to the SPAC serial link.

Description: The «INV» card is comprised of 3 main components:

1- a «**DSP**»: le SHARC 21062 is used for:

- its micro-controller functions (interrupts, ALU) and dispose of enough RAM (2Mbits) to allow temporary data storage.

- its 2-way «**Link Port**» provides a fast synchronous serial link to the NULOC cards. (speed foreseen = 32 MHz).

2- a «CPLD» (Complex Programmable Logic Device): this provides the communication protocol with the VME. We have used the SPAC protocol (developed at LAL, Orsay) which allows a transmission rate of 10 Mbits/s over distances of 30 m or more.

3- a «LCA» (Logical Cell Array). This provides the DSP-CPLD interface and completes the card's logical functions.

The INV card layout is schematised in figure n^0 27

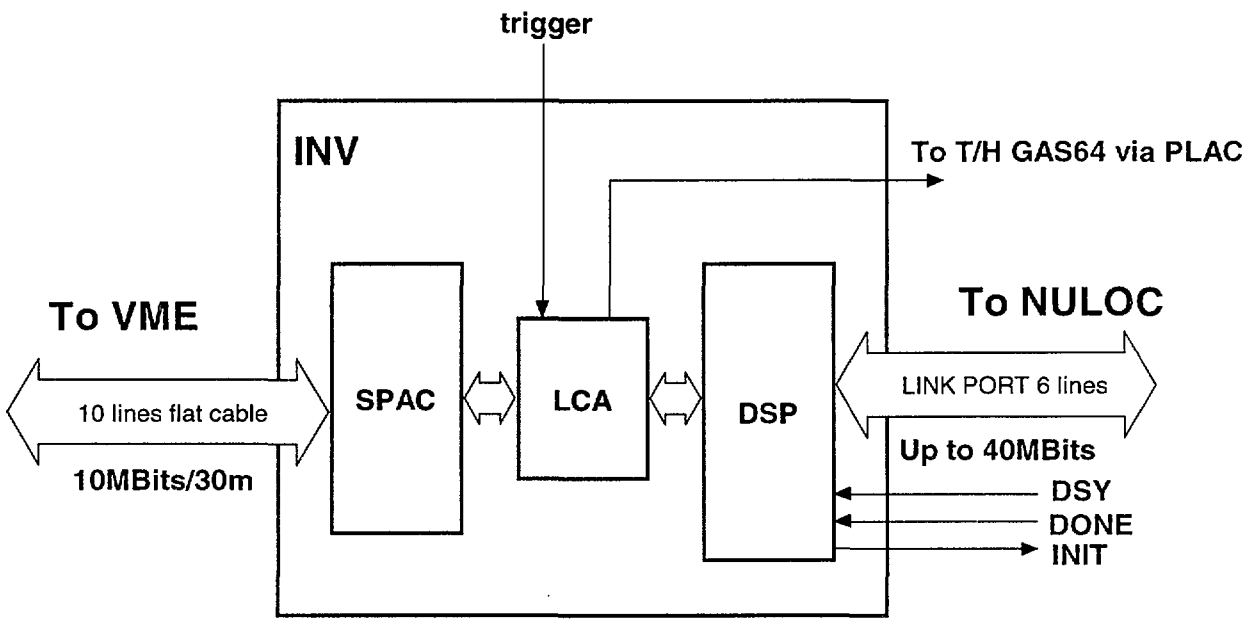


Figure 27: layout INV

Working modes:

The PATCH Master Control:

The master control allows the use of the 3 PATCH protocol modes. Chronologically they are:

- the initialisation mode,

- the adressing mode,

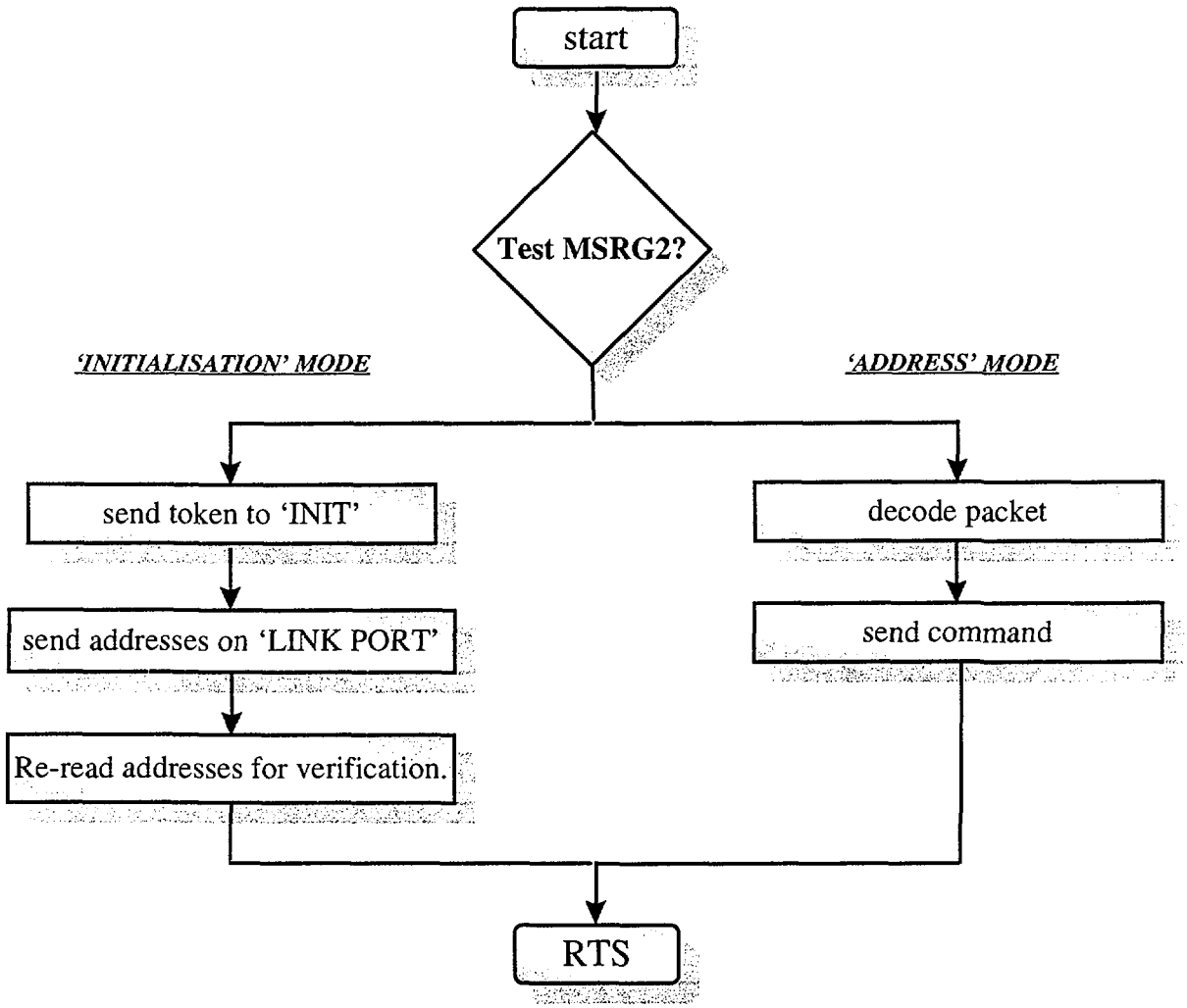
- the chained mode.

1:**'Initialisation mode'**: During recent tests, addresses for the programmed logic of each NULOC were static. In the long term, the NULOC cards will be integrated into the MCM circuitry and, due to the restricted space, it will no longer be possible to attribute static addresses for each NULOC. Instead, dynamical addresses will be allocated via the PATCH protocol. This will be carried out in the initialisation mode which is activated by the reception of a token. The token is generated by the DSP on the 'INIT' track. This in turn generates the first address on the LINK PORT. The token is then passed to the second NULOC and the second address is generated. This process continues until all the addresses are allocated. A verification is then carried out, via a test command, to ensure that all addresses have been downloaded to the NULOC's. This working mode is controlled by the "interrupt software" 'VIRPTI' provided by the DSP company. It has its own message register 'MSRG2' and a memory space which is reserved for this process.

2: **'Adressing mode'**. Various parameters and commands (pedestals and noise values per channel, resets, inhibits for cutting out undesired GASSIPLEX chips, etc...) need to be transmitted to the NULOC's. This occurs in the "addressing mode" and, as in the initialization mode, all downloaded values can be checked by the test command. This mode is also controlled by the 'VIRPTI' interrupt software of the DSP.

This IRQ controls the initialisation and addressing mode.

IRQ_VIRPTI



End of IRQ_VIRPTI

* **MSGR2** is a register that allows the acquisition to send a message to the DSP.

3: **'chained mode'** This mode authorises the transfer of the data from all the NULOC outputs available on the communication bus, and ensures their storage in a temporary buffer until the data acquisition system is ready to read them out. This whole process is controlled by the DSP.

Three hardware interrupts are used:

'irq2': DONE: This controls the downloading to the LCA and consequently validates the initialisation process.

'irq1': Trigger: This signals the start of an event and waits for data reception on the Link Port.

'irq0': DSY: End of data downloading.

NOTE: The priority order is of no importance as these interrupts are generated sequentially. Only one interrupt at a time is authorized. When "IRQ2" is finished, "IRQ1" is unmasked. When "IRQ1" is finished "IRQ3" is unmasked, etc...For additional security, the TIMER interrupt is used as a watchdog.

Two messages registers that allow exchanges with the acquisition are used:

MSRG2: acquisition informs the DSP that the acquisition process is accepted.

MSRG3: sends a message from the DSP to the acquisition to relay the number of events to be read out.

The general idea is that the acquisition process polls the MSRG3 register with the expectation of receiving a message that authorises it to read out the data stored in the DSP RAM. This message will arrive once the **'irq0'** interrupt routine is finished and its token sent. The message gives the number of channels to be read out. Then, it is the DSP's turn to keep an eye on the «**MSRG2**» register, until it receives an authorization allowing it to treat the next event. In interrupt terms, this implies that **'irq1'** is unmasked and is waiting for the next trigger to arrive.

The IRQ2: done interrupt allows to ensure that the LCA of each NULOC and the INV are correctly loaded and that their voltage supplies are working. This is only activated once, at the end of the DSP initialisation cycle.

Note: All the LCA's are loaded from a single PROM (Programmable Read Only Memory) on the INV. ».

detailed architecture:

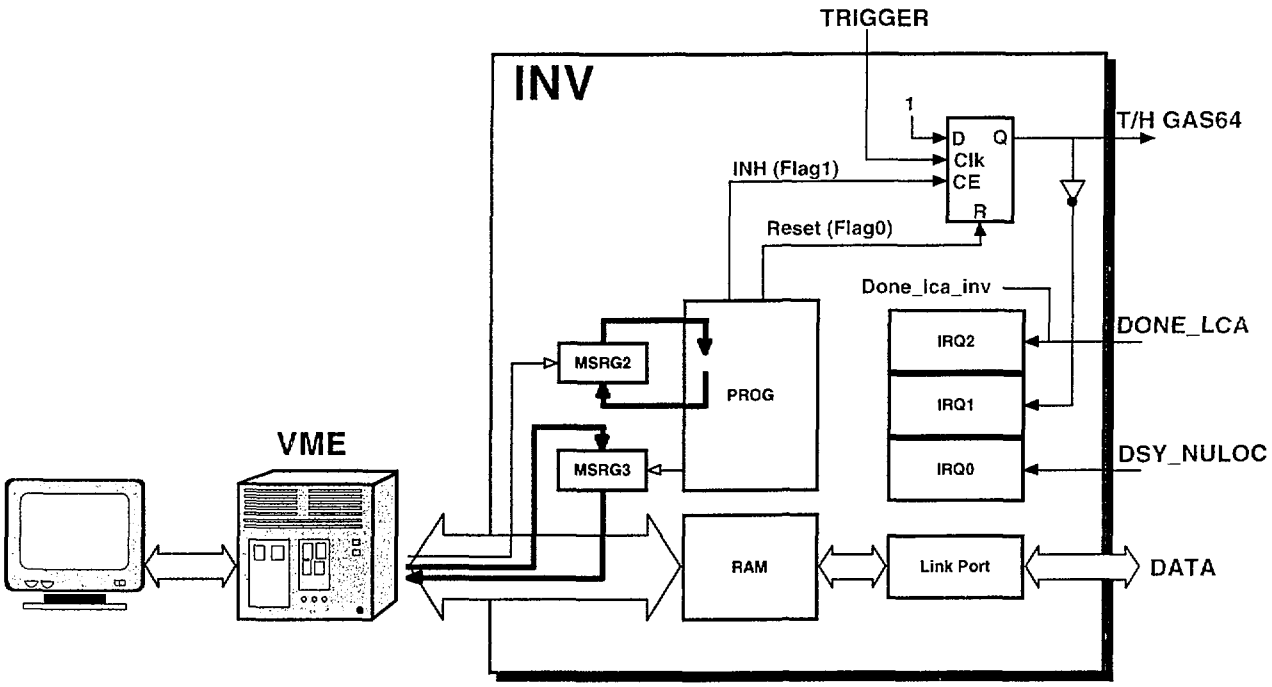


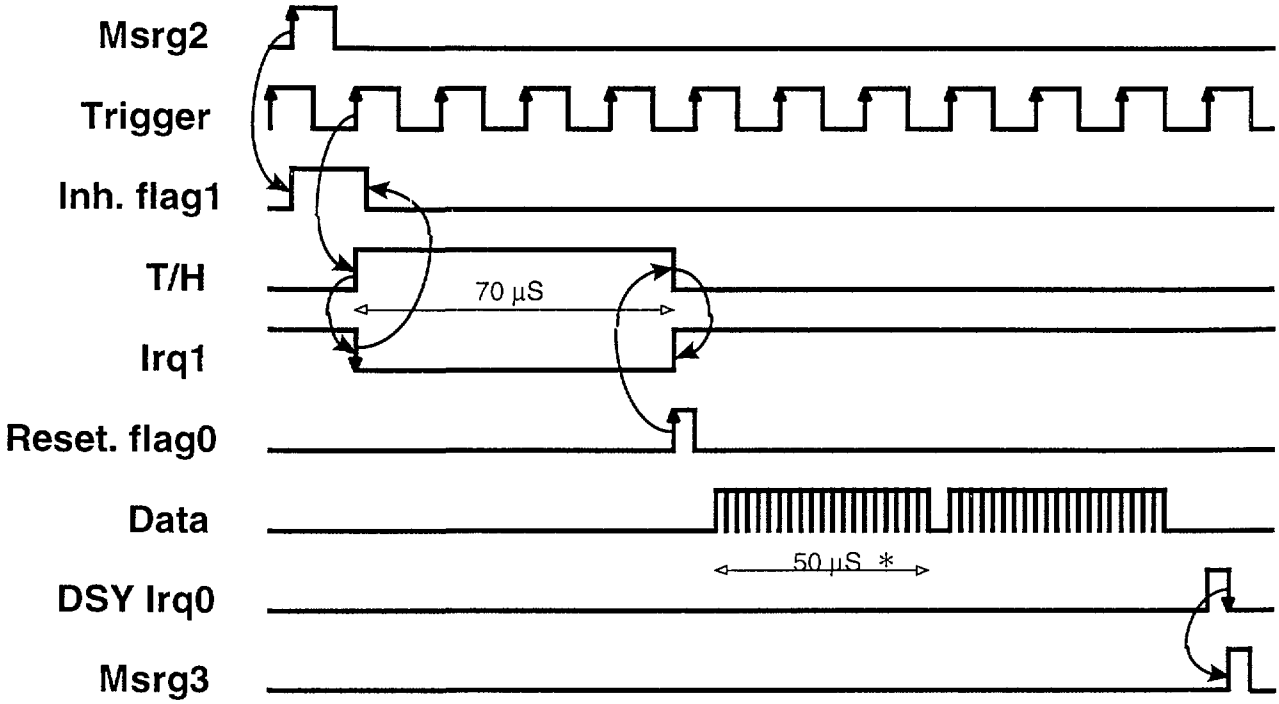
Figure 28:

The GAS64 T/H signal for calibrations or measurements is controlled via the "D" flip-flop on the INV card. Two DSP flags control this flip-flop.

- « **Flag1** » provides an inhibit signal. It describes when to send the T/H signal and is therefore directly related to the acquisition process. If an event is still being coded, this flip-flop inhibits the reception a new event.

- « **Flag0** » provides the flip-flop reset. This occurs 70µs after the trigger signal. The 70µs corresponds to the T/H time required to code 64 GASSIPLEX channels.

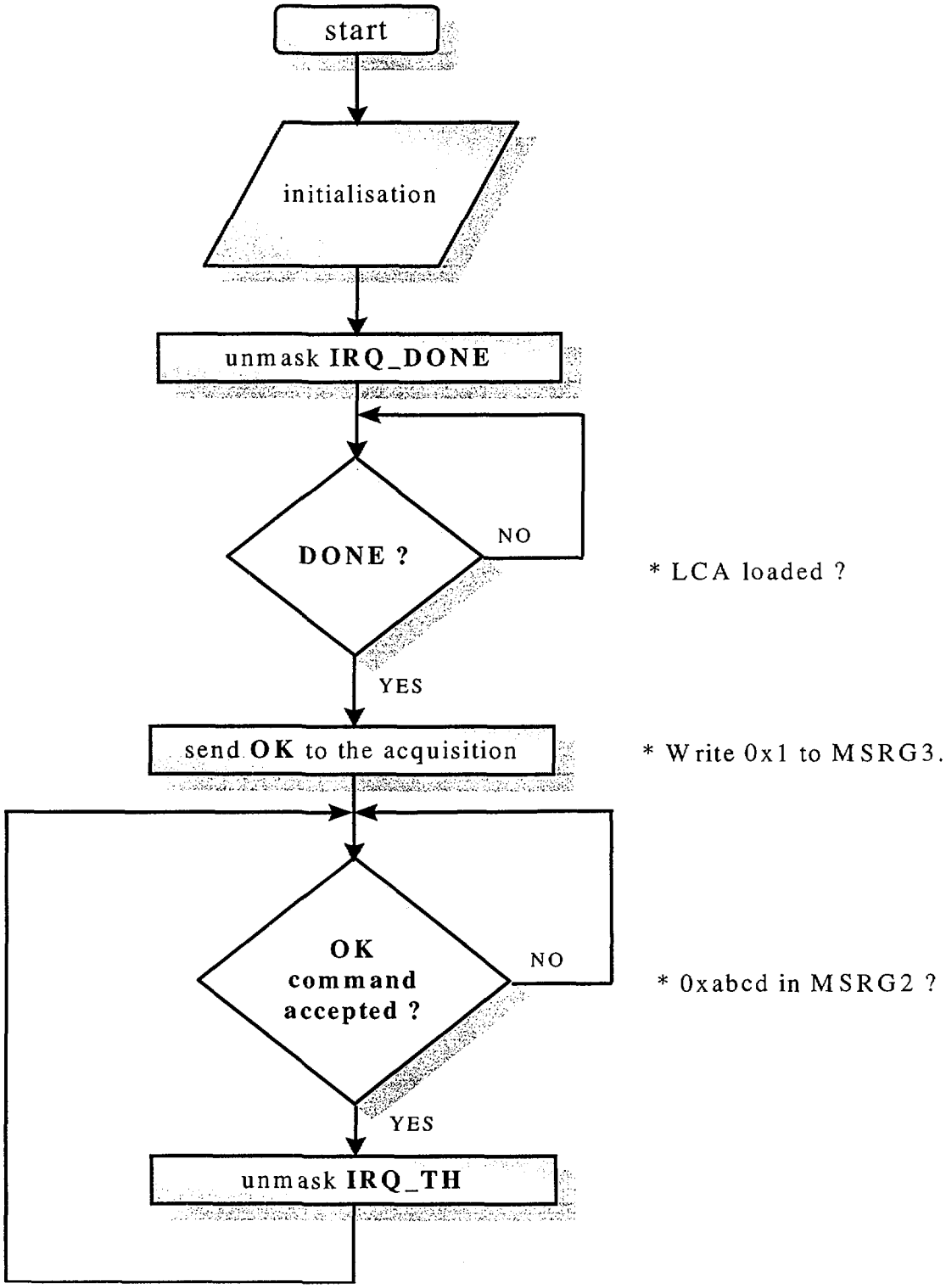
Timing diagram:



The cycle starts with an "accept" signal from the acquisition. The flip-flop is then allowed to change on a reception of the next trigger signal. A T/H signal is generated on the rising edge of the trigger pulse, followed by the Irq1 interrupt which disables the flip-flop. On the downgoing edge of the T/H signal, the NULOC's start down loading their data to the DSP memory one at a time. When this is finished a token is sent to the irq0 interrupt on the DSP. This starts a process that closes the data transmission line, and informs the acquisition that data is available on the RAM.

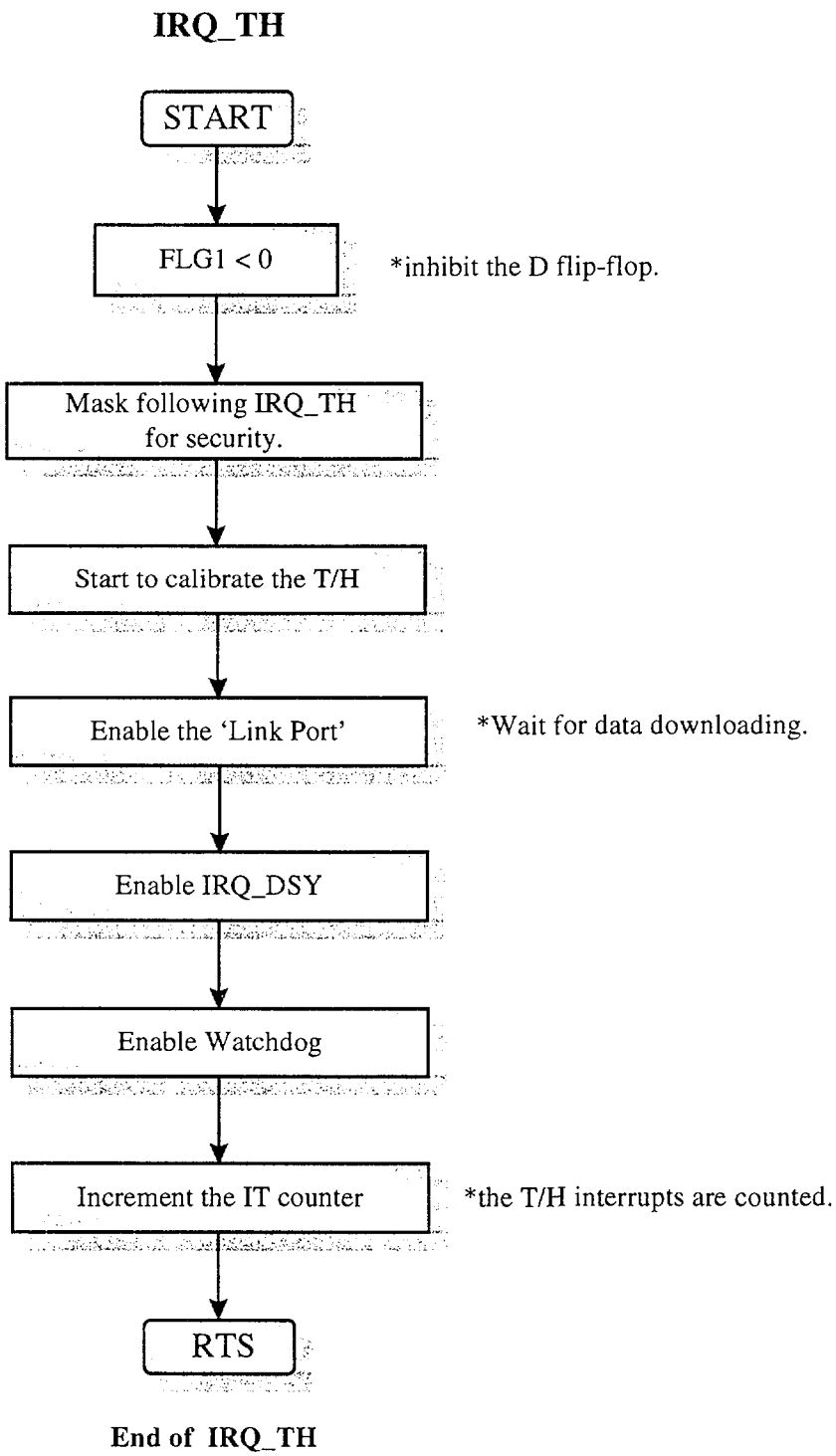
* The 50 µs for the Data signal corresponds to the time taken by one NULOC to transfer its data through the LINK PORT at 16 MHz.

DSP: Main program.



DSP: Irq TH .

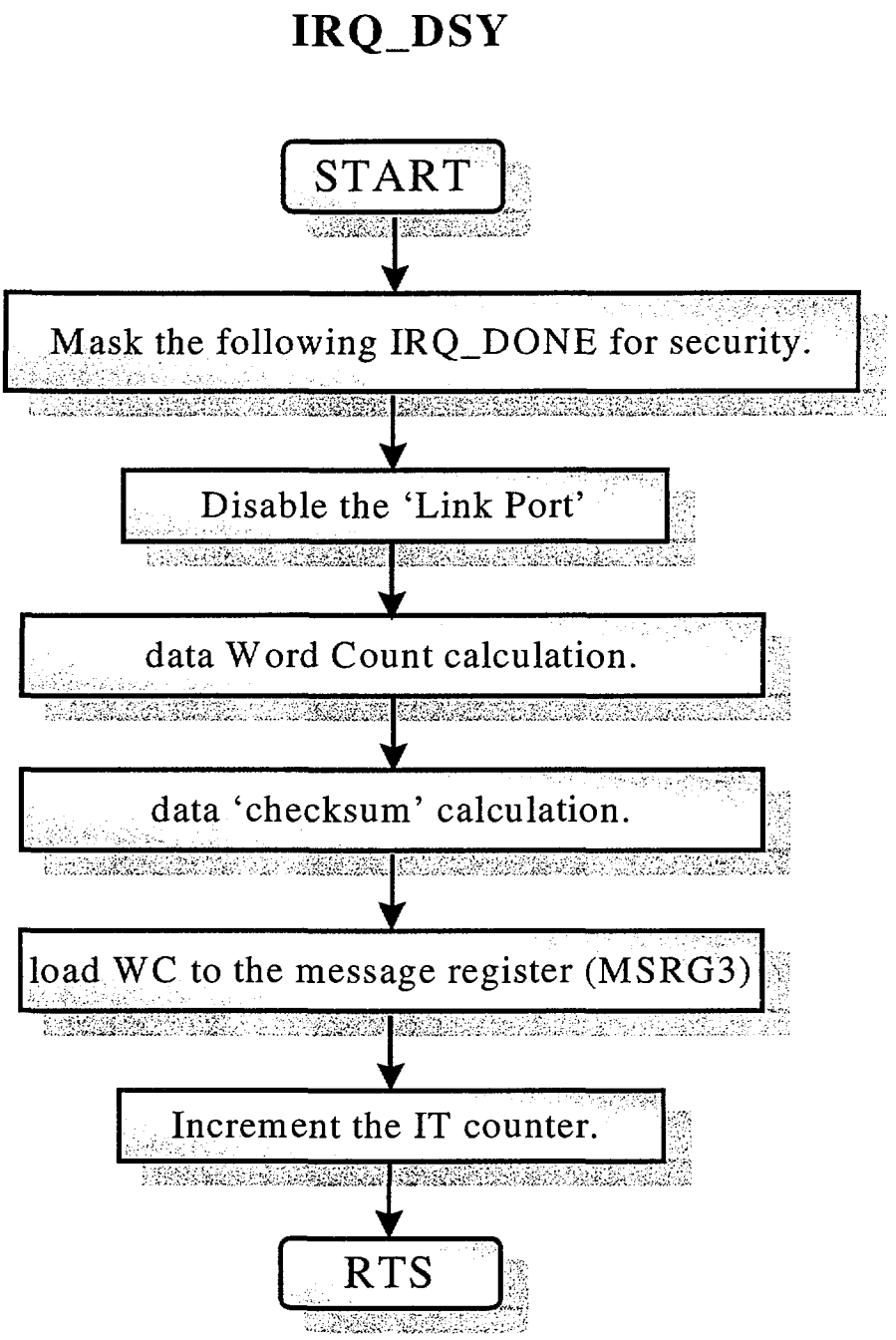
This IRQ is used for data downloading.



* Counter « **IRQ_TH_OUT_compt** » at address 0x25FF1.

DSP: Irq DSY .

Reminder: This IRQ signals the end of data downloading. It is controlled by the reception of a token



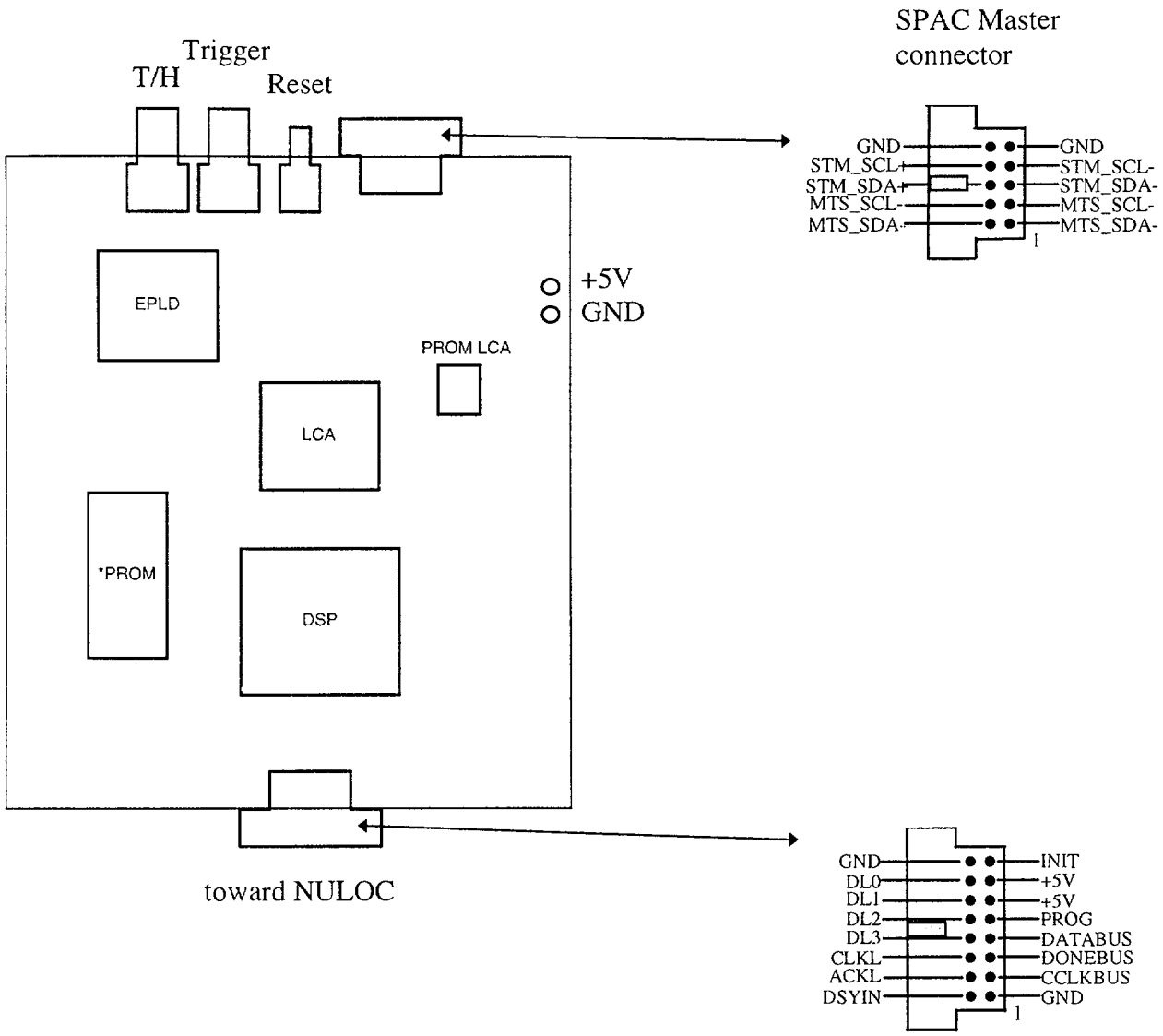
end of IRQ_DSY

* Counter « **IRQ_DSY_compt** » at address 0x25FF2.

* **MSGR3**Is a register that allows the DSP to send a message to The acquisition process (adr VME:0x0013).

MAIN CHARACTERISTICS
Dimensions = 164*137 mm^2.
Voltage supplies : +5V ~0.9A (INV only).
Note : The NULOC's are supplied by the INV card.

INV- TOP VIEW



Trigger:- TTL input activate in a high state.(LEMO 00).
T/H :- TTL output.(LEMO 00).
Reset : Manual reset. A software reset is also available.

*NOTE : Eventually, the DSP program will be downloaded from the PROM.

Interface with the SPAC serial link

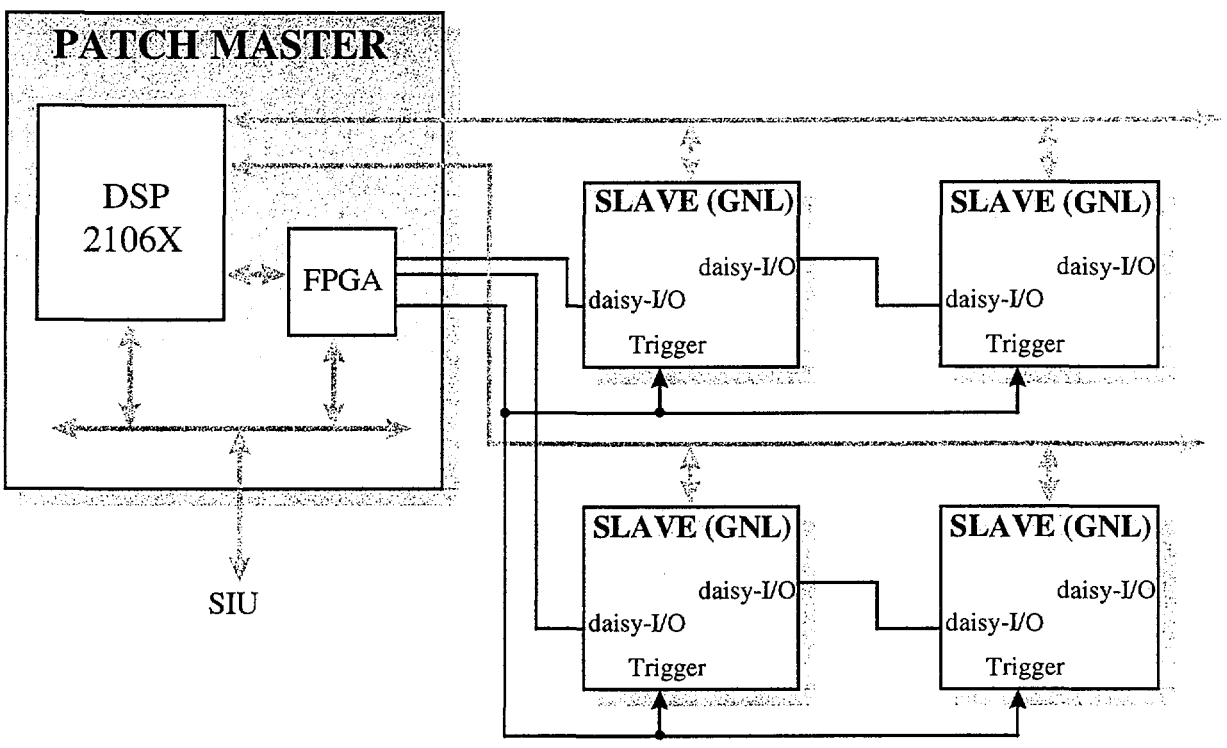
With the INV card implanted on the detector edge, a bus is required to provide the link between the VME crate and the INV card over a 30m distance. The SPAC serial link, developed at the Laboratoire de l'Accélérateur Linéaire (LAL) in Orsay, was chosen for its simplicity. Extra work was avoided as it was delivered with all the necessary software included.

APPENDIX 4

PATCH : Protocole for Alice Tracking Chamber

This protocol was developped to allow data readout and parameter control of an ensemble of modules (slaves) implanted on the ALICE tracking chambers. It consists of an auto-configuration mode that allows the dynamical attribution of addresses for each slave on the bus, a chained mode that allows the data readout of each consecutive slave and an addressing mode that allows to read and load all slave registers and memories. The bus is 2-way and works on a one-master, n-slaves basis. The bus was developed around the DSP LINK PORT (ADSP 2106X) made by Analog Devices. One DSP has 6 Link Ports. User programs may be written in machine code or C. More details concerning the different modes can be found in Appendix 3.

General view of the PATCH bus



1.1 Main characteristics

The bus characteristics are described in the next section. In the following the different types of transfer between the master and slaves are described.

- The protocol requires a Link Port Serial connection (see paragraph The Link Port), a 2-way link between the master and slaves (slaves are daisy chained) for the initialisation and chained readout mode and a physics trigger (one way communication).
The master and slaves are emitters or receivers on the bus. They are in ABT or GTL technology .

- It is the emitter that fixes the transfer rate. Rates up to 40 MB/s for a 80 MHz clock frequency are possible.

- The frame consists of 32 bits words which contains: a header word, an address register, channel numbers and data coded on 12 bits.

- The protocol has an auto-configuration phase where addresses for each slave on the bus are dynamically allocated. A register is reserved for the broadcast address (one address for an ensemble of slaves).

- The chained mode authorises the readout of data from all slaves on the bus. In chained mode, transmission from a slave is only authorised if it is in possession of a token. The token is transmitted from one slave to the next through the daisy chain. In chained mode the token is given to the first slave on the down-going edge of the trigger signal. The first slave is recognised by the hardware.

- slaves can only be configured through a command in broadcast address.

Addressing mode

- allows the read and write in the registers and memories of the slaves.

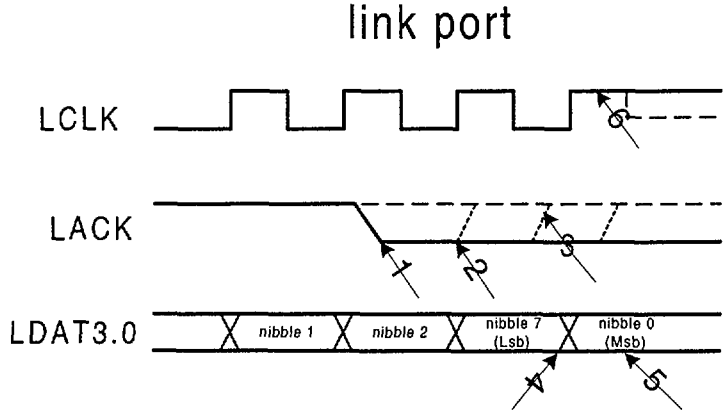
- acknowledgments are done through the first slave on the bus.

- the response format of a slave, to a read request from the master, is the same as that of the master, except for the header word.

- to avoid any risk of conflict, the slaves continually watch the status of the bus.

1.2 The LINK PORT

Each LINK PORT is comprised of 6 2-way communication lines. 4 lines are for data, one for a clock and one for the acknowledge signals. The clock allows the asynchronous transfer of data which is associated with an acknowledge signal from the handshaking process. A LINK PORT transfer is carried out through 32-bit or 48-bit words. This corresponds to 8 and 12 nibbles respectively (1 nibble = 4 bits). It is the emitter that fixes the transfer frequency. At a 80 MHz clock rate, this corresponds to 40 MB/s. It is also the emitter that pilots the signals corresponding to the data and the clock. The receptor controls the acknowledge signals. Each DSP contains 6 LINK PORTS which can work simultaneously or independently. Each possess their own DMA channel.



1) the acknowledge is set false (level 0) by the receiver after the 2nd nibble. This inhibits the transfer of the next word.

2) the acknowledge becomes true (level 1) as soon as the receiver is able to accept the next word

3) the emitter can "spy" on the acknowledge line in order to determine if it can send the next word without waiting.

4) the receiver accepts all nibbles of the last word sent, even if the acknowledge state is false.

5) the first nibble of the next word is held back until the acknowledge signal is enabled (true).

6) the clock stays enabled if the acknowledge is disabled. An enabled clock corresponds to a waiting period.

1.3 FRAME FORMAT

The 32 bits were composed as follow:

2^{31}	2^{30}	2^{29}	2^{24}	2^{23}	2^{18}	2^{17}	2^{12}	2^{11}	2^{0}
dir word instruction	r/w	subaddress		slave address		channel address		data	

The choice of the frame structure result from the need to minimise the reformating of the data while being read by the acquisition.

2^{31}: bit of tranfer direction (1 for the direction master to slave, 0 for the other).

2^{30} : Bit of read/write .The association of the two bits give the type of transfer .

2^{29} à 2^{24} : field of slave subaddress(61 possibilities), see figure of chapter 1.5 .

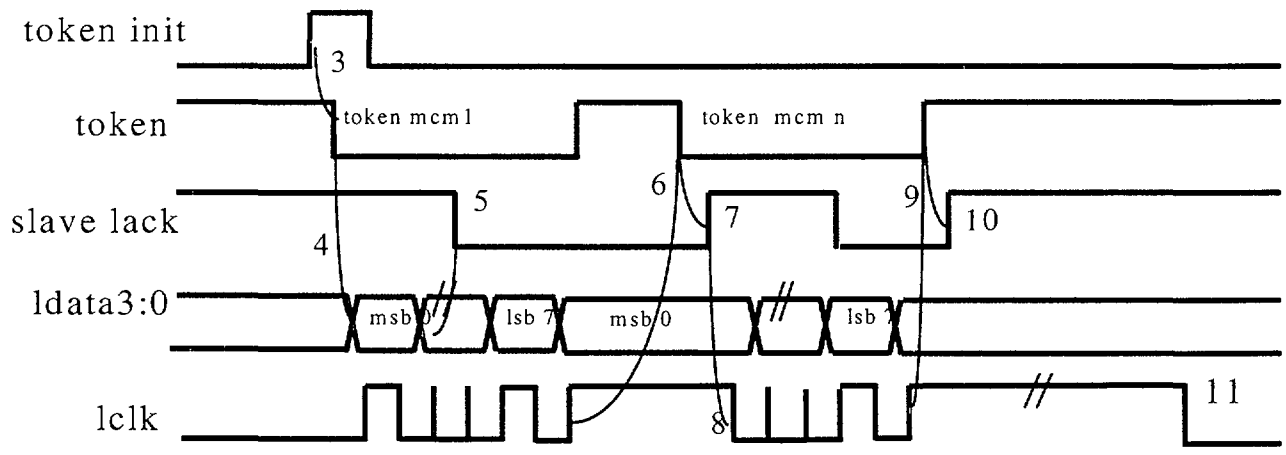
2^{23} à 2^{18} : slave address field (63 possibilities plus one broadcast address)

2^{17} à 2^{12} : channel address field (64 possibilities).

2^{11} à 2^{0} : data field

1.4 INITIALISATION MODE

This mode dynamically assigns one address for each slave after power up. The initial direction of the token line is slave to master, we manage the token line direction using a broadcast command. Chronologically, the process order is: 1st orientation of the token line ;2nd generation of a token to the nearest slave; 3rd the master sends the addresses to the slaves and 4th the orientation of the token line slave-to-master.



The master is the transmitter and generates a token (3) to the nearest slave then transmitted a word with the in the data field (4). The one de-assert acknowledge (5) to block the transmission of the next word, it decodes the command and memorises its address. The token (6) is then passed on to the next slave, the acknowledge is re-asserted (7). The master can

transmit the next word (8) with the address of the next slave who holds the token and this for 63 possible addresses.Then the master manages the token line direction (slave to master) . The master (in the addressed mode) scans all the possible addresses of the slave in order to discover the number of the slaves connected to the bus .

NB : before autoconfiguration the slave decodes the broadcast address
Example of transmitted frame:

1) Orientation of the daisy chain line : Master →slave

2e31	2e30	2e29	2e24	2e23	2e18	2e17	2e12	2e11	2e0
dir 1	r/w 0	subaddress 5		slave address 3F		channel address xx		data xx	

2) Transmission of the 63 addresses

2e31	2e30	2e29	2e24	2e23	2e18	2e17	2e12	2e11	2e0
dir 1	r/w 0	subaddress 1		slave address xx		channel address xx		data 0 à 2F	

3) Orientation of the daisy chain line: Slave →Master

2e31	2e30	2e29	2e24	2e23	2e18	2e17	2e12	2e11	2e0
dir 1	r/w 0	subaddress 6		slave address 3F		channel address xx		data xx	

1.5 ADDRESS MODE

This mode allows to give commands or to read/write in the slave registers connected to the bus. It is possible to address all the slaves connected to the bus through a broadcast address.The addressing of the slave is not possible until after the initialisation, ie. once each slave has been assigned an address.

The association of the first two bits gives the type of transfer

	2^{31} dir	23^{0} r/w
write master -> slave	1	0
read request master -> slave	1	1
reply slave → master	0	1

The subaddress field defines certain commands, the rest depends on the type of slave.

subaddress	2^{29}	2^{24}	2^{0}
slave address	0		
reset slave	1		
token_line direction Ms → Sla	2		0
token_line direction Ms <-- Sla	2		1
daisy chain mode	3		1
slave define	4 → 0x3F		
data coding	4		
offset + sigma	5		

The channel number is defined between 0 and 0x3F

In the field address, the broadcast address is fixed on the upper address of the field, the lower field structure 2^{22} a 2^{0} remain unchanged during the data read out.

address	2^{29} 2^{18}
broadcast address	0x3F
slave address	0 →0x2F

1.5.0 Example of frame transmitted by the PATCH protocol

write B into a register n of the slave Y

2^{31}	2^{30}	2^{29} 2^{24}	2^{23} 2^{18}	2^{17} 2^{12}	2^{11} 2^{0}
dir	r/w	subaddress	slave address	channel address	data
1	1	n	Y	xx	B

read request of a register n of the slave Y

2^{31}	2^{30}	2^{29} 2^{24}	2^{23} 2^{18}	2^{17} 2^{12}	2^{11} 2^{0}
dir	r/w	subaddress	slave address	channel address	data
1	0	0xY	0xY	xx	xxx

reply of the slave

2^{31}	2^{30}	2^{29} 2^{24}	2^{23} 2^{18}	2^{17} 2^{12}	2^{11} 2^{0}
dir	r/w	subaddress	slave address	channel address	data
0	1	n	0xY	xx	0x00B

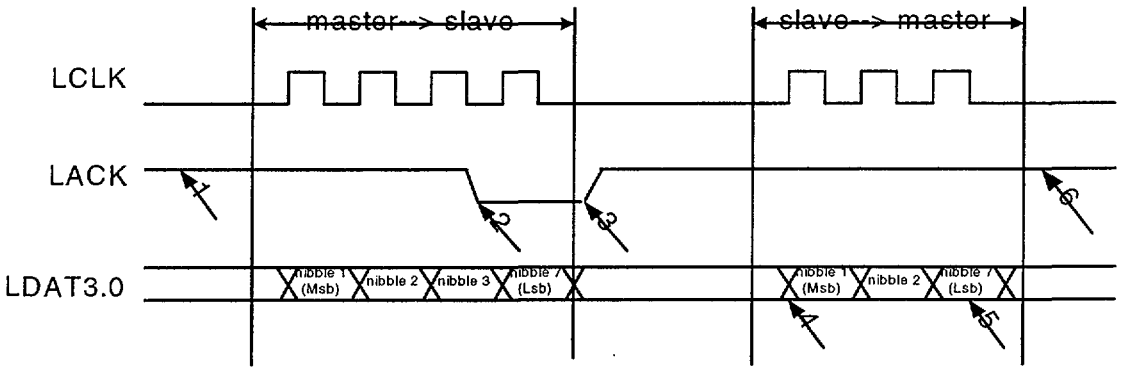
reset slave y

2^{31}	2^{30}	2^{29} 2^{24}	2^{23} 2^{18}	2^{17} 2^{12}	2^{11} 2^{0}
dir	r/w	subaddress	slave address	channel address	data
1	0	1	0xY	xx	xxx

reset the ensemble of the slave on the bus

2^{31}	2^{30}	2^{29} 2^{24}	2^{23} 2^{18}	2^{17} 2^{12}	2^{11} 2^{0}
dir	r/w	subaddress	slave address	channel address	data
1	0	1	0x3F		xxx

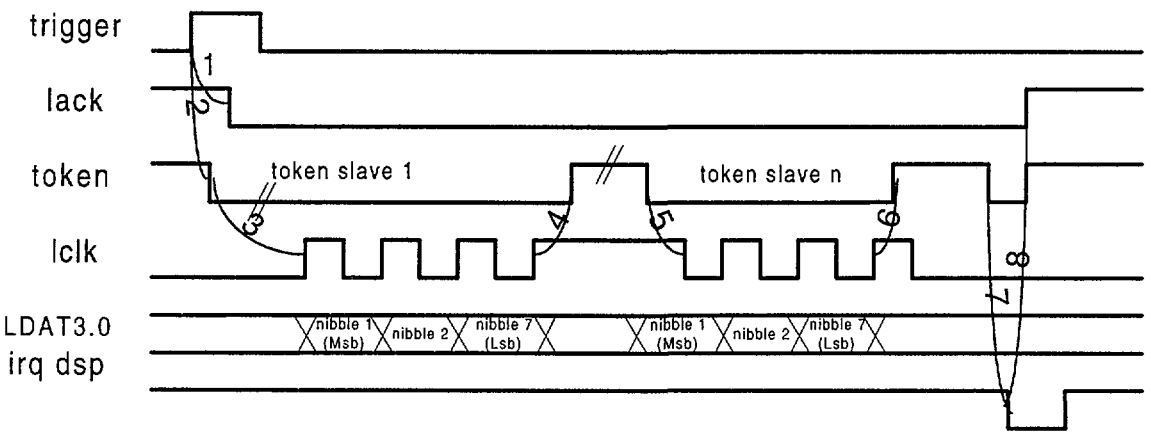
1.5.1 Relative timing of master read request



When the slaves are in receiving state the acknowledge is de-asserted (1) which permits the transmitter to send its word; at the fifth nibble (2) the slave which identifies its address de-asserts the acknowledge in order to block the next transmission, and to be able to treat the received word. At the end of the transmitted word, the master goes into receiver state, once the slave has finished treating the word it asserts the acknowledge (3) and goes into transmitter state. Before transmitting data the transmitter slave scans the clock and the acknowledge line to discover if they are not activity on the bus. Then transmits the word (4); at the end of the transmission (5) ,the slave returns into receiver state (6)

1.6 CHAINED MODE

This mode allows the reading of physical parameters memorised by all the slaves on the bus. There is no decoding in this mode, it is the possession of the token that allows the slaves to transmit their data on the bus. The slaves are configured in chain mode by a broadcast commanding.



On the edge of the trigger signal, all the slaves scan the `daisy-in` signal. The first slave on the line becomes the owner of the token (2), and the master goes into receiver state

(1). The slave which is in possession of the token transmits its data on the bus (3). At the end of the transmission the slave n passes the token to slave n+1 (4) and frees up the bus. The new holder of the token transmits its data (5). At the end of the transmission the last slave passes the token to the master (which generate an interruption (7)), this stops the transfert by de-asserting the acknolwedge (8).

1.6 TIMING CONSIDERATION FOR THE ALICE PROJECT

1.6.1 READING IN DAISY-CHAIN MODE

The clock frequencies of the patch slave is now 32 MHz, this is due to the type of logic used for the test module. This frequency allows to transmit up to 16 MB/s or 4 Mwords/s.

One chamber plane is divided in 36 regions. Each of them is managed by its own PATCH bus. The simulation gives the maximum number of words to be read by the bus as being 80. This implies a total of 20 μs to read and 1.5 μs for the token passing and other 3.5 μs is required for the software treatment. The total time per maximum event size is therefore **25** μs.

1.6.2 MASTER READING BY THE ACQUISITION

The architecture for the concentrator card for one plane is based on a cluster of 6 DSP in connection with a DDL (SIU). The transfer rate on the bus is 160 Mbytes/s. If we consider that we have 7.5 Kevts to read, then the total size for one event is 150 Kbytes/evt. The time of transfer will be **47** μs.

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[3] N. Willis et al.,

[4] J. Peyré, B. Genolini and J. Pouthas. *A full scale prototype for the tracking chambers of the ALICE muon spectrometer. Part I- Mechanics; Anode and Cathode plane design; Assembly and construction.* IPN Internal Report 98-07 and ALICE Note INT-98-28.

[5] J.C. Santiard et al., rapport interne CERN-ECP/94-17 et communication à "6th Pisa Meeting on Advanced Detectors, La Biadola, Isola d'Elba, Italy, 22-28 May 1994".

[6] J.C. Santiard, Note Interne N^0 2, ECP/MIC 1-09-95

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http://home.cern.ch/~richrd26/hmpid/pub/gassidoc.ps
Multipurpose analog multiplexed read out system for pad/strip detectors: description and instruction manual

[8] ALICE DATE User's Guide. ALICE 98/44 Internal Note/DAQ