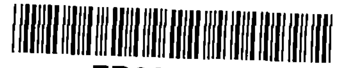

FR0203898
INIS-FR-2053

0.25µm Radiation Tolerant Technology for Space Applications

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Introduction

Historically, radiation hardened technologies have lagged state-of-the-art commercial technologies by several generations, a fact that limited space system capabilities. With the advent of broadband space communications, the need for high density, low power, radiation tolerant technology becomes imperative. Lockheed Martin Federal Systems (LMFS) in Manassas, VA, USA, has developed a state-of-the-art, radiation tolerant 0.25µm CMOS capability that is compatible with commercial foundries as well as radiation hardened fabrication. The technology satisfies the needs of advanced commercial space as well as radiation hard military applications.

Radiation Hardened CMOS

LMFS has over the years transferred several generations of Commercial CMOS technology to its Semiconductor Technology Center (STC), and enhanced them for radiation applications while preserving the basic technology attributes such as performance, power and density (Figure 1). A commercial design can be easily migrated to the radiation hardened process to achieve Mega-rad total dose hardness and latch-up immunity. Furthermore, Single Event Upset (SEU) enhanced features can be added to achieve SEU immunity. Radiation hardened 1.0µm, 0.8µm, and 0.5µm CMOS have been QML production qualified for years, and used for the fabrication of SRAM, ASICs and Micro processors.

The same successful methodology is being used for the transfer and hardening of a commercial 0.25µm CMOS technology. A low power, SEU enhanced library has been developed and is being validated; a SEU enhanced 4M SRAM is in fabrication; and a high performance IBM Power PC 740/750 is being enhanced for space applications. Power, performance and density attributes of the 0.25µm CMOS (R25) are presented in Figure 2 and compared to other technology generations. R25 represents 30X improvement in technology figure of merit over the current state of the art generation (RHCMOS-5M) and 7000X improvement over 1993 capability.

Evaluation

A technology test chip (TTC) was designed, fabricated and evaluated for performance, power and radiation hardness in order to validate the methodology and evaluate the technology. Additional evaluation results will be available by mid-1999.

Total dose: Ionizing radiation degrades CMOS behavior by inducing threshold voltage shift and creating parasitic leakages due to field inversion. As the technology scales to smaller dimensions the threshold voltage shift becomes negligible, while parasitic leakages become the predominant mechanism. Figure 3 shows the 1 Mrad (Si) threshold shift as a function of gate oxide thickness for 0.5µm, 0.35µm and 0.25µm devices (tox = 12nm, 7nm and 5nm respectively). It is evident that active transistor threshold shift is negligible for 0.25µm CMOS. For field hardening, we used a similar hardening technology on the 0.25µm Shallow Trench Isolation (STI) as was used with the radiation hardened LOCOS on previous generations of CMOS. Figure 4 shows a transistor response of a STI isolated transistor before (a) and after (b) field hardening. It is clear that the hardened STI can support Mega-rad applications.

Single Event Effects (SEE): the radiation enhanced 0.25μm CMOS is fabricated on thin epitaxial substrates and utilizes twin (n and p) wells. This approach reduces the parasitic resistance as well as the parasitic bipolar gain, thus increasing the holding voltage well beyond the operating voltage of 2.5V. Electrical latch-up testing on sub-groundrule structures showed no latch-up below 4.5V. Neither single-event latch-up (SEL) nor single-event gate rupture (SEGR) were detected during heavy ion testing of SRAM and logic circuits through 3.3V, LET= 104 MeV- cm^2/mg and 125°C.

Table 1 shows representative SEU test results for the 0.25μm TTC. This information was vital to the development of the ASIC library, 4M SRAM, and radiation enhanced Power PC. It can be seen, that with the proper use of hardened elements, an average SER of 1E-10 upset/bit-day can be achieved in the 90% geosynchronous orbit environment. Furthermore there is no proton sensitivity for proton belt application.

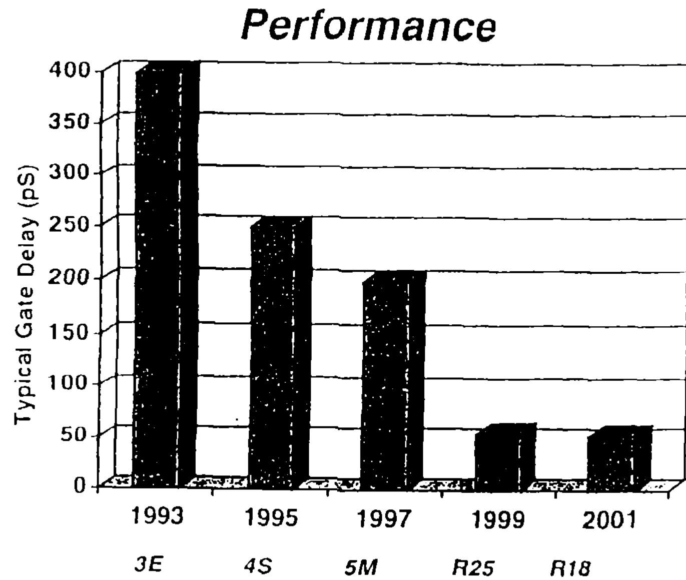
Conclusion

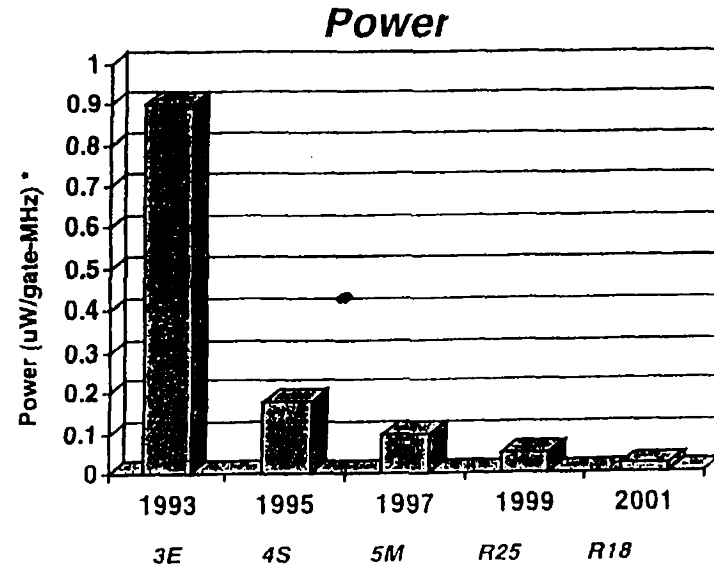
A 0.25μm CMOS radiation tolerant capability (Leff = 0.18μm) has been developed and demonstrated. The technology is intended to support high density, high performance and low power space applications. Hence, it is immune to latch-up and SEGR, and is hardened against single event upset. It is currently being used for the design of spaceborne ASICs, 4M SRAM, and a radiation enhanced Power PC Processor.

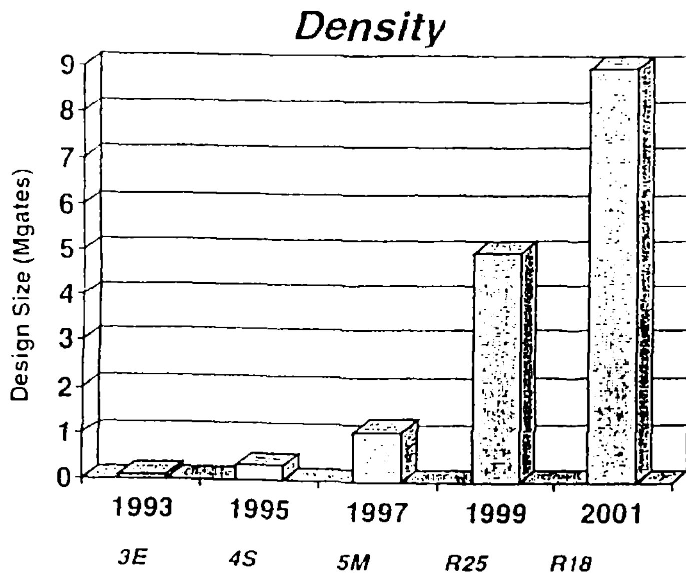
	RHCMOS 2E/2S	RHCMOS 4E/4S	RHCMOS 5ML/5M	RHCMOS 5XL/5X	RH-25	RH-18	RH-15
Minimum Feature:	1.0μm	0.7μm	0.5μm	0.5μm	0.25μm	0.18μm	0.15μm
Effective Channel:	0.8/0.5μm	0.8/0.5μm	0.5μm	0.3/0.25μm	0.20μm	0.15μm	0.12μm
Power Supply:	5V/3.3V	5V/3.3V/2.5V	5V/3.3V/2.5V	3.3V/2.5V	2.5V/1.8V	1.8V/1.5V	1.5V/1.2V
Substrate:	Epi	Epi	Epi	Epi	Epi / SOI	Epi / SOI	Epi / SOI
Isolation:	LOCOS	LOCOS	LOCOS	Trench (STI)	Trench (STI)	Trench (STI)	Trench (STI)
Interconnects:	Lift off	Planar	Planar	Planar	Planar	Planar	Cu/Low-K
Wiring Levels:	2 to 3	2 to 4	3 to 5	3 to 5	4 to 5	4 to 6	5 to 7
Max Chip Size:	161 mm^2	196 mm^2	400 mm^2	400 mm^2	848 mm^2	848 mm^2	848 mm^2
Package Pins:	308	340	340	340	1,089	1,089	1,800
Die-Package Wiring:	Wirebond, Flip-Chip	Wirebond, Flip-Chip	Wirebond, Flip-Chip	Wirebond, Flip-Chip	Wirebond, Flip-Chip	Wirebond, Flip-Chip	Wirebond, Flip-Chip
Hermetic Package:	Flatpack	Flatpack	Flatpack	Flatpack	Flatpack/CGA	Flatpack/CGA	Flatpack/CG/
Typical Radiation Hardness:	Total Dose: >1 Mrad(Si); Single Event Upset: <1E-10 Upset/Bit-Day; Single Event Latch-Up: Immune; Prompt Dose Upset: >1E9 rad(Si)/s						
QML Qual:	Complete	Complete	Complete	Demo	4Q00	4Q01	4Q03

Figure 1. Radiation Hardened Technology Roadmap

Figure 2: ASIC Technology Evolution







Power x Performance/Density

RHCMOS-3E = 200X
RHCMOS-4S = 8X
RHCMOS-5M = 1X
RH-25 = 0.03X
RH-18 = 0.008X

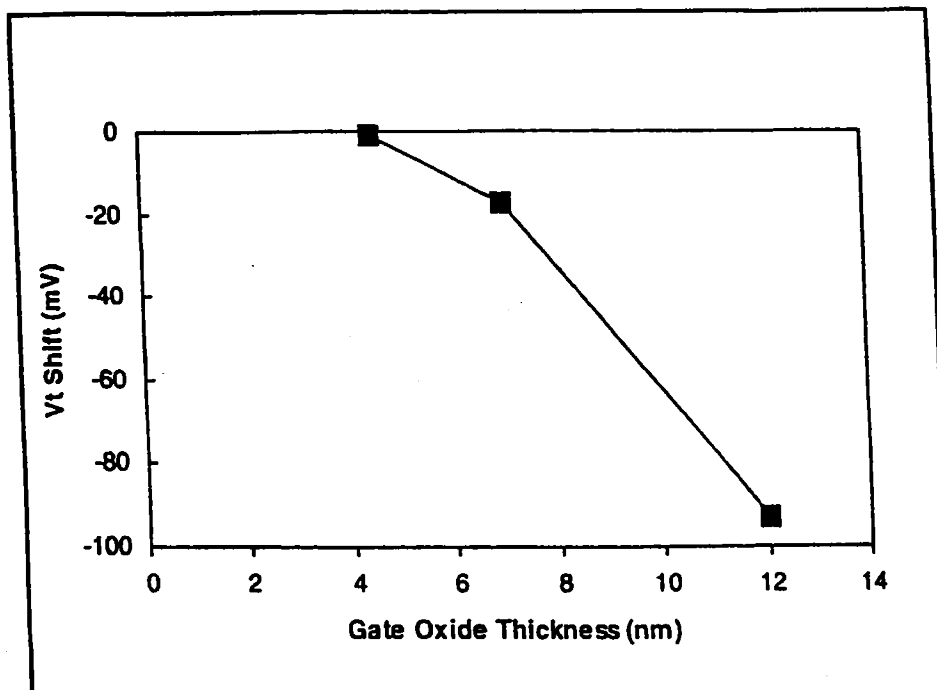


Figure 3: Vt Shift Versus Gate Oxide Thickness

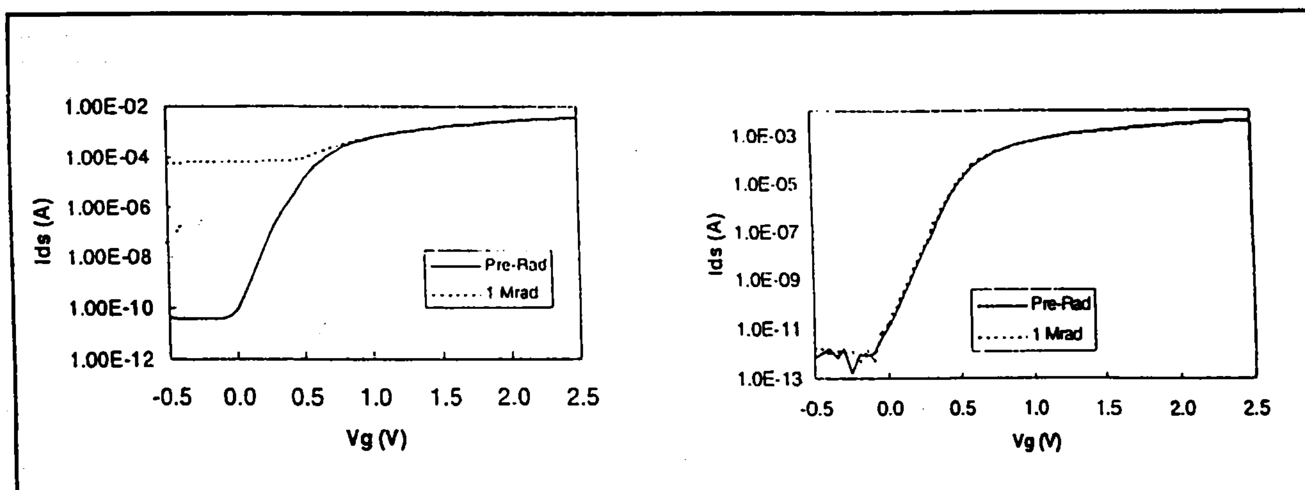


Figure 4 (a): Radiation Shift For Non Hardened Devices

Figure 4 (b): Radiation Shift For Hardened Devices

Table1: Sample SEU test Results for the 0.25μm Technology Test Chip.

Circuit	LET_{TH} (MeV.cm²/mg)	X-Section (μm²/bit)	90% GEO SER (upset/bit.day)
Soft RAM	5	20	2E-6
Hardened RAM	30	0.5	1E-10
Soft Latch	11	10	6E-7
Hardened Latch/ Hardened Clock	85	0.02	3E-12
Hardened Latch/Soft Clock	25	1	1E-8