HOT INTERCONNECTS 25

IEEE Symposium on High Performance Interconnects
August 28-30, 2017
Ericsson, Santa Clara, CA

The international forum where the high-performance computing and high-speed networking communities meet

MONDAY, AUGUST 28

TRACK 1	**Tutorial 1** *8:30 – 12:00*	Exploiting High-Performance Interconnects to Accelerate Big Data Processing with Hadoop, Spark, Memcached, and gRPC/TensorFlow *D. K. Panda & X. Lu,* **Ohio State University**
	Tutorial 2 *13:30 – 17:00*	High Performance Distributed Deep Learning for Dummies *D. K. Panda, A. A. Awan, and H. Subramoni,* **Ohio State University**
TRACK 2	**Tutorial 3** *8:30 – 10:00*	Designing and Developing Performance Portable Network Codes *P. Shamis,* **ARM** *& Y. Itigin,* **Mellanox Technologies**
	Tutorial 4 *10:30 – 12:00*	Developing to Open Fabrics Interfaces libfabric *S. Hefty,* **Intel** *& J. Swaro,* **Cray**
	Tutorial 5 *13:30 – 17:00*	The TraceR/CODES Framework for Application Simulations on HPC Networks *N. Jain,* **LLNL** *& M. Mubarak,* **ANL**

TUESDAY, AUGUST 29

MORNING	**Welcome Address** *9:00 – 9:10*	*Elisabetta Romano,* **Ericsson**
	Keynote *9:10 – 10:15*	RDMA deployments: from cloud computing to machine learning *Chuanxiong Guo,* **MSR**
	Best Papers *10:30 – 12:00*	▪ Improving Non-Minimal and Adaptive Routing Algorithms in Slim Fly Networks ▪ Routing Keys ▪ Fast Networks and Slow Memories: A Mechanism for Mitigating Bandwidth Mismatches
AFTERNOON	**Large Scale Networking** *13:00 – 14:00*	▪ WaveLight: A Monolithic Low Latency Silicon-Photonics Communication Platform for the next generation Disaggregated Cloud Data Centers ▪ An FPGA Platform for Hyperscalers ▪ Throughput Models of Interconnection Networks: the Good, the Bad, and the Ugly
	Invited Talk *14:00 – 14:45*	Performance Isolation for Highly Efficient Shared Infrastructure Services *Nandita Dukkipati,* **Google**
	Panel *15:05 – 16:35*	**Ethernet vs. HPC: Can the hyperscale Ethernet data center handle all workloads?** Moderator: *Roy Chua,* Partner, **SDxCentral & Wiretap Ventures** *Yogesh Bhatt, Senior Director,* Ecosystem Innovation & Strategy, **Ericsson** *Dave Cohen,* Senior Principal Engineer & System Architect, **Intel** *Pete Fiacco,* CTO, **GigaIO Networks** *Bithika Khargharia,* Former Principal Architect, **Extreme Networks** *Dave Meyer,* Chief Scientist, **Brocade** *Ying Zhang,* Software Engineer, **Facebook**
	16:35 – 18:35	HEAD BUBBA MEMORIAL COCKTAIL RECEPTION

WEDNESDAY, AUGUST 30

MORNING	**Keynote** *9:00 – 10:00*	Information Transfer in the era of 5G *David Allan,* **Ericsson**
	Optics & Networks for Science *10:30 – 12:00*	▪ A High Speed Hardware Scheduler for 1000-port Optical Packet Switches to Enable Scalable Data Centers ▪ Subchannel Scheduling for Shared Optical On-chip Buses ▪ Utilizing HPC Network Technologies in High Energy Physics Experiments
AFTERNOON	**Topologies, Routing & Process Placement** *13:30 – 15:00*	▪ On the Impact of Routing Algorithms in the Effectiveness of Queuing Schemes in High-Performance Interconnection Networks ▪ Placement of Virtual Network Functions in Hybrid Data Center Networks ▪ MPI Process and Network Device Affinitization for Optimal HPC Application Performance
	Invited Talk *15:15 – 16:00*	Communication at the Speed of Memory *Paolo Faraboschi,* **HP**
	Efficient Network Design & Network Architecture *16:00-17:30*	▪ Characterizing Deep Learning over Big Data (DLoBD) Stacks on RDMA-capable Networks ▪ Low-Level Host Software Stack Optimizations to Improve Aggregate Fabric Throughput ▪ Userspace RDMA Verbs on Commodity Hardware using DPDK
	17:30 – 17:45	AWARDS & CLOSING REMARKS

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