Implementation of Heart Rate Variability Signal Processing into FPGA: System on-Chip Design

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Abstract

In this paper, we try to develop and implement the HRV signal processing into a Field Programmable Gate Array (FPGA) for extracting this signals feature.

The hardware implementing algorithm was developed in Verilog Hardware Description Language (HDL). In designed hardware, after defining the number of samples in the input, it extracts and analyses the time domain features of HRV signal and also the parameters that can be extracted from the Poincare plot of this signal. The number of 15 recorded HRV signal from the Physionet database (Normal Sinus Rhythm (NSR), Congestive Heart Failure (CHF) and Atrial Fibrillation (AF)) used as test input to test the modules implemented on FPGA. The performance of the system was tested using MATLAB and validated based on the mentioned input signals.

Simulations show that the proposed system is able to achieve appropriate HRV analyses in the hardware. This system can be develop and use for more feature extraction by different kinds of analysis on HRV signal. The proposed system is suitable for portable monitoring devices and arrhythmia detection and as a biomedical signal processor on a system-on-chip (SOC) design.

1. Introduction

The surface ECG is the recorded potential difference between two electrodes placed on the surface of the skin at pre-defined points [1]. The largest amplitude of a single cycle of the normal ECG is referred to as the R-wave manifesting the depolarization process of the ventricle [1-3]. The time between successive R-waves is referred to as an RR-interval [3]. The variability in a series of RR intervals has been widely used as a measure of heart function which helps to identify patients at risk for a cardiovascular event or death. Analysis of variations in this time series is known as heart rate variability (HRV) analysis [2].

Heart rate variability (HRV) is a reliable reflection of the many physiological factors modulating the normal rhythm of the heart [4]. The analysis of HRV signal provides more valuable information for the physiological interpretation of heart rate fluctuations [3, 4]. The importance of this signal needs more investigation of methods as aids to clinical evaluation. Many works have been done to extract different kinds of information from HRV signal in various ways. Time, Frequency and nonlinear analysis of this signal are the majors processing that have been done on HRV signal and the resulted features are useful tools for diagnosis different problems in heart function [2].

In the other side, intelligent system requires smart controller for performance improvement of the system. Medical instrumentation also require intelligent controller for more sophisticated facilities to improve the performance [5]. Behind the intelligent system there is an intelligent controller plays an important role [6]. In the block diagram shown in figure 1, the medical instrumentation application requires sensor for sensing physiological signal from the patient body. After getting electrical signal from the sensor output the signal is amplified and conditioning for appropriate signal strength. Since the intelligent digital controller requires digital data to further processing there is Analog to Digital Convertor (ADC) chip. The controller here is responsible for overall handing of the signal like recording, displaying and sending to the remote places.

Above mansion functionality of the system requires different architecture of the controller to handle different activity like speed, data storage program ability and power consumption of the system [5].

The performance of the system depends on the processing power and the computational power of the central controller unit. Depending on the central controller selection one can improve the system performance in terms of power, speed and cost of the system [5]. There are varieties of controller unit available
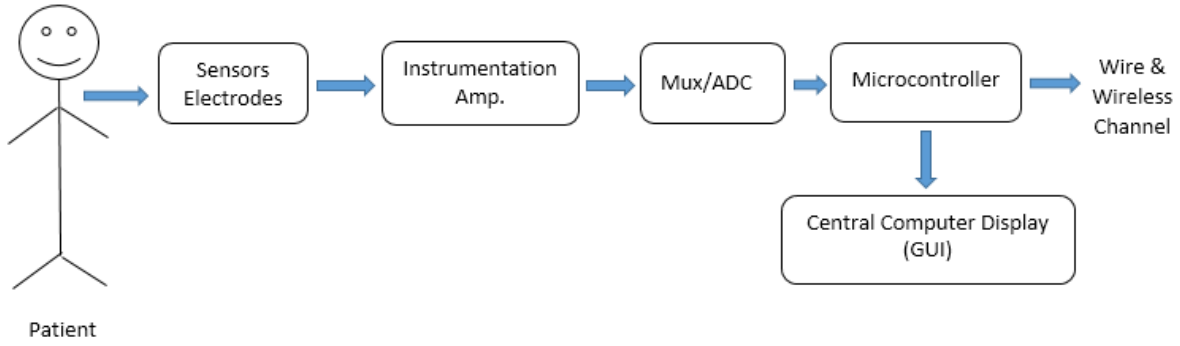
Figure 1. Medical instruments requirement.

like microcontrollers, Programmable system on chip, Digital Signal Processor and soft core which can be utilized on specialized programmable hardware like FPGAs and CPLDs.

Todays VLSI technology offers field programmable logic devices (FPGA). These devices offer total system requirements into a single chip by configuring by hardware descriptive languages (HDLs) [7]. The program can be erased and reprogram again as per user requirements. Here, the programmable logic devices can be programmed by the electronic design automation (EDA) tool which offers the programming in the various HDL options. The FPGA based embedded core offers dynamic change of algorithm and reprogrammed it many times [7].

In this paper, we tried to use the advantages of FPGA systems to increase and develop the performance of Heart rate variability signal processing. For this purpose, first of all we mention the parameters of the HRV processing that we have implement on the hardware and then explain hardware implementation. At last, for evaluating the system, we compare the results with which one obtained from analyzing our signals by MATLAB.

2. HRV signal processing features

First we have the signal of heart rate variability with a finite number of intervals, consider RR intervals as RR_i with $i = 1, 2, …, N$ where RR_i denotes the value of i'th RR interval and N is the total number of successive intervals.

The most evident of linear indexes of HRV is the mean value of RR intervals (RR) or correspondingly, the mean Heart Rate (HR). In addition, several variables that measure the variability within the RR series exist.

The standard deviation of RR intervals (SDRR) reflects the overall (both short-term and long-term) variation within the RR interval series which is defined as

[8]:

$$SDRR = \sqrt{\frac{1}{N-1}\sum_{i=1}^{N}\left(RR_i - \overline{RR}\right)^2} \qquad (1)$$

in which the mean RR interval is shown by $\overline{RR} = E\{RR_i\}$.

For stationary RR series, the root mean square of successive differences (RMSSD) given by [8]:

$$RMSSD = \sqrt{\frac{1}{N-1}\sum_{i=1}^{N-1}\left(RR_{i+1} - RR_i\right)^2} \qquad (2)$$

The next parameters are ones which are obtained from the Poincare plot of RR intervals. A standard Poincare plot of RR interval is shown in figure 2. Given a time series $RR = \{RR_1, RR_2, …, RR_n, RR_{n+1}\}$ the standard Poincare plot is a scatter gram constructed by locating points from the time series on the coordinate plane according to the pairing (x_i, y_i) in which [9],

$$x = \{x_1, x_2, …, x_n\} = \{RR_1, RR_2, …, RR_n\} \qquad (3)$$

$$(4)$$
$$y = \{y_1, y_2, …, y_n\} = \{RR_2, RR_3, …, RR_{n+1}\}$$

and i = 1, 2, 3, …, n and n is the number of points in the Poincare plot which is one less than the length of the RR time series [9].

$SD1$ and $SD2$ are two standard descriptors of Poincare plot [10]. $SD2$ is defined as the standard deviation of the projection of the Poincare plot on the line of identity ($y = x$), and $SD1$ is the standard deviation of projection of the Poincare plot on the line perpendicular to the line of identity ($y = -x$) [10]. So we may define them as:

$$SD1 = (Var(d_1))^{1/2}, \quad SD2 = (Var(d_2))^{1/2} \qquad (5)$$

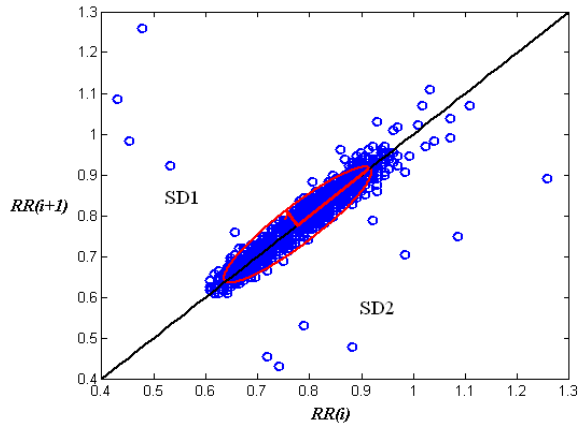Figure 2. Poincare plot of RR intervals of a healthy person with its standard descriptors *SD1* and *SD2*

where Var(d) is the variance of *d*, and

$$d_1 = (x-y) / (2)^{1/2}, \quad d_2 = (x+y) / (2)^{1/2} \qquad (6)$$

3. Designing and implementation into FPGA

The algorithm can be analyzing the component of the HRV signals and information in real time for identifying the abnormal rhythm and heartbeat. The programmed System on Chip (SoC) will be controlling analyzing and extracting features of HRV signals.
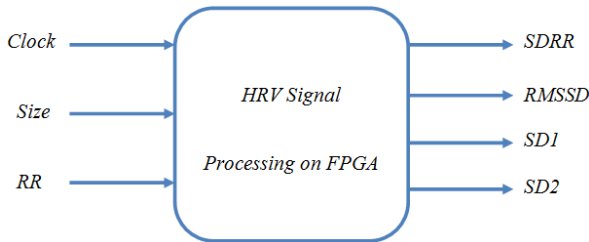

Figure 3. Block diagram of the inputs and outputs of the designed system.

The hardware implementing algorithm was developed in Verilog Hardware Description Language (HDL). In designed hardware, we have three inputs: Clock, Size, RR. These inputs are shown in figure 3. Clock should be an oscillators with optional frequency. This frequency

have relation with the speed of the process. If the oscillator's frequency is higher, the speed of the process is more. The second input of the system is Size. Size is a decimal number which defined the length of the HRV signal, it means Size is the number of RR intervals. The last input and the main one is RR that contains the HRV signal with the length of Size. These inputs are enters with the high edge of the clock. For improving the performance of the system, synchronization of the input and pulse of clock have been used. The input data save in a *1 x Size* matrix. After analyzing and calculating the mentioned features, we will have the outputs. As explained above, the system has four outputs which are the known features of HRV processing: SDRR, RMSSD, SD1 and SD2. These outputs are shown in figure 3.

4. Evaluation of performance of the SoC

Three groups of different heart arrhythmia (Normal Sinus Rhythm (NSR), Congestive Heart Failure (CHF) and Atrial Fibrillation (AF)) used as test input to test the modules implemented on FPGA. The performance of the system was tested using MATLAB and validated based on the mentioned input signals and the results have been compared.

The data from MIT-BIH Physionet database [11] are used in the experiment. In this study, we have used 15 long-term ECG recordings of subjects in normal sinus rhythm from Physionet Normal Sinus Rhythm database. Furthermore, we have used 15 long-term ECG recordings of subjects with CHF from Physionet Congestive Heart Failure database along with 15 ECG recordings of subjects with Atrial Fibrilation from Physionet Atrial Fibrillation database [11]. The original long term ECG recordings in every three groups were digitized at 128 Hz [11].

5. Results

For evaluating the performance of the designing SoC for HRV processing, we compared the results obtained from the system with the results we get using MATLAB software. For this purpose, two parameters were used to evaluate the designed system, which are Sensitivity:

$$Se = TP/(TP+FN) \qquad (7)$$

And the positive Predictivity:

$$+P = TP/(TP+FP) \qquad (8)$$

in which *TP* is the number of true positive detections, *FN* is the number of false negatives, and *FP* is the number of false positives. The results for using three groups is shown on Table 1 and Figure 4.

These results show that the implemented system, has the correct results with the benefits of parallel calculation and real time measurements of features.

Table 1. Evaluation Results

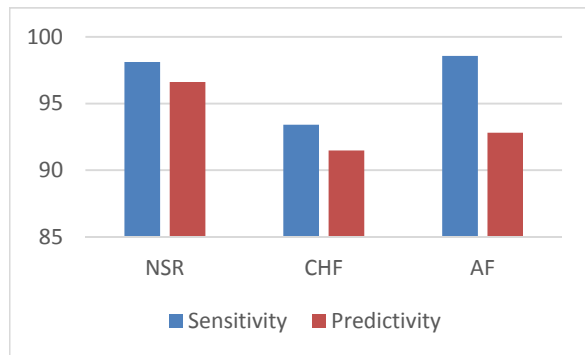| Groups	Sensitivity (Se)	Predictivity ($+P$)
NSR	98.12%	96.62%
CHF	93.41%	91.47%
AF	98.58%	92.81%

Figure 4. Evaluation results.

6.   Discussion

In this paper, we try to develop and implement the HRV signal processing into a Field Programmable Gate Array (FPGA) for extracting this signals feature.

Simulations show that the proposed system is able to achieve appropriate HRV analyses in the hardware. Specially for analyzing nonlinear parameters such as Poincare plot features, it was so useful. This system can be develop and use for more feature extraction by different kinds of analysis on HRV signal. The proposed system is suitable for portable monitoring devices and arrhythmia detection and as a biomedical signal processor on a system-on-chip (SOC) design.

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