HEART2015 Advanced Program

Day 1 : June 1

08:30-16:00	Registration
08:50-09:00	Opening
09:00-10:00	**Keynote Session 1** Session chair: Prof. Miriam Leeser, Northeastern University Accelerating the Data Center Dr. Steven Guccione, Bank of America
10:00-10:30	Coffee/Tea Break
10:30-12:10	**Session 1: Best Paper Candidates** Session chair: Prof. Wim Vanderbauwhede, University of Glasgow ***Off-loading LET generation to PEACH2: A switching hub for high performance GPU clusters*** Chiharu Tsuruta, Yohei Miki, Takuya Kuhara, Masayuki Umemura and Hideharu Amano ***Power Performance Profiling of 3-D Stencil Computation on an FPGA Accelerator for Efficient Pipeline Optimization*** Koji Okina, Rie Soejima, Kota Fukumoto, Yuichiro Shibata and Kiyoshi Oguri ***Understanding Outstanding Memory Request Handling Resources in GPGPUs*** Ahmad Lashgar, Ebad Salehi and Amirali Baniasadi ***A Line Rate Outlier Filtering FPGA NIC using 10GbE Interface*** Ami Hayashi, Yuta Tokusashi and Hiroki Matsutani
12:10-13:30	HEART2015 Lunch (Day 1)
13:30-14:45	**Session 2:** Session chair: Prof. Hideharu Amano, Keio University ***Adapting the DySER Architecture with DSP Blocks as an Overlay for the Xilinx Zynq*** Abhishek Jain, Xiangwei Li, Suhaib Fahmy and Douglas Maskell ***ffLink: A Lightweight High-Performance Open-Source PCI Express Gen3 Interface for Reconfigurable Accelerators*** David Christopher de La Chevallerie, Jens Korinth and Andreas Koch ***A Transfer-Aware Runtime System for Heterogeneous Asynchronous Parallel Execution*** Soukaina Nait Hmid, Jose G.F. Coutinho and Wayne Luk
14:45-15:10	Poster Session 1 & Coffee/Tea Break
16:00-17:00	FPGA Design Contest
19:00-22:00	HEART2015 Banquet (busses leave from Photonics Center 17:45)

Day 2 : June 2

08:00-17:00	Registration
08:00-09:00	Breakfast
09:00-10:00	**Keynote Session 2** Session chair: Prof. Miriam Leeser, Northeastern University Computing in the IoT Era, Opportunities and Challenges Dr. Khaled Benkrid, ARM
10:00-10:45	Coffee/Tea Break
10:45-12:00	**Session 3:** Session chair: Prof. Kentaro Sano, Tohoku University ***Efficient Mapping and Allocation of Execution Units to Task Graphs using an Evolutionary Framework*** Ahmed Al-Wattar, Shawki Areibi and Gary Grewal ***Exploring the Efficiency of the OpenCL Pipe Semantic on an FPGA*** Amir Momeni, Hamed Tabkhi, Yash Ukidave, Gunar Schirner and David Kaeli ***Breadth First Search on Cost-efficient Multi-GPU Systems*** Takuji Mitsuishi, Jun Suzuki, Yuki Hayashi, Masaki Kan and Hideharu Amano
12:00-13:20	HEART2015 Lunch (Day 2)
13:20-14:10	**Session 4:** Session chair: Prof. Wayne Luk, Imperial College London ***Interface Based Memory Synthesis of Image Processing Chains in FPGA*** Michael Mefenza, Nicolas Edwards and Christophe Bobda ***High Throughput Sketch Based Online Heavy Hitter Detection on FPGA*** Da Tong and Viktor Prasanna
14:10-14:35	Poster Session 2 & Coffee/Tea Break
14:35-15:50	**Session 5:** Session chair: Prof. Jason Anderson, University of Toronto ***A Configurable Architecture for Sparse LU Decomposition on Matrices with Arbitrary Patterns*** Xinying Wang, Phillip Jones and Joseph Zambreno ***Stream Computation of Shallow Water Equation Solver for FPGA-based 1D Tsunami Simulation*** Kentaro Sano, Fumiya Kono, Naohito Nakasato, Alexander Vazhenin and Stanislav Sedukhin ***Parallel Genetic Algorithms on Multiple FPGAs*** Liucheng Guo, Andreea-Ingrid Funie, David Thomas, Haohuan Fu and Wayne Luk
15:50-16:05	Closing

Poster Session 1

June 1
14:45-15:10

Programmable Processing Element for Crypto-Systems on FPGAs
Mohamed El Hadedy, Kevin Skadron, Hristina Mihajloska and Danilo Gligoroski

A Hardware-Based Approach for Frequent Itemset Mining in Data Streams
Lazaro Bustio-Martinez, Rene Cumplido, Raudel Hernandez-Leon, Jose Bande-Serrano and Claudia Feregrino-Uribe

A GPU-Based Acceleration Method for Document-Oriented Databases
Shin Morishima and Hiroki Matsutani

Parallel Sparse Coding for Seafloor Image Analysis
Genlang Chen, Chenggang Lai and Miaoqing Huang

Monte Carlo simulation for the first-order Greeks for the Black-Scholes and Heston models using Automatic Differentiation on FPGA
Grzegorz Kozikowski, Erik Vynckier, Xiao-Jun Zeng and John Keane

Poster Session 2

June 2
14:10-14:35

Towards Low-Latency Communication on FPGA Clusters with 3D FFT Case Study
Jiayi Sheng, Chen Yang and Martin Herbordt

Evaluation of different debug approaches in FPGA rapid prototyping
Zdravko Panjkov

A study of a real-time keyword matching process targeting Twitter data
Yusuke Sekihara, Takashi Aoki and Akihiko Miyazaki.

Quality-Scalable Signal Processing via Probabilistic Computing
Mohammed Alawad and Mingjie Lin

An Intermediate Language and Estimator for Automated Design Space Exploration on FPGAs
Syed Waqar Nabi and Wim Vanderbauwhede