Sigma-Delta Based Techniques For Future Multi-Standard Wireless Radios

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To the esteemed reader.

Contents

Abstract

Improvements in process technology and design innovations have resulted in compact and cost effective digital baseband solutions. The radio part, however, has remained a bottleneck in terms of chip area and power consumption as the feature size of analog devices does not directly benefit from scaling. With the addition of yet more standards into emerging products, the requirements of future radios will extend over characteristic performance features into demands of programmable and reconfigurable hardware for radios covering multiple frequency bands. Hence, a guideline in the design of such radios is a large degree of hardware sharing.

The thesis investigates the application of sigma-delta modulation to arising multi-standard wireless radios. First, it reviews principles in wireless radios, such as selected modulation and access techniques. It also examines several communication standards of personal wireless radios as well as common receiver architectures for their implementation. This is followed by general considerations and background information about sigma-delta modulators. In the third and fourth chapter, implementations to two blocks of a wireless radio receiver system are suggested: An architecture for a frequency synthesizer and an implementation of an analog-to-digital converter.

In the first contribution, the thesis develops a novel concept for frequency synthesis that is more suitable for multi-band, multi-standard radio architectures, achieving a large amount of hardware sharing among different wireless standards. As a second pillar, the thesis contributes with the design of a dual-standard sigma-delta modulator for data conversion within a radio receiver. Parts of the work concerning the dual-standard modulator are embodied in a granted swedish patent.

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Relevant Publications

[1] Steffen Albrecht, Adam Strak, Yasuaki Sumi and Mohammed Ismail; "Frequency Detector Analysis for a Wireless LAN Frequency Synthesizer"; IEEJ Analog International VLSI Workshop, Macao; 2004

[2] Steffen Albrecht, "A Frequency-Locked Loop Using Sigma-Delta Modulation", Conference for Design Automation & Test in Europe (DAC), Ph.D.-Forum, Germany; 2003

[3] Steffen Albrecht, Yasuaki Sumi, Mohammed Ismail, and Hannu Tenhunen, "A Frequency Synthesizer Using Frequency Difference Detection", 46th IEEE Midwest Symposium on Circuits and Systems, Cairo, Egypt; 2003

[4] Steffen Albrecht, and Hannu Tenhunen, "A Frequency Synthesizer Architecture for RF Applications", Proceedings of Norchip conference, Riga, Latvia; 2003

[5] Steffen Albrecht, Andreas Gothenberg, Yasuaki Sumi, and Hannu Tenhunen, "A Study of Nonlinearities For a Frequency-Locked Loop Principle", South-West Symposium for Mixed Signal Design (SSMSD), Las Vegas, USA; 2003

[6] Steffen Albrecht, Yasuaki Sumi and Hannu Tenhunen, "A Frequency Synthesizer Principle with Sigma-Delta Loop Filtering", IEEJ International Analog VLSI Workshop, Singapore; 2002

[7] Steffen Albrecht et al., "A Dual-Standard GSM/DECT Baseband Sigma-Delta ADC", NorChip conference, Turku, Finland; 2000

[8] *Steffen Albrecht et al., "A Front-End Receiver Sigma-Delta Modulator", Swedish Patent SE0002065-1, Stockholm; 2000*

[9] *Steffen Albrecht, Xiaopeng Li, Bingxin Li, Costantino Pala, Yonghong Gao, Mohammed Ismail and Hannu Tenhunen, "A Sigma-Delta A/D Based Architecture for Multi-Standard Front-End Radio Receivers", IEEJ International Analog VLSI Workshop, Stockholm, Sweden; 2000*
[This paper received the best paper award at the IEEJ Analog VLSI Workshop]

List of Abbreviations

AC	Alternating Current
ADC	Analogue-to-Digital Converter
AM	Amplitude Modulation
AMPS	Advanced Mobile Phone Service
ASK	Amplitude Shift Keying
BPSK	Binary Phase Shift Keying
CCK	Complementary Code Keying
CDMA	Code Division Multiple Access
CT	Continuous Time
DAC	Digital-to-Analog Converter
DC	Direct Current
DECT	Digital Enhanced Cordless Telecommunications
DNL	Differential Nonlinearity
DR	Dynamic Range
DSP	Digital Signal Processor
DT	Discrete Time
EDGE	Enhanced Data for Global Evolution
ETSI	European Telecommunications Standards Institute
F	Noise Factor
FCC	Federal Communications Commission
FDMA	Frequency Division Multiple Access
f_{FB}	frequency of feedback signal
FHSS	Frequency Hopping Spread Spectrum
FM	Frequency Modulation
f_{REF}	frequency of reference signal

f_s	sampling frequency
FS	Frequency Synthesizer
FSK	Frequency Shift Keying
GFSK	Gaussian Frequency Shift Keying
GMSK	Gaussian minimum Shift Keying
GSM	Global System for Mobile communication
IF	Intermediate Frequency
IMT-2000	International Mobile Communications at 2000 MHz
INL	Integral Nonlinearity
ISM	Industrial, Scientific and Medical (frequency band)
ITU	International Telecommunication Union
MASH	Multi-stAge noise SHaping
NF	Noise Figure
NMT	Nordic Mobile Telephone
NTF	Noise Transfer Function
OFDM	Orthogonal Frequency Division Multiple access
OSR	OverSampling Ratio
OTA	Operational Transconductance Amplifier
PA	Power Amplifier
PDC	Personal Digital Cellular
PHS	Personal Handyphone System
PM	Phase Modulation
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quaternary Phase Shift Keying
RF	Radio Frequency
ROM	Read Only Memory

ΣΔ	Sigma-Delta
SC	Switched Capacitor
SNDR	Signal-to-Noise plus Distortion Ratio
SNR	Signal-to-Noise Ratio
SOI	Silicon On Insulator
SQNR	Signal-to-Quantization Noise Ratio
STF	Signal Transfer Function
TACS	Total Access Communication System
TDMA	Time Division Multiple Access
UMTS	Universal Mobile Telecommunications System
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network

1. Introduction

This chapter will first give a brief historical review on wireless communications and mention the motivation for this work. Then, principles of selected modulation and access techniques employed in today's radio communication are examined. The impact of modulation schemes on the requirements of utilized hardware is viewed upon. Secondly, several communication standards are compared with respect to application area and performance parameters. The third section describes radio architectures, typically found in today's radio communication.

1.1 A Brief History of Communication

Before stepping into principles and standards of radio communication, this section will glance over a few important milestones in the development of information transmission. This review is of course by no means complete, as this is not the scope of this thesis, nor is it intended to be encyclopaedically. May the inventors of past and present excuse, if they have been left out here.

Today's accessibility of communication around the globe using telephones, fax, radio and television, internet connections, mobile phones at relatively low costs is a matter of course. However, this development has been a long process. Transmission of information, i.e. the desired data, over distance to a receiving instance has always played a large role in human life. Without it, human interaction and coordination or imparting of knowledge would not have be possible. Before an automated procedure for a transmission was invented, messages had to be carried from a sender to the destination: Afoot or mounted, oral or written, crypted or plain; using letters, smoke, trumpets or flags. Limits in number of symbols, transmission distance and speed made these transmissions time consuming or complicated.

In the beginning of the 18th century, during the French revolution, Claude Chappe, a former priest, built a mechanical-optical communication device, a so called semaphore telegraph (figure 1.1). It was first used in 1794 and consisted of 15 repeating stations in a line of sight, linking the cities Lille and Paris [Chapp1794]. The distance of about 200 km could be covered in a few minutes what used to be many hours for a mounted courier. A technology that proved critical for an aspiring France. Other telegraph systems had also been tested before, but Chappe was presumably the first who constructed an applicable and mechanical, wireless communication system.

The invention of the galvanometer by Johann Schweigger and the work on electromagnetism by people like Hans Christian Oerstedt, André Marie Ampère, William Sturgon and Michael Faraday in the 1820's laid the basics for Joseph Henry's principle of telegraphing [Henry1831]. This principle was later used in the development of a long distance telegraph communication system like the ones by Wheatstone and Cooke [Wheat1837] and by Samuel F.B. Morse [Morse1840]. In 1876, Elisha Gray and Alexander Graham Bell developed a device that transmitted speech electrically [Bell1876]; the telephone was invented. Although communication was bound to wires, both telephone and telegraph provided fast and reliable means of communication of both text and sounds, and their technological successors are still in use today.

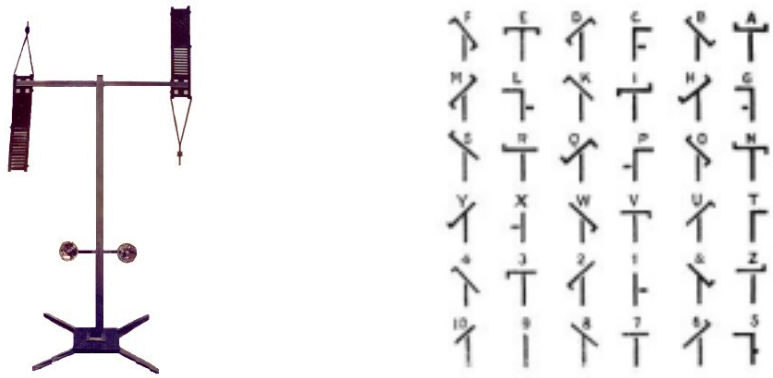


Figure 1.1: Claude Chappes optical telegraph and part of his signal transmission code.

The physicist Heinrich Rudolf Hertz extended Maxwells ideas on electromagnetic waves. He proved the physical existence of radio waves experimentally [Hertz1892]. The path was open for the wireless telegraph and the radio. Physicist Nikola Tesla is credited with the invention of modern radio [Tesla1897]. He obtained more than 100 patents in the areas of motors/generators, transformers, lightning, radio, engines and other areas. In the dawn of a new century, Guglielmo Marconi, an italian inventor, built a first practical radio communication link in England [Marco1900]. The first transatlantic wireless transmission of Morse code followed in 1901. With the development of the audion tube by De'Forest [DeFor1906], radio waves could be amplified, which enabled the advance of wireless telephony. Military and enterprise interests pushed for improvements in radio communications. Commercial radio and first television broadcasting started in the 1920's, radar detection was fit for service in 1936. With the invention of the transistor by Shockley, Brattain and Bardeen in 1947 and the advance into integrated circuits, [Kilby1959] and [Noyce1959], the area of smaller, lighter and more powerful radios began. Mobile, hand held terminals became available and cellu-

lar radio communication systems were developed. The first commercial cellular phone system was in operation in Tokyo in 1979.

1.2 Motivation of this work

With communication technology developing in different parts of the world and driven by different economic interests, naturally, a large variety of communication methods matured. Today's frequency spectrum is crowded by a large number of applications. The same method might occupy different bands in different countries. With numerous standards defined for wireless communication, the need for interoperability between various technologies arises. Mobile terminals such as phones, PDAs or notebooks gain seamless access to a multitude of available services. This in turn reduces the number of devices and increases user-friendliness. But interoperability comes at the expense of added complexity. Powerful signal processing is accomplished using programmable DSPs. However, radio interface specifications vary considerably and transceiver hardware is typically optimised for a specific standard.

An evolutionary trend for transceivers is therefore not only towards higher data rates. Also integration of several radio interfaces into one programmable and reconfigurable hardware supporting multiple standards and multiple frequency bands becomes important. Although accommodating several individual, optimised transceivers into one terminal already enables multi-standard operation, it would cause larger implementation costs, higher power consumption and bulkier terminal size.

Due to advances in manufacturing, feature size, speed and area usage of integrated structures improve continuously. An estimation for this development was first given by Gorden Moore in [Moore1965]. The advance of recent processes can be followed from the International Technology Roadmap for Semiconductors [ITRS04] or relevant internet publications from manufacturing companies. However, the mentioned improvements mainly benefit digital processing. Area, size and power reduction of analog circuits is limited by different noise sources.

The work presented in this thesis targets the above mentioned objective of increased flexibility to reduce implementation costs and to add functionality. Multi-standard and multi-band operation is achieved by making use of digital processing and configurability.

1.3 Wireless Radio Principles & Standards

A wireless transmission does not necessarily have to be a radio connection. For instance, Chappes telegraph system [Chapp1794] used a combination of optical and mechanical means, a connection without wires. Also, capacitive or inductive crosstalk is a wireless connection, but does not constitute radio communication. For the scope of this thesis, radio communication is referred to as the transmission, emission and reception of information (signs, symbols, images, sound or data) by means of modulated electromagnetic waves. A generalized block diagram of a wireless radio communication system is shown in figure 1.2. Information from the source, e.g. a baseband signal, is modulated with and frequency translated onto electromagnetic carrier waves in the transmitter prior to emission from an antenna. These waves travel through the channel medium and are then received at another antenna. The receiver detects and demodulates the information before handing it over to its destination. During transmission, propagation loss, multipath fading, delay differences and interferences from other communications affect the quality of the signal depending on the used frequency band and the application environment. More details on disturbances of radio communication channels can be found in e.g. [Rappa1996].

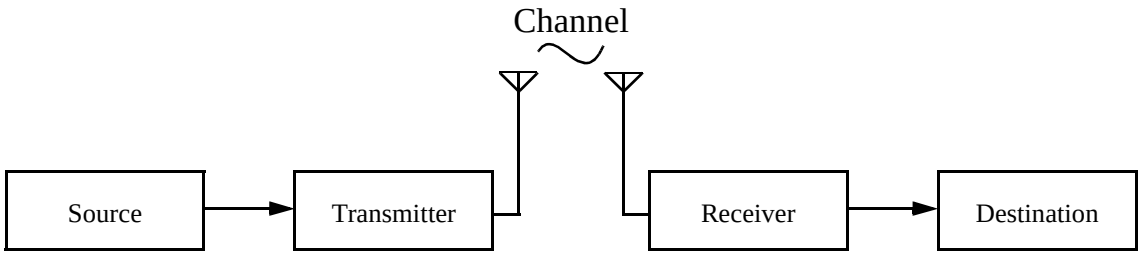


Figure 1.2: Block diagram of a general radio communication system.

1.3.1 Modulation

Modulation and demodulation are essential functions in wireless radio communication systems. Modulation improves transmission, reception and detection properties in the presence of noise within the transmission channel. It also adds to security of data transmission. Important attributes of modulation and demodulation are signal transmission quality, spectral efficiency and power efficiency. Local and international authorities regulate and limit frequency bands for communication. Hence, the same application might occupy different bands in other countries, i.e. requiring a different carrier signal. Different communication standards employ different modulation tech-

niques, for reasons of required bit rate, application area or noise impact to the air interface.

The transmission quality can be quantified with parameters like Signal-to-Noise Ratio (SNR) for analog or audible applications, or with the Bit Error Rate (BER) for digital and data transmission. SNR expresses the ratio of signal power to noise power that is present during communication. The BER, on the other hand, states the ratio of bits that were received erroneously to the total number of transmitted bits within a certain time frame. Hence, it is a measure of how many bits have to be resent to complete the information transfer. A higher transmission quality allows to lower the transmission energy for the same distance and increases battery life. Alternatively, the signals could be transferred over larger distances. Spectral efficiency expresses the ratio of channel throughput to the required radio spectrum. More complex modulation techniques combine several bits into symbols that are transmitted within the same or a smaller spectrum. If the amplitude envelope of a signal becomes variable due to modulation, then the power amplifier (PA) needs to provide amplification with higher linearity. Otherwise, the signal will experience spectral regrowth, causing lower spectral efficiency and energy leakage into adjacent channels [Morai1980], [Sevic1996]. However, highly linear PAs have considerably lower power efficiency. Hence, modulation scheme requirements for spectral efficiency and power efficiency have to be traded off.

The basis of modulation is the variation of a carrier by a baseband signal. This carrier, e.g. a sinusoid, can be modulated by both, amplitude and phase. This converts the baseband signal to the passband. A passband signal can be described as

$$x_C(t) = a(t) \cdot \cos(\omega_C t + \phi(t)) \tag{1.1}$$

where ω_c is the carrier frequency and $a(t)$ and $\phi(t)$ are the amplitude and phase of the carrier signal, that vary proportionally with the baseband signal. In analog modulation, the carrier is modulated by an analog baseband signal. When varying $a(t)$, $\phi(t)$, or $d\phi/dt$, the scheme is called amplitude (AM), phase (PM), or frequency modulation (FM), respectively. AM is more susceptible to noise and interferences and requires linear power amplifiers. PM and FM carry the baseband information in the phase or frequency instead. Hence, the carrier envelope is constant, leading to lower linearity requirements for the PA.

Modern modulation schemes employ digital baseband signals for carrier alteration. Digital modulation offers higher resilience to noise or multi-path effects, increases quality of communication and spectral efficiency, and brings better compatibility with digital services. Data security is improved and modern, powerful digital signal processors (DSPs) can be employed for complex modulation schemes. Similar to analog

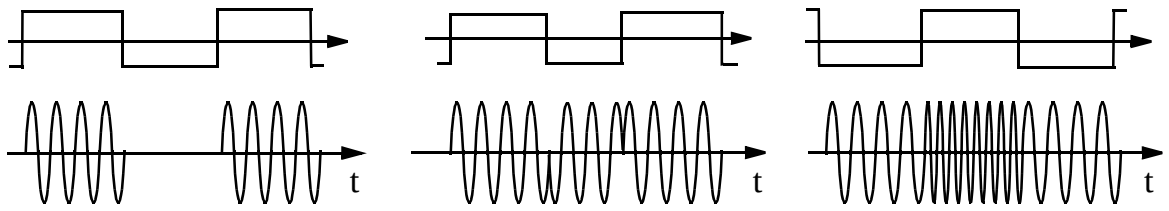
modulation, the schemes are called Amplitude Shift Keying (ASK), Phase Shift Keying (PSK) and Frequency Shift Keying (FSK). Their principles are depicted in figure 1.3(a-c) for the case of binary modulation. A general expression of the digital baseband signal $x_{bb}(t)$ is

$$x_{bb}(t) = \sum_n b_n \Pi(t - nT_b) \tag{1.2}$$

with b_n being the bit values and $\Pi(t\text{-}nT_b)$ the pulse function of interval T_b. The number of discrete values of b_n defines the levels of modulation, for instance [-1, 1] or [0, 1] for binary modulation. Each digitally modulated waveform *x(t)* can be expressed as a linear combination of basis functions:

$$x(t) = \alpha_1 \cdot \Psi_1 + \alpha_2 \cdot \Psi_2 + \ldots + \alpha_m \cdot \Psi_m \tag{1.3}$$

where the Ψ_j are the orthogonal basis functions and the α_j are their parameters that were modified by $x_{bb}(t)$, respectively. For m = {1, 2, 3}, the symbols of x(t) in equation (1.3) can be represented graphically. Such representations are called signal constellations. The larger the geometrical distance between the symbols, the lower the probability of detecting a wrong symbol.



a) ASK b) BPSK c) BFSK

Figure 1.3: (a) Amplitude, (b) Phase, and (c) Frequency shift keying for modulation with binary base band signals (shown above)

ASK encodes information in the amplitude of one carrier. In binary signalling, the carrier can simply be switched either on or off. ASK offers low circuit complexity, but suffers from signal quality loss due to higher sensitivity to amplitude noise during transmission than PSK and FSK. It is therefore not often used in digital radio communications [Razav1998]. Since there is only one basis function, Ψ_1, the signal constellation is one dimensional, as shown in figure 1.4a. The modulated signal x(t) of equation (1.3) is described with $\alpha_1 = \{0, A_c\}$ and $\Psi_1 = \cos(\omega_c t)$, with A_c being the car-

rier amplitude and ω_c the carrier frequency, respectively. Phase and frequency shift mechanisms are much less susceptible to amplitude variations, and are hence most often used for wireless radio transmission. In PSK, information is coded in the phase of the carrier. Figure 1.3b and figure 1.4b show the time domain diagram and signal constellation for the binary case, i.e. BPSK. The modulated signal x(t) can be described with $x(t) = A_c \cdot \cos(\omega_c t + \phi)$, where the phase ϕ can take the values 0 or 180 degree. The constellation now comprises a single carrier, $\Psi_1 = \cos(\omega_c t)$, and two amplitudes $\alpha_1 = \{-A_c, A_c\}$. The symbol distance is now twice as large as for binary ASK, which means lower detection error probability. When using coherent detection, phase synchronisation is required between the received carrier and the receiver oscillator.

In frequency shift keying, different symbols are encrypted with frequencies. This principle is illustrated in figure 1.3c. In binary FSK (BFSK), the baseband signal selects one of two carriers with equal amplitudes. Hence, the signal x(t) has two basis functions: $\Psi_1 = \cos(\omega_{c1} t)$ and $\Psi_2 = \cos(\omega_{c2} t)$. The two carrier frequencies are ω_{c1} and ω_{c2}, and $[\alpha_1\ \alpha_2] = \{[0\ A_c], [A_c\ 0]\}$ are the amplitude values. The constellation of BFSK is shown in figure 1.4c. It can be seen that the symbol distance is reduced by a factor of $\sqrt{2}$ with respect to BPSK. Hence, the probability of detecting a symbol erroneously is increased. Also in frequency shift keying modulation, phase synchronization is required if coherent detection is used. Despite the higher error probability, BFSK enables simpler detection schemes and better power efficiency [Razav1998].

In binary modulation, one symbol representing a binary value is modulated onto one carrier signal. Higher data rates can be obtained by multiplexing more symbols onto a single carrier. For instance, pairs of two bits $[b_0\ b_1] = \{[00], [01], [10], [11]\}$ can be mapped to one out of four symbols, say [a b c d]. This requires x(t) of equation (1.3) to have two basis functions, Ψ_1 and Ψ_2, that are orthogonal with respect to each other. Such modulation scheme is called quadrature modulation. If the phase of the basis signals is modulated, the scheme is called quadrature phase shift keying (QPSK). Equation (1.3) becomes $x(t) = \alpha_1 \cdot \cos(\omega_c t) + \alpha_2 \cdot \sin(\omega_c t)$, with $[\alpha_1\ \alpha_2] = [\pm A_c\ \pm A_c]$. As two bits comprise one new symbol, the symbol rate is half the bit data rate. Hence, the required bandwidth for the same data stream is reduced by a factor of two with respect to BPSK. Alternatively, twice as much data could be send. The signal constellation for QPSK is shown in figure 1.4d. Variations of quadrature modulation are for instance offset-QPSK (O-QPSK), $\pi/4$-QPSK and Mean Shift Keying (MSK). These techniques introduce time offsets, phase rotation, or smooth phase transitions to improve spectral or power efficiency. The higher data rate of QPSK comes at the expense of higher detection complexity.

The signal amplitudes in PSK modulation schemes are constant. A combination of phase shifts and amplitude variations allows for a higher level of modulation, for in-

stance in Quadrature Amplitude Modulation (QAM). Each out of *M* possible symbols represents *m* bits, with $m = \log_2(M)$. When modulated with QAM, the signal of equation (1.3) becomes $x(t) = \alpha_1 \cdot \cos(\omega_c t) + \alpha_2 \cdot \sin(\omega_c t)$, where $\alpha_1 = [\pm A_1, \ldots, \pm A_k]$ and $\alpha_2 = [\pm A_1, \ldots, \pm A_k]$ are the *k* amplitudes of each basis function.

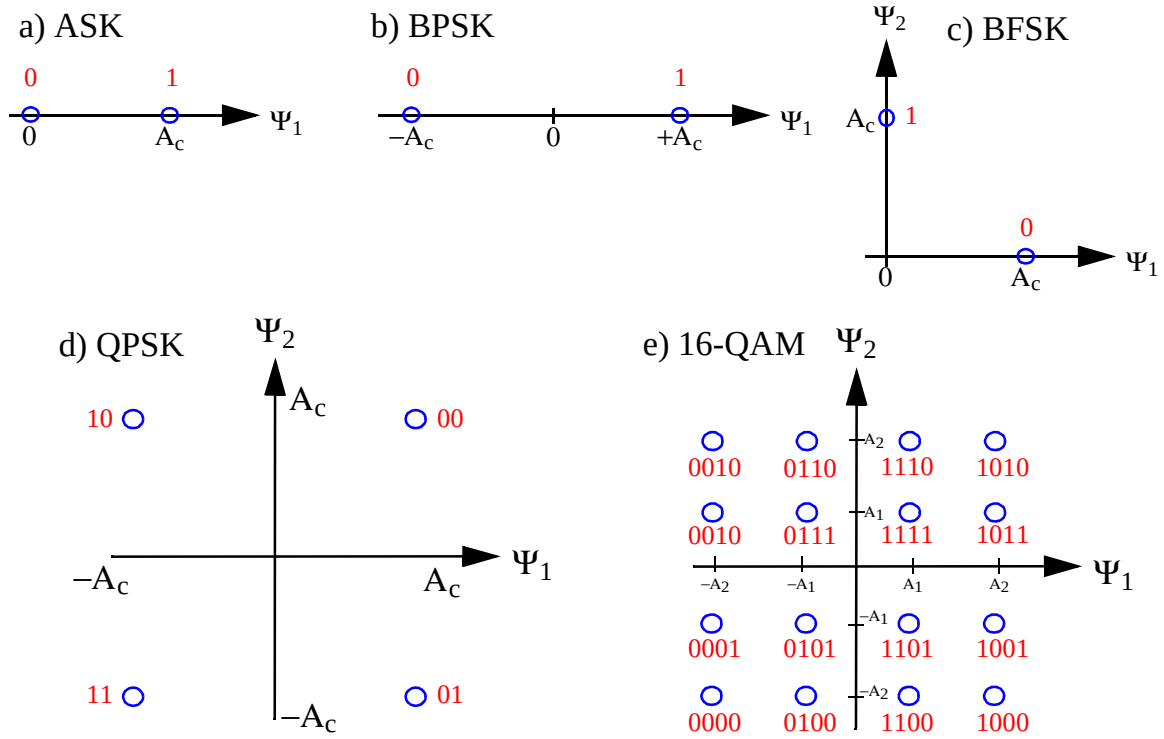


Figure 1.4: Signal constellation for (a) ASK; (b) BPSK; (c) BFSK; (d) QPSK; and (e) 16-QAM. The digital numerals represent the modulated symbols.

The constellation of 16-QAM is shown in figure 1.4e. The modulation accuracy and quality of the transmitted QAM signal can be expressed with the error vector magnitude (EVM). EVM represents the vector distance between ideal and measured symbol in a QAM constellation. As with the techniques mentioned above, more symbols give higher data rates, and hence, better spectral efficiency. But it also increases amplitude and phase noise performance requirements of the (de)modulating circuitry. Increased symbol energy can only partly improve transmission quality, as regulations on maximum transmit power limit this option. Therefore, power and bandwidth efficiency need to be traded off. More detailed discussions on digital modulation schemes can be found e.g. in [Couch1993], [Feher1995], [Proak1989], and [Rappa1996].

Coherent detection requires phase synchronization between transmitter and receiver. This phase information is usually obtained from training sequences carried in pilot signals. However, in the presence of strong interferences and low signal levels, phase recovery becomes difficult. Alternatively, noncoherent detection schemes can be employed. For instance, differential phase shift keying (DPSK) does not require phase alignments, as information lies within the phase change from one symbol relative to the previous one, not in absolute phase values. Only an extra starting bit prior to the first transmitted symbol is required for correct interpretation of the symbol sequence. Symbols modulated with noncoherent FSK are detected with bandpass filters (to determine if the wanted frequency component is present) and envelope detectors instead of correlation filters. The error performance of noncoherent modulation is slightly worse than for coherent systems. However, reduced complexity and robustness to interference make these modulation schemes attractive [Burr1992], [Colav1999], [Razav1998].

1.3.2 Access Techniques

Access techniques regulate the management of available communication channels and allocate connections to the users. Multiple access techniques permit that many users simultaneously access the same fixed bandwidth. A selection of methods employed in todays radio communications are described here.

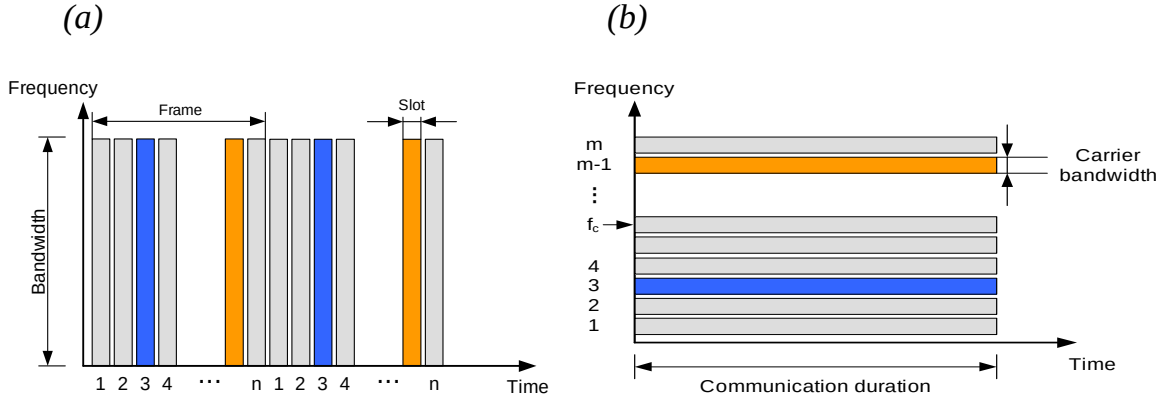


Figure 1.5: Channel definitions for (a) TDMA for n channels, and (b) FDMA for m channels

In Time Division Multiple Access (TDMA), a time frame is split into several fractions, so called slots [figure 1.5(a)]. Signals are transmitted for the duration of one time slot within the frame. Hence, the number of physical channels corresponds to the number of time slots. Different users can be assigned to these slots which makes it pos-

sible to transmit signals from several users within one time frame. The data is buffered and transmitted at a high rate. Each time slot uses the whole assigned frequency band. The receiver decompresses the signal to its original timing schedule, so that its output is a seemingly continuous stream. Due to buffering and synchronisation, TDMA cannot send analog data directly and is used only for digital communication.

In Frequency Division Multiple Access (FDMA), the available spectrum is divided into several narrower bands [figure 1.5(b)]. A physical channel is now such narrow band, e.g. 30 kHz, with a carrier frequency, f_c, at the channel centre. The transmission is continuous, i.e. is suitable for analog signals. Each user is assigned to one carrier for receiving and for transmission to achieve simultaneous access. Hence, the number of signals that can be transmitted corresponds to the number of carriers, and no additional synchronisation data is needed. To increase the number of users, the available spectrum can be divided into more, narrower bands. However, the modulation technique defines the minimum carrier spacing. In a hybrid FDMA/TDMA system, both access methods are combined. For each carrier with its bandwidth, the time frame is separated into several slots. A physical channel corresponds to a time slot within one carrier.

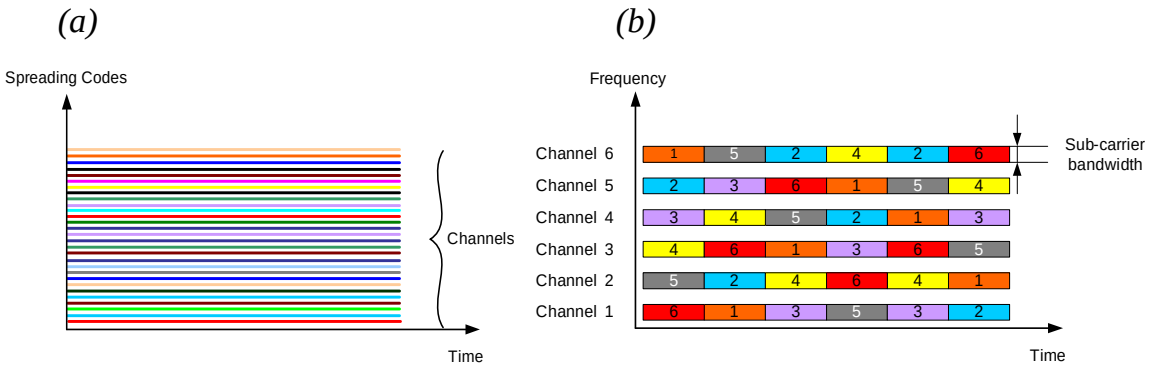


Figure 1.6: Channel definitions for spread spectrum applications: (a) DSSS, and (b) FHSS

Code Division Multiple Access (CDMA) is a technique where many users use the whole assigned spectrum and transmit simultaneously. Two different techniques to spread the bandwidth of the original data signal are used. In Direct Sequence Spread Spectrum, DSSS or DS-CDMA, each data signal is assigned a pseudo random noise code (thereof the name ‘code’ division). This canalization or spreading code is a sequence of binary symbols (chips) and each code corresponds to a physical channel. For each successive connection, the spreading code changes. The required bandwidth for transmission is much larger than the bandwidth of the original signal. To send one bit of information, e.g. a “1”, the whole code sequence is sent. To send a “0”, the complement of the code is sent. After spreading, the signal is modulated to the RF band. Since

the signal is coded, the receiver cannot distinguish certain time slots or carriers. The receiver input contains small parts of all signals at each instant of time. The received signal is first down-converted from RF before it is recovered by correlation with the same spreading code as in the transmitter. A second technique used to spread the data bandwidth is Frequency Hopping Spread Spectrum, FHSS or FH-CDMA. The RF spectrum is divided into a larger number of sub-carriers and the transmitted signal switches rapidly between different carriers in a predetermined, pseudo random sequence. The receiver has to know beforehand where to find the signal at any given time. To cause interference, another transmitter has to send at the same time at the same sub-carrier. The channel definitions are depicted in figure 1.6.

CDMA offers a high immunity to interferences during transmission because the signal energy is spread over a large bandwidth. The effect of band spreading is depicted in figure 1.7. The larger the processing gain, i.e. the ratio of the spread bandwidth to the original data bandwidth, the higher the interference immunity. Longer spreading codes increase the processing gain and improve the system transmission rate. If too many signals are sent out simultaneously by different stations, the bit error rate increases due to intersymbol interference. Hence, the channel capacity in DS-CDMA is defined as the highest number of codes that are used simultaneously while keeping a defined bit error rate of the receiver.

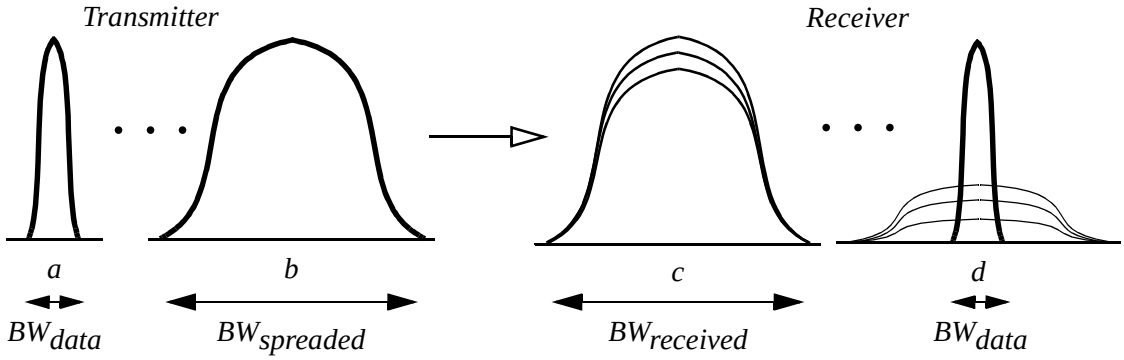


Figure 1.7: CDMA spectra: (a) original data, (b) spread spectrum after modulation with PN code, (c) received spectrum containing noise and interference, and (d) de-spread signal.

Orthogonal Frequency Division Multiplexing (OFDM) resembles FDMA, but provides several sub-carriers for each channel in the band [figure 1.8]. The sub-carriers are orthogonal to one another, so they can be placed close together in the band without causing interference. A high data rate bit stream is converted into n parallel low rate bit streams. Each parallel bit stream is then modulated on a sub-carrier, where each carrier modulation can be different (BPSK, QPSK or QAM). To get a higher bandwidth

efficiency, the sub-carriers are overlapping. The symbol rate in each carrier is low, so intersymbol interference occurs only for large delay spreads. This gives higher tolerance to multipath delay spread and fading. However, challenges of OFDM are for instance sensitivity to frequency offsets, oscillator phase noise and the more complicated design of (de)modulation circuitry.

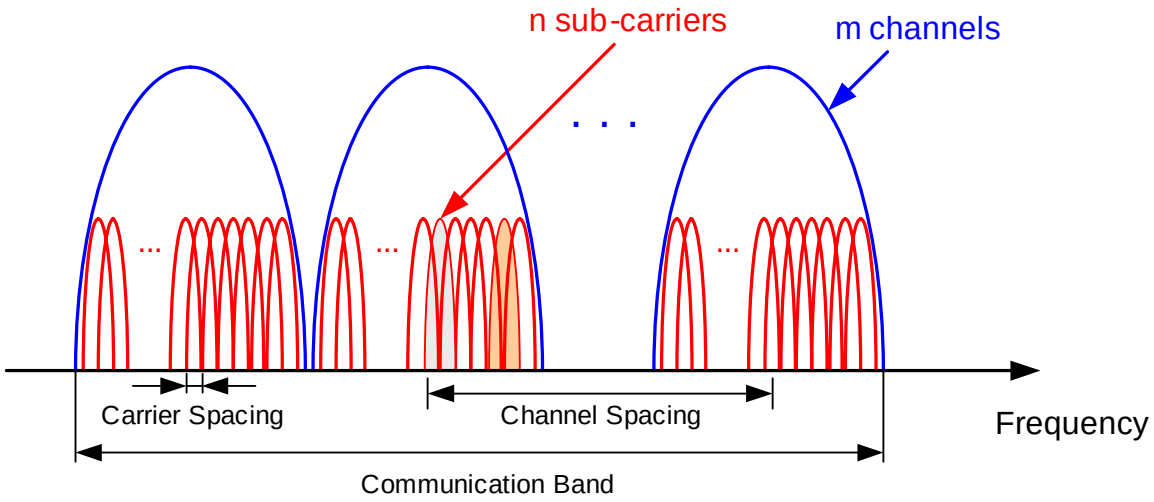


Figure 1.8: Channel and carrier definitions for Orthogonal Frequency Division Multiplexing

1.3.3 Wireless Communication Standards

For any wireless communication to function, both transmitter and receiver shown in figure 1.2 have to comply to the same frequency band, method of modulation, and access technique. For this reason, communication standards are defined. The standards mentioned below represent only a small selection of the range of existing radio communication systems.

Since the spectra for wireless services are limited, frequency resources have to be shared to ensure service to a large number of customers. Here, radio communication lends a principle from radio and TV broadcast. If two senders are positioned at a sufficiently long distance from each other, their signals have only negligible interference. Hence, they can use the same frequency band for transmission. This frequency reuse principle is commonly extended into a cellular system, as depicted in figure 1.9 for the example with 7 adjacent cells. Each neighbouring cell operates in a different frequency band. Users within a cell are served by one base station until leaving the cell. Then, communication is handed off to the nearest base station with the help of a mobile telephone switching office (MTSO).

Technologies that make extensive use of this cellular approach are for instance personal wireless phone systems. Though already available in the 1940's, technical and administrative restrictions delayed its advance until the late 1970's and early 1980's. Today termed as analog, or first generation wireless telephone, systems like the scandinavian Nordic Mobile Telephone (NMT) and the german C-Netz commenced operation in 1981.

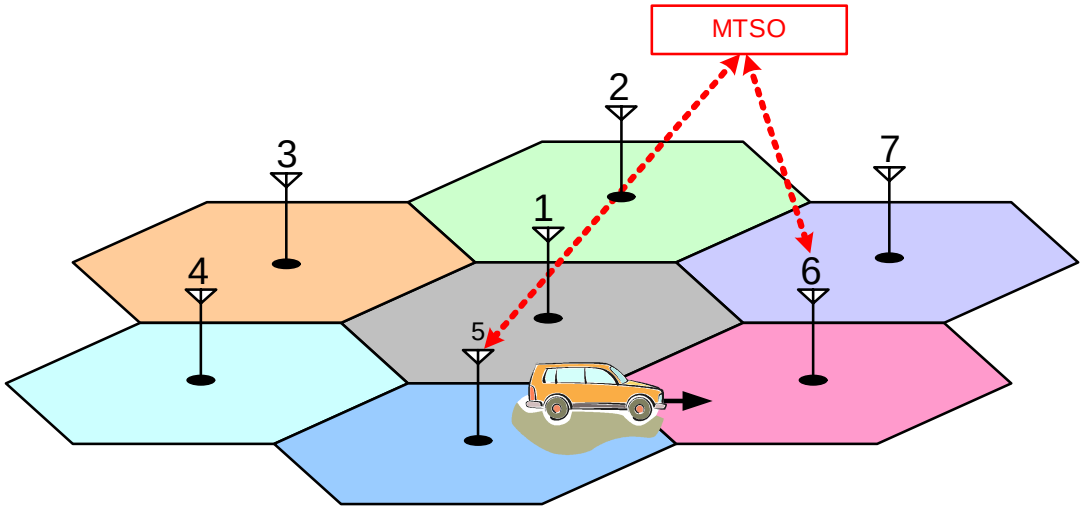


Figure 1.9: A 7 cell system for personal communication systems with handoff by an MTSO.

Also, the Advanced Mobile Phone Service (AMPS) and Total Access Communication System (TACS) were operational in 1983 and 1985, respectively. Second generation systems employing digital modulation schemes offered increased data rates, better quality and new types of communication. The Global System for Mobile communication (GSM) became a unified standard for Europe and many other countries. Corresponding systems in the US are based on standards IS-54/IS-136 and IS-95. In either case, the number of subscribers quickly exceeded channel capabilities, so that additional frequency bands were needed. Whereas first generation systems allowed roaming only on a national or bilateral basis, communication standards are largely unified for second generation on a more continental basis. However, roaming with one device on different continents requires multiple transceiver interfaces to be included in the mobile terminal, increasing costs and weight. Wireless communication of the third generation aims for wider roaming services as well as new applications due to higher data rates and more effective use of the available spectrum. Besides improved voice communication, third generation services include transmission of data, video, and internet access, all at reduced costs for subscribers. The standard International Mobile Telecommunications-2000 (IMT-2000) comprises several individual standards, e.g.

Universal Mobile Telecommunication System (UMTS), CDMA2000, Enhanced Data rate for Global Evolution (EDGE), and Digital Enhanced Cordless Telecommunications (DECT). Though IMT-2000 greatly improves roaming capabilities, there is yet no single worldwide standard.

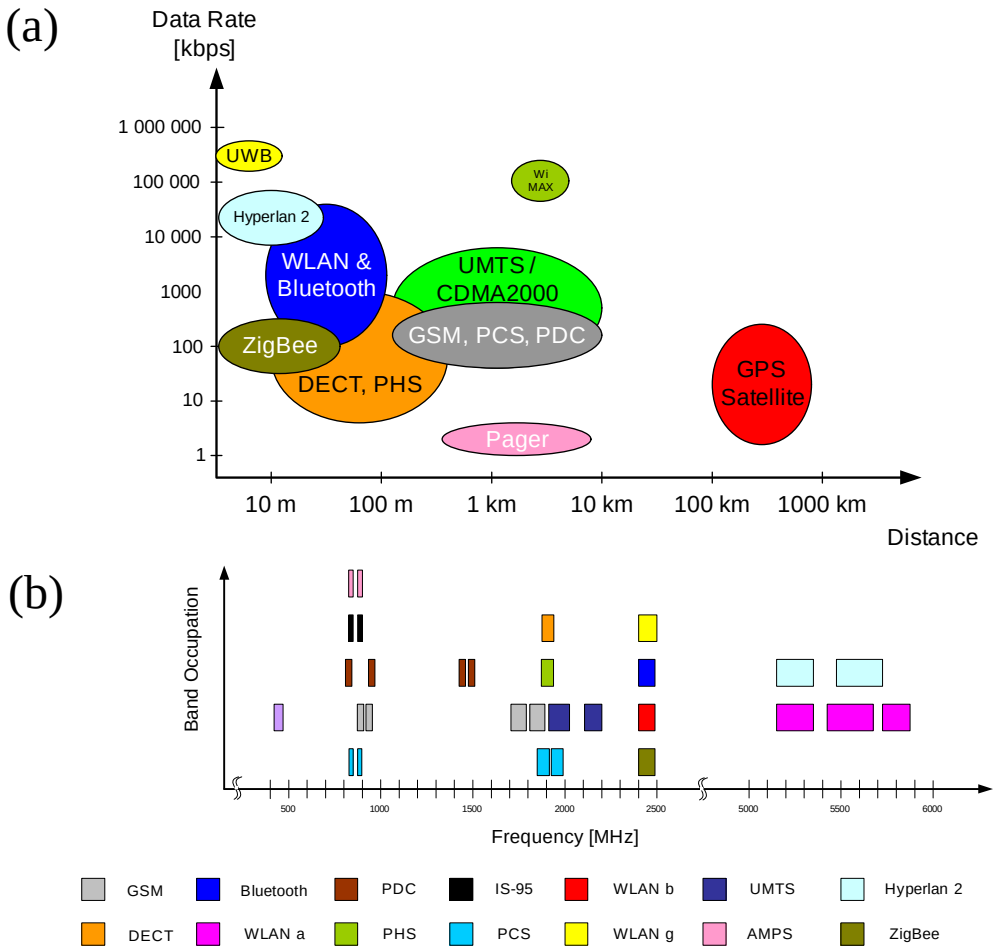


Figure 1.10: (a) Data rate versus cell size for selected wireless standards; (b) Band occupation for selected standards of Table .

Whereas wireless phone systems aim for long distance connections with relatively low data rate, other applications like wireless local area network (WLAN) services, Ultra Wide Band (UWB) or HiperLan target transmission of large amount of data over shorter distances. Additionally, short distance, low data rate applications for very low costs (e.g. ZigBee) and large data rate, long distance (e.g. WiMAX) systems are available. Figure 1.10 shows an overview of selected standards with relevant data rates versus applicable cell sizes as well as their band occupation. Table 1 compares access

technologies, modulation schemes and other parameters of radio interfaces for various mobile communication standards.

Table 1: Overview for selected mobile communication standards[a]

Standard	Frequency Bands (MHz)[b]	Data Rate (air interface)	Access	Modulation	No. of Channels	No. of Carriers	Spacing
AMPS	824 - 849 869 - 894	10 kbps	FDD	FM	1	832	30 kHz
PCS (IS-54 / IS-136)	824 - 849 869 - 894 1850-1910 1930-1990	48 kbps	TDMA/ FDD	DQPSK	3	832	30 kHz
IS-95	824-849 869-894	1.2288 Mbps	DS-CDMA	QPSK, O-QPSK	256	1	1.25 MHz
GSM	890-915 935-960 1710-1785 1805-1880	270 kbps	FDMA/TDMA FDD	GMSK	8	124	200 kHz
PDC	810-826 940-956 1429-1453 1477-1501	42 kbps	TDMA	DQPSK	3	640	25 kHz
DECT	1880-1930	1.152 Mbps	TDMA/TDD	GFSK	12	10	1.728 MHz
PHS	1895-1918.1	384 kbps	TDMA/TDD	DQPSK	4	77	300 kHz
Bluetooth	2400-2483.5	1 Mbps	FH-CDMA TDD	GFSK	79	79	1 MHz
UMTS/WCDMA[c]	1900 - 2025 2110 - 2200	3.84 Mbps	DS-CDMA	QPSK	4...256	1	5 MHz
CDMA-2000	422.5-457.475 462.5-467.475	1.2288 Mbps 3.6864 Mbps	DS-CDMA	QPSK/BPSK	4...128 4...256	1 3	1.25 MHz
WLAN 802.11a	5150-5350 5425-5675 5725-5875	54 Mbps	OFDM	BPSK, QPSK, 16/64 QAM	12	52	20 MHz
WLAN 802.11b	2400-2484	11 Mbps	DS-CDMA	CCK	13	13	5 MHz
WLAN 802.11g	2400-2497	54 Mbps	OFDM	BPSK/QPSK CCK	12	52	30 MHz
Hiperlan 2	5150-5350 5470-5725	54 Mbps	OFDM	BPSK/QPSK 16/64 QAM	5	52	20 MHz
802.15.4 (ZigBee)	868.0-868.6 902.0-928.0 2400-2483.5	20 kbps 40 kbps 250 kbps	DS-CDMA	BPSK BPSK OQPSK	1 10 16	3	– 2 MHz 5 MHz
UWB[d]	3100-10600	480 Mbps	OFDM	QPSK	255	3	528 MHz

a. References: [IEEE1999a], [IEEE1999b], [IEEE2003a], [IEEE2003b], [IEEE2003c], [Holma2001], [ETSI2001], [MBOA2004], [Goodm1997]
b. The lower bands correspond to uplink, higher bands to downlink connections.
c. Spectrum according to IMT-2000, including bands for satellite, licensed and nonlicended bands.
d. Standardization in progress.

1.4 Radio Receiver Architectures

In wireless radio communication, all signals are transmitted as electromagnetic waves, occupying the same transmission medium. Receiver and transmitter shown in figure 1.2 perform different tasks. Receivers need to select a desired, narrow channel from a broad spectrum that is supplied by the antenna. The task of a transmitter is to convert a given baseband signal of limited bandwidth to RF and transmit it to the antenna with adequate output power without disturbing neighbouring channels. Hence, design challenges for both parts differ. The most important characteristics of a receiver are its sensitivity and selectivity. Sensitivity expresses the level of the smallest possible input signal that can still be detected correctly (i.e. within a given BER). Selectivity, on the other hand, describes the receivers ability to detect a weak desired signal in the presence of strong adjacent channels, so called interferers. These interferers are sometimes also called blockers that desensitize the receiver. Important characteristics of transmitters are power efficiency, antenna insertion loss and linearity, as nonlinear products create interferers in neighbouring channels. The following section reviews receiver architectures that are commonly employed in modern radio communication systems.

Radio communication systems operate typically with carrier frequencies at many hundreds of MHz to several GHz. Directly converting the antenna signals to digital form in an integrated ADC would require prohibitively large sensitivity, selectivity, linearity, and very high conversion speed. As of today, such analog-to-digital converters do not exist. Therefore, the received RF signals have to be converted to lower frequencies, for signal processing steps like channels selection and amplification. This conversion is accomplished in a mixing process, producing a downconverted (used in receiver) and an upconverted (used in transmitter) component. Low- or high-pass filtering then selects the desired band. However, mixing includes two inherent sources of problems. First, nonlinearities generate many other signal components, e.g. harmonics and intermodulation products, which distort desired information. The second problem is that of images. Interferers that are present at frequencies symmetrical from the desired band to the local oscillator (LO) are mixed into the same target band as the desired channel. This corrupts the signal and degrades the receiver sensitivity. A larger difference between RF and LO signal allows for a simpler image rejection filter. But it also raises the intermediate frequency (IF), making channel selection with practical on-chip filters more difficult. Hence, there is a design trade-off between sensitivity and selectivity. The architectures described below display different design challenges, e.g. capability for monolithic integration, sensitivity/selectivity trade-off, linearity, and power consumption.

Heterodyne Receiver

Conventional radio transceivers utilize the so called heterodyne architecture (hetero = different, dyne = mix). This architecture, introduced first by [Armst1918], usually has two or more stages for frequency conversion. An example is shown in figure 1.11. A passive bandpass filter limits the input spectrum provided by the antenna. Due to noise introduced in the mixer, the signal is first amplified in a low noise amplifier (LNA). Interferers at frequencies symmetrically with f_{IF} to the local oscillator (LO) signal will create images during mixing. Hence, these bands have to be removed by an image reject filter first. For that, the signal goes off-chip into an image rejection (IR) filter using passives with high quality factor. Then, mixing with a tunable LO signal at RF downconverts the selected channel to IF. This LO_1 output needs to be variable in small frequency steps for narrow band selection. To alleviate the aforementioned sensitivity-selectivity trade-off in image rejection, an off-chip, high-Q bandpass filter performs partial channel filtering at a relatively high intermediate frequency. A second downconversion mixing step translates the signal down to baseband and further reduces the requirements for the final, integrated channel selection filter.

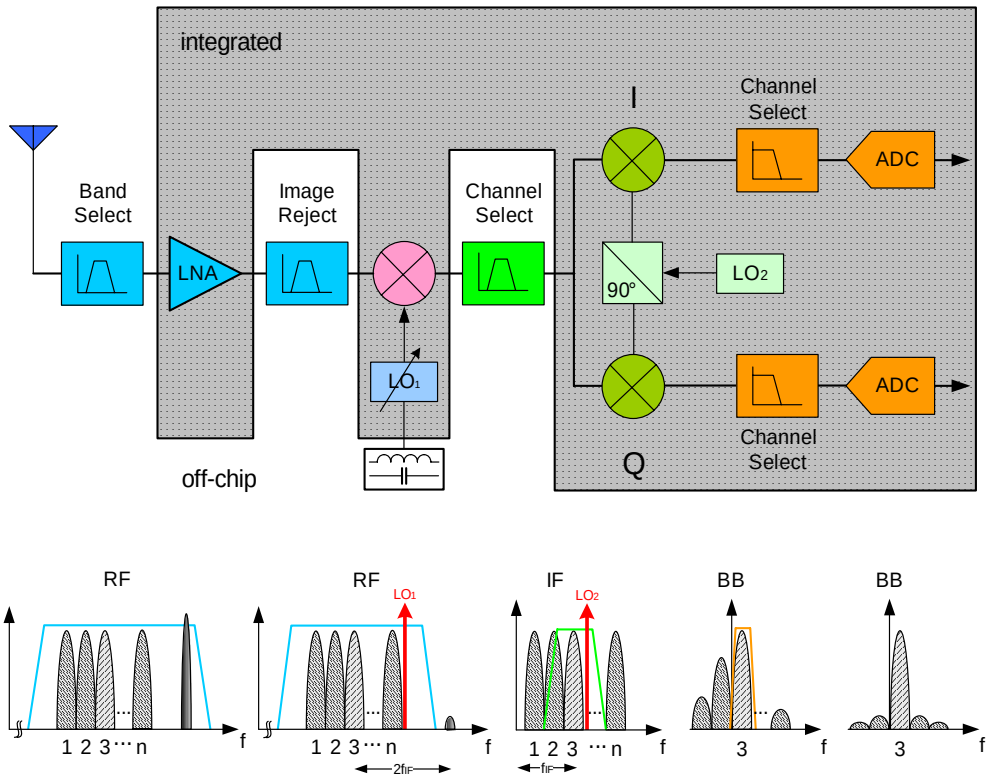


Figure 1.11: Example of a heterodyne receiver architecture with high-Q off-chip filters.Channel selection is done partly at IF and partly at baseband.

Digital modulation schemes, like those presented in section 1.3.1, use both in-phase and quadrature elements of a signal. Both components can be generated in the second mixing stage, as shown in figure 1.11. Since the channel of interest is already selected by the first mixer, the frequency of the second LO is fixed.

Off-chip passive components provide filters with a high Q-factor. This results in good performance for both sensitivity and selectivity and makes the heterodyne architecture a common choice. Furthermore, noise introduced by the local oscillator is less problematic, as it is filtered by subsequent channel selection. The filters can be manufactured in different technologies, e.g. bipolar and CMOS. However, off-chip filtering comes to the price of extra signal buffering (driving typically 50 Ohm loads), increased complexity, higher power consumption and larger size. Drawbacks that are contradicting the goals of increased portability. Examples using a heterodyne architecture can be found for instance in [Stetz1995], [Fenk1997], [Razav2001], and [Ahola2004].

Homodyne Receiver

The homodyne (homo = same, dyne = mix) architecture uses a single frequency translation step to convert the RF channel directly to baseband without operations at intermediate frequencies.

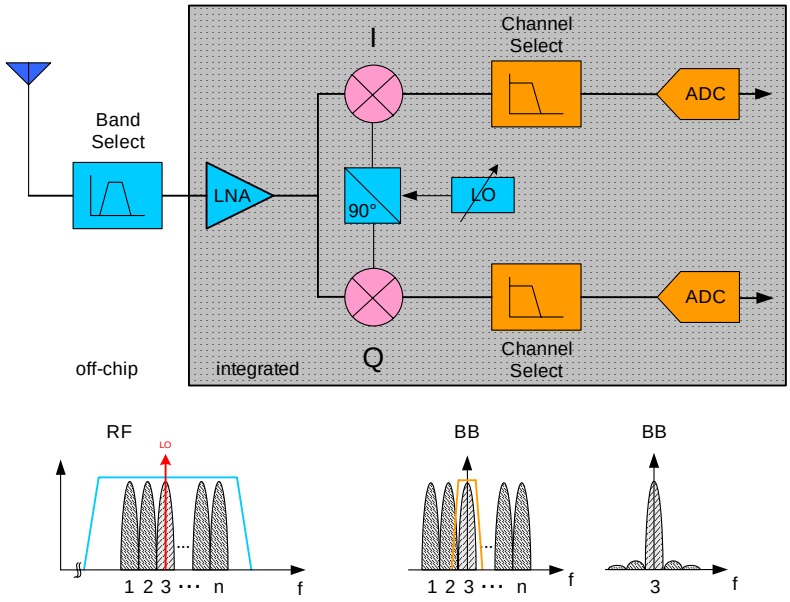


Figure 1.12: Zero-IF receiver architecture with quadrature downconversion.

It is therefore also called zero-IF or direct conversion architecture. Figure 1.12 shows this architecture for the case of quadrature downconversion. As in the hetero-

dyne case, an off-chip RF filter first performs band limitation, before the received signal is amplified by an integrated LNA. Channel selection is done by tuning the RF frequency of the LO to the centre of the desired channel, making the image equal to the desired channel. Hence, the problem of images is not present, and the off-chip IR filter can be omitted. A subsequent channel selection low-pass filter (LPF) then removes nearby channels or interferers prior to A/D conversion. Channel filtering is now possible entirely on-chip. But since neither image rejection filter nor channel select filtering is done prior mixing, all adjacent channel energy is untreated. This requires the LPF and ADC to have a sharp cutoff profile and high linearity, respectively. In the view of low-Q values of integrated components this implies tougher design challenges.

A severe problem in homodyne receivers are DC offsets. If one mixer input contains signal components from the second input, then mixing will generate a DC component. Caused by leakage from the local oscillator to the LNA (or vice versa), self-mixing will corrupt the baseband signal at DC and saturate subsequent processing blocks. If the receiver moves spatially, it receives reflected LO signals at the antenna which generates time varying offsets. These DC offsets need to be compensated. One technique is to disregard a small part of the signal band close to DC and employ a high-pass filter with very sharp cutoff profile at low corner frequencies. This requires large time constants, and hence, large capacitors, i.e. area. It is only practical for wide-band applications, where the loss of a few tens of hertz bandwidth at DC does not degrade the receiver performance significantly. For narrow band applications, this would cause large performance losses. Alternatively, in non-continuous transmission schemes, e.g. TDMA access, the DC offset can be periodically sensed and compensated by the receiver during the quiescent time intervals. Compensation is either carried out prior to the ADC, or in the digital domain using digital-to-analog conversion in a feedback path.

Due to direct conversion to DC, homodyne receivers are more susceptible to disturbances arising from I/Q phase mismatches, nonlinearities and flicker noise than heterodyne designs. To control the performance loss, additional circuitry and design efforts are required. However, there is no need for image rejection or other off-chip filters, saving power and total receiver volume. Its monolithic integration capabilities make the homodyne architecture an attractive alternative for wireless receivers. More information regarding cancellation of offset and other limitations, can be found e.g. in [Abidi1995], [Yoshi1998], [Razav1997], [Matin2000], [Namgo2001], [Cheun2001], [Faulk2002], [Sohn2002], and [Cao2004]. If the RF signal is downconverted in a single step to a low (but not to DC) frequency, then limitations at DC have less impact on the receiver performance. This approach is followed in low-IF architectures.

Low-IF

In a low-IF architecture, example shown in figure 1.13, an off-chip bandpass filter performs band selection prior to amplification by an LNA. In order to overcome the drawbacks associated with the homodyne architecture, the RF signal is downconverted to a frequency close to the baseband, but not including DC (typically between a several 100 kHz and few MHz). Hence, the problem of DC-offset is eliminated, and the effects of flicker noise and distortion are notably reduced. Furthermore, the conversion is done in a single step and all subsequent filtering can be performed on-chip. This improves integration capabilities. Similar to zero-IF, a tuneable local oscillator selects the desired RF channel. However, the image from downconversion is now different from the wanted signal and it has to be taken care of after the mixing stage. This can be achieved with integrated complex bandpass filters or in the digital domain using DSPs. However, gain and phase errors originating from mismatches in the quadrature mixing limit the image suppression. Compared to the homodyne architecture, power consumption is increased (due to analog-to-digital conversion at IF). Moreover, bandpass filter and ADC have to deal with double as wide bandwidth. Further details on low-IF receiver architectures can be found for instance in [Seven1994], [Gray1995], [Crols1995], [Crols1998], [Adise2002], and [Fang2005].

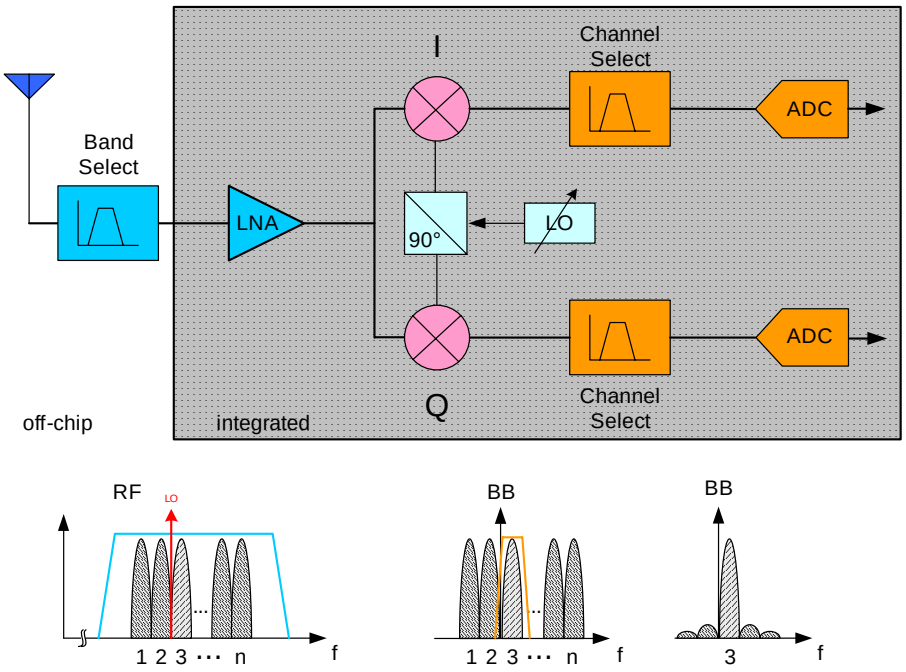


Figure 1.13: Low-IF receiver architecture with quadrature conversion.

Wideband-IF

An alternative to the designs above is the wideband-IF architecture shown in figure 1.14. Signals that passed the off-chip band selecting filter are amplified in the LNA and are then downconverted to IF. In contrast to the previous architectures, the first local oscillator frequency is fixed. All available channels are converted to intermediate frequency, resulting in a wide bandwidth at IF. Upconverted frequency components are removed by a simple low-pass filter. Channel selection and filtering are done at IF. The requirements for the tuneable LO and low-pass filter in the second downconversion stage are relaxed due to the lower operation frequency. Hence, a narrow channel can be selected and filtered without off-chip components. Furthermore, filtering can be performed partly in the digital domain, which adds to multi-standard operation capabilities of this architecture. This flexibility comes to the expense of higher linearity requirements of the ADC.

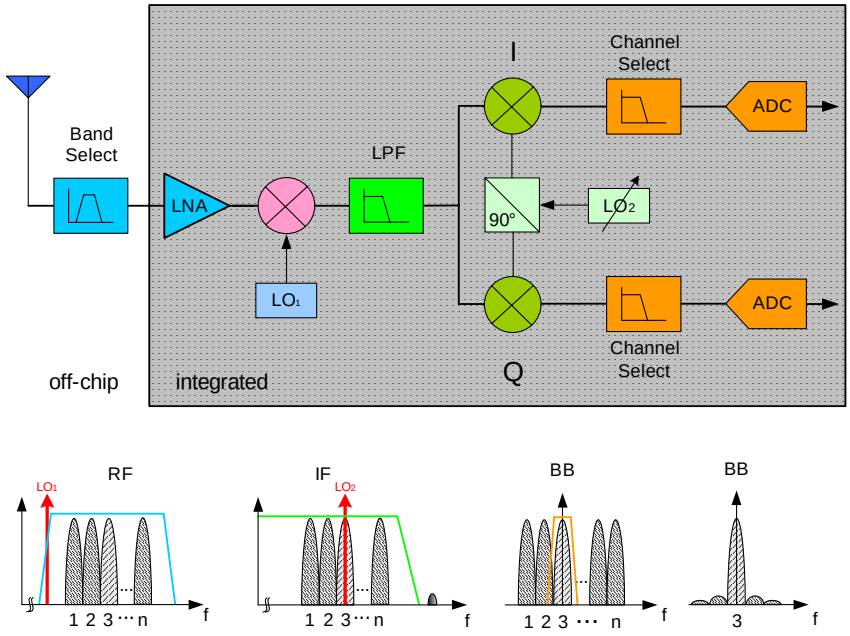


Figure 1.14: Wideband-IF receiver architecture.

Since the first local oscillator output is fixed and different from the channel frequencies, the problem of DC offset is alleviated in the wideband-IF architecture. The still existing self-mixing in LO_1 or LO_2 results in constant DC offsets that can be removed either in analog or digital domain. Isolation from the channel selection oscillator (LO_2) to the antenna is much larger than in the heterodyne case. This greatly reduces problems associated with time varying offsets. Using a fixed frequency at LO_1 allows for

phase noise optimization for this oscillator [Rudel1997]. Frequency conversion to IF introduces images again. These can be removed using a Weaver architecture [Weave1956], but mismatches between the I and Q paths limit the image suppression. Also, additional components from the second conversion stage inevitably result in larger power consumption. These problems are balanced by good monolithic integration capabilities and improved multi-standard prospects due to programmable filtering in the DSP. Further information on wideband-IF architectures can be found for instance in [Rudel1997] and [Bernd2003].

2. Sigma-Delta Modulation

This chapter reviews the principle of sigma-delta modulation and characterizes different noise shaping topologies, e.g. low and higher order modulators, single and multi-bit quantization, as well as continuous time modulation. At the end, design challenges are presented.

2.1 The Modulation Principle

Digital signal processing relies on discrete samples of data. According to the Nyquist theorem, [Nyqui1928] and [Shann1949], the sampling (or processing) frequency, f_s, has to be at least twice as large as the bandwidth of the input signal, f_B, to obtain an unambiguous reproduction of the signal. If this theorem is not fulfilled, aliasing will occur and information is lost. Data converters using $f_s = f_{Ny} = 2 \cdot f_B$ are hence called Nyquist converters. However, for reasons of noise margin and filter design complexity, a sampling speed of $f_s > f_{Ny}$ is usually applied.

As has been shown in literature, e.g. [Johns1997], the process of quantization can be modelled a process where the output y(n) is determined from the input sample x(n) plus an additive noise component e(n) as shown in figure 2.1. With the assumption that the additive quantization noise is independent and has white distribution, its power P_e is derived to equal $\Delta^2/12$, where Δ corresponds to the quantization step size. Therefore, the spectral density of the quantization noise, $S_e(f)$ is constant for a certain Δ.

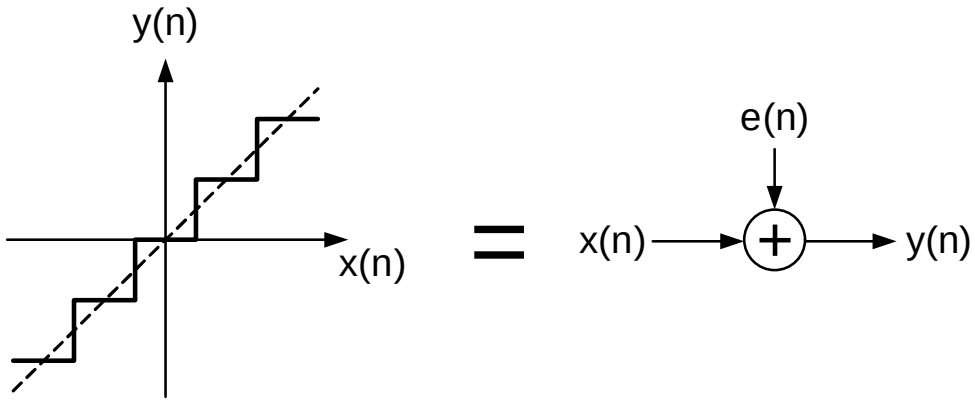


Figure 2.1: Linear quantizer model with additive noise source, e(n).

Sampling at a frequency much higher than the Nyquist rate is called oversampling and the rate by which f_s exceeds f_{Ny} is called the oversampling ratio, OSR

$$OSR = \frac{f_s}{f_{Ny}} = \frac{f_s}{2f_B} \tag{2.1}$$

Due to the white noise assumption, a larger sampling frequency causes the constant quantization noise power to be distributed over a larger spectrum. This reduces the noise power in the band of interest, f_B. A filter that limits the band to f_B cuts off all noise components for $f > f_B$ reducing the remaining quantization noise power, P_{e0}, within DC and f_B. It can be shown [Norsw1997] that the quantization noise power is decrease by a factor OSR. Each doubling of the oversampling ratio decreases the quantization noise power by a factor of two.

$$P_{e0} = \frac{\Delta^2}{12} \cdot \frac{1}{OSR} \tag{2.2}$$

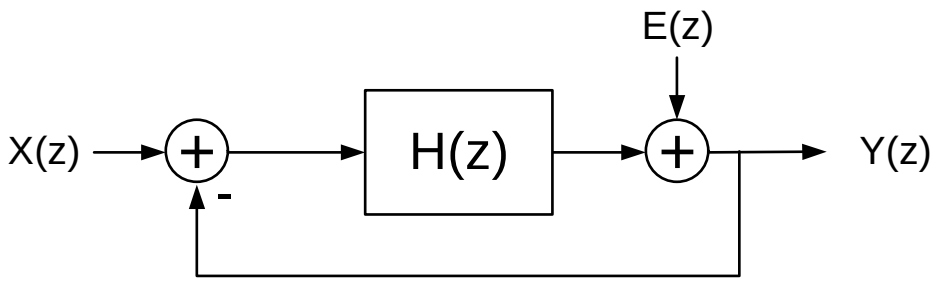


Figure 2.2: Linear model of sigma-delta modulator (1st order) with injection of quantization noise E(z) in the quantizer.

The technique of sigma-delta (or delta-sigma) modulation originates from the 1960‘s [Inose1963] and 70‘s [Candy1974]. Its name is derived from the difference and summing nodes in a loop configuration. Additional to oversampling, sigma-delta (ΣΔ) modulators modify the spectral properties of the quantization noise. They are said to *shape* the noise spectral density, $S_e(f)$, such that it is low in the band of interest and high elsewhere. This spectral shaping results from a negative feedback loop system as shown in figure 2.2. Here, the linear quantizer model from figure 2.1 is employed. Signal input x(n) and quantization noise contribution e(n) are assumed to be independent, leading to an examination using the superposition principle. With the help of the z-transform, the output is described as

$$Y(z) = (X(z) - Y(z)) \cdot H(z) + E(z) \tag{2.3}$$

where *H(z)* denominates a generic filter function. Two transfer functions can be derived: A Signal Transfer Function (STF) and a Noise Transfer Function (NTF):

$$STF(z) \equiv \frac{Y(z)}{X(z)} = \frac{H(z)}{1 + H(z)} \tag{2.4}$$

$$NTF(z) \equiv \frac{Y(z)}{E(z)} = \frac{1}{1 + H(z)} \tag{2.5}$$

With equations (2.4) and (2.5), the loop output is determined as:

$$Y(z) = SFT(z) \cdot X(z) + NTF(z) \cdot E(z) \tag{2.6}$$

In order to minimize the effect of quantization noise at the output, the NTF(z) should reach its minimum in the band of interest. That is achieved when H(z) reaches its maximum, i.e. has a pole. However, STF(z) would be close to unity for a maximum of H(z), leaving the input signal almost unchanged.

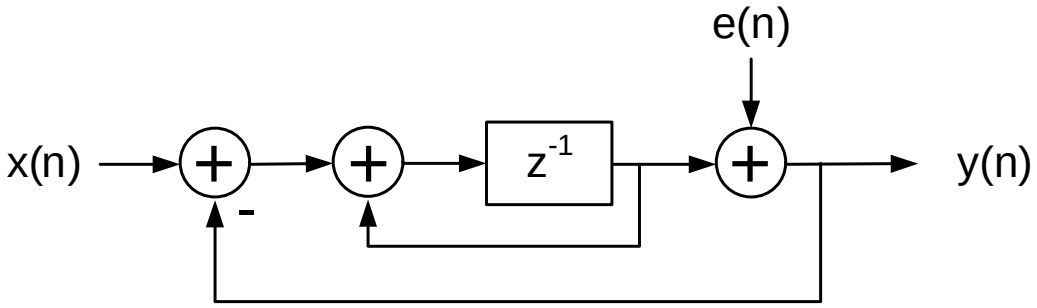


Figure 2.3: First order sigma-delta modulator with discrete time integrator.

First order noise shaping can be obtained by choosing the pole of H(z) to be located at DC. A straightforward integrator satisfies this requirement having

$$H(z) = \frac{1}{z - 1} \tag{2.7}$$

A possible implementation of a first order sigma-delta modulator is shown in figure 2.3. It is also called a single-loop, first order modulator architecture. With equation (2.7), the signal transfer functions becomes a simple delay

$$STF(z) = \frac{\frac{1}{z-1}}{1+\frac{1}{z-1}} = \frac{1}{z} = z^{-1} \tag{2.8}$$

whereas the noise transfer function describes a high-pass filter function

$$NTF(z) = \frac{1}{1+\frac{1}{z-1}} = (1-z^{-1}) \tag{2.9}$$

The quantization noise power for first order noise shaping, P_{e1}, is approximated in the band of interest [Johns1997] with

$$P_{e1} \approx \left(\frac{\Delta^2}{12}\right)\left(\frac{\pi^2}{3}\right)\left(\frac{2f_B}{f_s}\right)^3 = \frac{\Delta^2\pi^2}{36}\left(\frac{1}{OSR}\right)^3 \tag{2.10}$$

Compared to equation (2.2), this is a significant reduction in quantization noise power. Each doubling of OSR decreases this power now by a factor of 8. The higher the filter order of H(z), the more quantization noise is moved out of the signal band f_B.

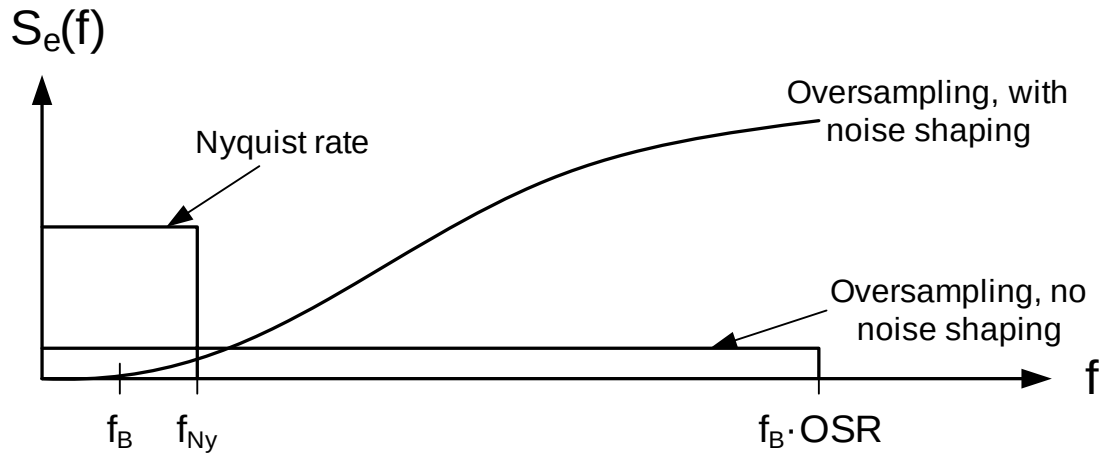


Figure 2.4: Noise density of sigma-delta modulation for 1st and 2nd order noise shaping compared to Nyquist rate and oversampling.

It should be noted, however, that sigma-delta modulation only alters the spectral properties of the quantization noise. The noise power is shifted to higher frequencies and still needs to be removed from the signal by means of low-pass filtering. In fact, the total amount of quantization noise increases for higher modulation orders. The fil-

tering is achieved by means of a decimation filter which also reduces the sampling rate and thereby the number of samples to be processed in DSPs.

2.2 Modulator Topologies

Sigma-delta modulators find a wide range of applications in data conversion systems, especially where high signal-to-noise ratios (SNR) are required. As indicated in equation (2.10), the reduction in noise power comes at the expense of a high sampling speed. This inherently limits the application range of this modulation technique. For instance, employing an oversampling ratio of OSR = 128 for a 20 kHz input signal, requires a sampling speed of 5.12 MHz. This relatively low sampling speed does not result in implementation difficulties. However, if the input is a wideband signal, of say 5 MHz, a sampling rate of f_S = 1280 MHz is needed. A high sampling rate naturally has a negative effect on power consumption. Also, some circuit technologies, e.g. CMOS switched capacitor designs, are not suitable for high speed operation in the GHz range. Hence, sigma-delta modulation has long been used in audio and narrow band applications. In recent years however, modulators with input bandwidth extending into the MHz range have been reported, e.g. [Fujim2000], [Geert2000a], [Tabat2000], [Burge2001], [Salo2001], [Vleug2001], [Dezza2003], [Veldh2002], [Veldh2003].

To maintain a reasonable power consumption, the oversampling rate must be reduced for wideband applications, resulting in insufficient removal of quantization noise. Thus, a different approach than brute force sampling rate increase must be taken. Some options to expand the signal bandwidth while maintaining a high signal-to-quantization noise ratio (SNDR) are summarized below.

Higher Order Modulation

In a first order modulator, the quantization error from the previous sample is subtracted from the present sample. Higher order modulation is achieved by adding more integration stages. This results in a sharper high-pass filter transfer function H(z) and shapes the quantization noise more aggressively out of the input signal band. In general, a modulator of M^{th} order exhibits an M times better noise shaping property compared to a first order modulator, whereas the input is only delayed by a factor of M. The SQNR improves by about (6·M+3) dB per octave of f_S [Johns1997]. Equation (2.11) presents a general modulator transfer function for an M^{th} order sigma-delta modulator.

$$Y(z) = X(z) \cdot z^{-M} + E(z) \cdot (1 - z^{-1})^{M} \tag{2.11}$$

The single loop topology in figure 2.5(a) is a straightforward extension of the simple first order architecture presented in figure 2.3. Several integration stages are accommodated in a single loop. The gain stages in the feedback path adjust signal amplitudes. Local feedback (or local resonators), introduced in [Fergu1991], can be added to shift the NTF zeros away from DC to further reduce the inband noise power. A one bit quantizer reduces the DAC implementation in the feedback path to a simple switch with good linearity.

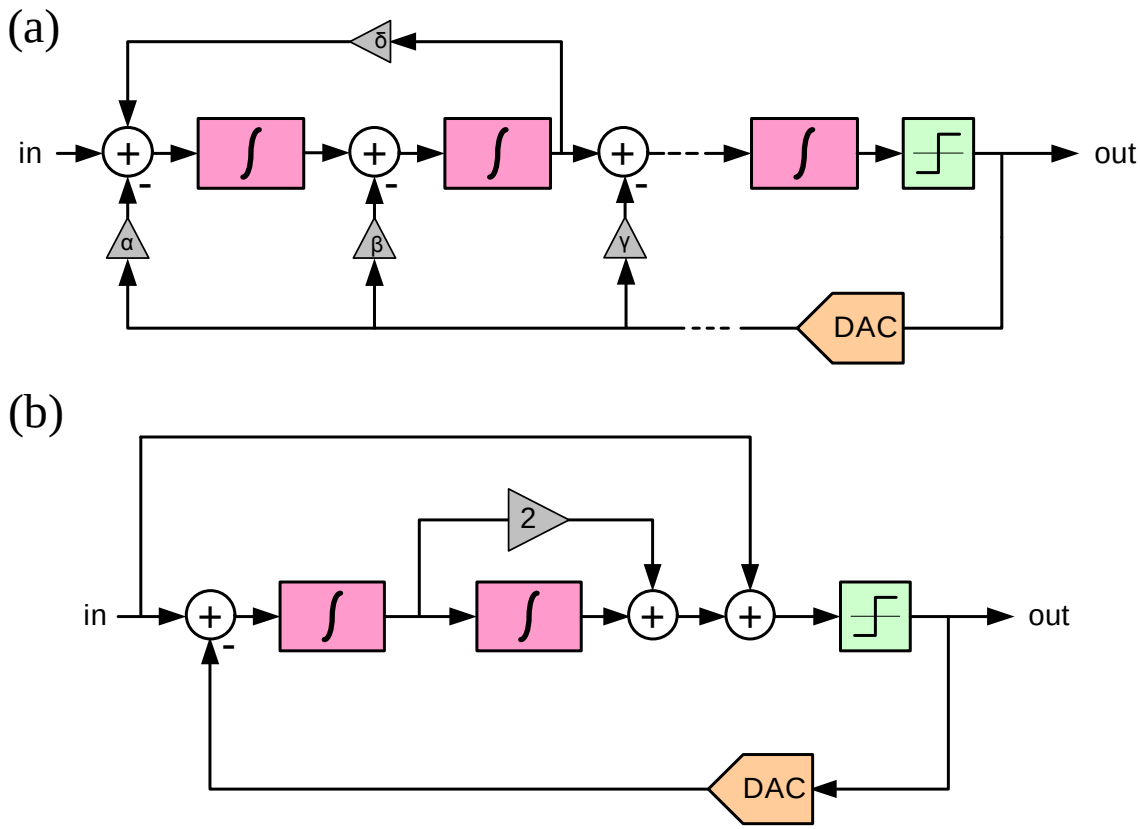


Figure 2.5: Single loop higher order modulators: (a) chain of inverters and local resonators; (b) low distortion feed forward architecture

An architecture using feed forward of the input signal, figure 2.5(b), has been proposed in [Steen1998] and [Silva2001] and was further developed in [Gothe2003]. It approaches the problem of integrator nonidealities such as finite slew rate and gain for wideband applications at low oversampling ratios. The reduced sensitivity to circuit nonidealities derives from decoupling of sensitive circuits from the input signal. The

integrator stages ideally only process quantization noise, reducing their performance requirements.

Major limitations to high order, single loop structures are concerns of stability. If the input signal level to the quantizer exceeds its normal range, the quantizer becomes overloaded, i.e. the quantization error becomes larger than ±Δ/2. The system might not be able to return to a stable state even if the quantizer input returns to low values. The larger the number of integrators, the higher the risk to overload the quantizer. Solutions to this problem lie in adding sensing circuitry to reset the modulator in the event of instability or by reducing the input signal level. The latter method impacts the dynamic range performance, and hence, the sensitivity of the total receiver. Different methods for this are discussed for instance in [Johns1997].

Alternative topologies are cascaded (MASH) modulator architectures. They employ 2 or more modulator loops, each comprising a low order modulator to maintain stability. Each following loop processes only the quantization noise of the previous loop, which improves the total resolution. The quantization noise of the following loops is subtracted from the output of the first loop in a digital error cancellation logic, further reducing the total quantization noise. An architecture with four integration steps arranged in two 2^{nd} order loops is shown in figure 2.6. This 2-2 MASH modulator provides 4^{th} order noise shaping. The DACs in the feedback paths have the same resolution as their corresponding quantizers, e.g. 1 bit.

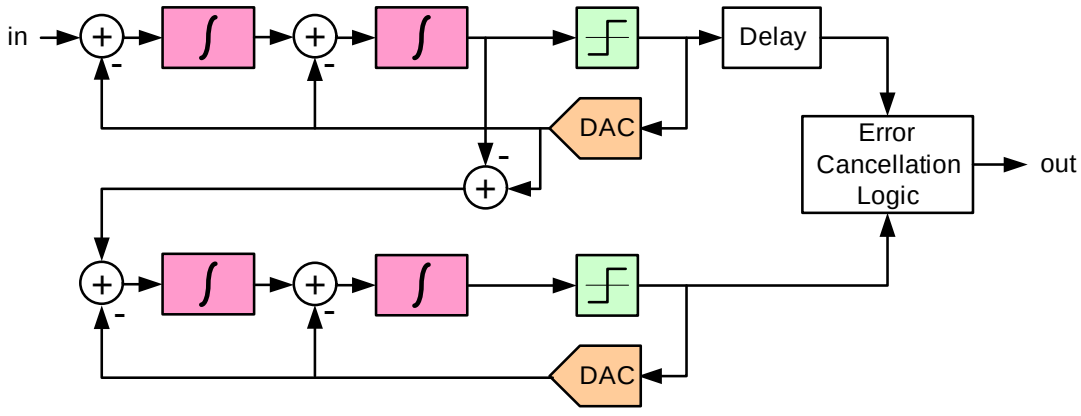


Figure 2.6: Cascaded modulator showing a 4^{th} order, dual loop architecture.

The MASH topology was first introduced in [Matsu1987] and quickly gained much interest in sigma-delta applications. The main advantage of a MASH architecture is the high degree of noise shaping without emerging stability problems. In theory, there is

no limit on how many cascades can be used. However, cascaded modulators require very good matching between analog and digital processing paths. In practice, the second and following loops do not only process noise and the quantization error is not cancelled completely resulting in leakage noise at the modulator output. Furthermore, internal signal level scaling impacts the dynamic range. In order to improve matching, bigger analog components are used, increasing the silicon area. The larger number of components also contributes to a higher power consumption.

Error Feedback Structure

A modulator using a noise shaping filter in the feedback part is the error feedback topology shown in figure 2.7 [Anast1989], [Norsw1997]. Its transfer functions are readily derived as STF = 1 and NTF = G(z)-1. This modulator leads to simple circuit implementations. An important drawback, however, is its susceptibility to analog component mismatch. The zeros of the NTF, i.e. G(z) = 1, are not created by a large DC gain. Therefore, small coefficient mismatches cause the remaining quantization noise. Hence, this circuit is more suitable for digital modulator implementations, where no component mismatches occur.

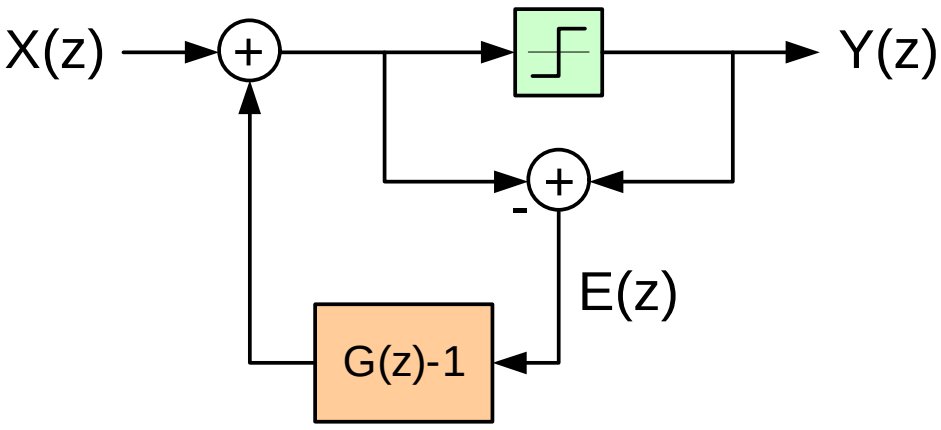


Figure 2.7: General, first order error feedback architecture.

Multi-Bit Quantization

Another option for improving the signal to noise ratio at low oversampling ratios is to extend the single bit quantization into multiple bits. This reduces the quantization step size Δ, and hence lowers the quantization noise power. A more linear quantizer gain allows for higher orders of noise shaping before the modulator reaches instability.

For single bit quantization, the feedback DAC comprises only a switch between positive and negative reference voltage. For the case of multi-bit quantization, a multi-bit DAC is needed. Any nonlinearities that are introduced in the feedback DAC directly add to the input signal and experience the same transfer function as the original input. These nonlinearities are therefore not noise shaped, regardless of the filter transfer function H(z). The effects of nonlinearities can be reduced by randomizing the errors (dynamic element matching), employing digital compensation techniques, non uniform quantizing, and/or careful layout. For instance, modulators having a signal-to-noise ratio of larger than 90 dB have been reported in e.g. [Fujim2000], [Geert2000b], and [Vleug2001]. However, each compensation technique also increases the required die area and power consumption.

Continuous Time Modulators

Discrete time (DT) sigma-delta modulators use a sample and hold stage after the anti-aliasing filter and prior to the actual modulator. These modulators are implemented using switched capacitor (SC) circuits. In order to comply to settling time requirements for fast sampling, the operational amplifier needs to have a high slew rate.

Alternatively, sigma-delta noise shaping can also be achieved in the continuous time (CT) domain. These modulators employ sampling first after the noise shaping filter, as part of the quantizer. Loop filtering remains in the analog domain. This already performs an anti-aliasing function which relaxes the requirements of the preceding filter or even eliminates its need. Area and power advantage of CT modulators originate from reduced kT/C-noise, as the input of the modulator is not a sampling capacitor. Since much smaller capacitors can be employed, the settling time requirements are reduced, allowing for higher speed or lower power consumption.

However, as input subtraction and the noise shaping filter operate continuously, clock jitter from the feedback path severely impacts the modulator SNR performance. Furthermore, since the filter relies on absolute component values rather than capacitor ratios, the impact of process and temperature variations is worse than for a SC implementation. To achieve similar performance, CT modulators require additional power/

area expensive biasing, tuning, compensation, and calibration techniques. These and other techniques are described for instance in [Cherr1999], [Gerfe2001], [Henke2002], [Ortma2002], [Veldh2003], and [Thoma2005].

Future Design Challenges

Sigma-delta modulation employs oversampling and noise shaping to obtain high signal to noise ratios. Trading precision in amplitude for resolution in time, they rely on high operating speeds for relatively small signal bandwidths. Traditionally, sigma-delta modulators have preferably been used in narrow band applications.

An eminent challenge for sigma-delta application in wireless radios is the demand for ever more bandwidth, i.e. several tens of MHz. Simply increasing the operating frequency would result in prohibitively large power consumption and also renders circuit implementation very difficult. New modulator architectures have to be designed that obtain sufficient SNR at low oversampling ratios. An increase of modulator order, use of multi-bit quantization as well as continuous time loop filtering are further measures to qualify sigma-delta modulators for wideband applications. Additional circuitry for more modulator loops, compensation and tuning circuits contrast the design goals for lower power consumption and smaller die size.

Continuous time, single loop modulators with single bit quantization are suitable for wideband applications of up to 5 MHz bandwidth (e.g. Bluetooth, WCDMA, GSM). For larger bandwidths, like WLAN, continuous time, single loop modulators with multi-bit quantization are preferable [LeGui2005].

With continuing technology development, device sizes are scaled down. Following the projection of the International Technology Roadmap for Semiconductors [ITRS04], feature sizes around 30 nm by the year 2010 can be expected. Shrinking gate oxide thickness of active devices is likewise anticipated. This in turn requires the supply voltage to drop (about 0.7 Volt in 2010) to maintain similar electric field strengths, leaving very low margins for device operation and noise immunity. New architectures and devices for circuits like amplifiers are essential for operation in such supply realm.

Another design challenge is that for ultra-low power consumption. A low supply voltage contributes to this goal. But the increase of circuit complexity offsets this advantage. Especially in the field of multi-standard operation, hardware sharing between the standards should be maximized.

Although CMOS circuits consume most power during switching operation, static consumption due to leakage currents plays an increasing role. Arising from gate tun-

nelling and junction or sub-threshold leakage, these currents remain in the order of few nA, but the large number of digital gates needed for sophisticated filtering sums up to significant amount of power that is dissipated even in a non-active state. Future implementations of sigma-delta converters should therefore include shut down/wake up functions for both, analog and digital signal processing.

Another design challenge is noise immunity. Integration of RF and analog baseband circuits onto the same die as the digital logic makes the analog circuits prone to noise from switching events in the digital domain. This materializes for instance in form of substrate noise coupling, signal crosstalk or power supply variations. Noise isolation can be improved by increasing the on-chip distance between analog and digital circuit blocks, separate power supplies, design of defined signal return paths and improved layouts. However, this not only raise die costs, but also lowers the production yield. Hence, alternative technologies, e.g. silicon on insulator (SOI), are envisioned to solve the noise coupling problem.

Future sigma-delta topologies need to incorporate innovative solutions on device, circuit and system level. Nevertheless, sigma-delta modulators are well suited for wideband applications, as they provide high signal to quantization noise ratios and offer relaxed requirements of preceding analog filters. Their qualification for standard CMOS processes contributes to low-cost wireless radio transceiver implementations. Further discussions and applications of sigma-delta modulator topologies can be found for instance in [Boser1988], [Schre1989], [Jantz1991], [Zhang1991], [Candy1992], [Karem1994], [Baird1995], [Razav1995], [Brook1997a], [Brook1997b], [Johns1997], [Norsw1997], [Marqu1998], [Li2003], [Li2003], and [Gothe2003].

3. Frequency-Locked Loop

Chapter three introduces a novel frequency synthesizer concept and architecture. Placing emphasis on flexibility of frequency bands, its applications are envisioned in a multi-standard, multi-band environment of future wireless radio communications. The synthesizer uses a negative feedback loop to lock on a target output frequency. The architecture and its processing blocks are described, their functionality is analysed and design trade-offs as well as limitations are presented. In the end of this chapter, simulation results and possible directions for further research are presented. Frequency synthesizer concepts and application areas are reflected over in the beginning of this chapter.

3.1 Frequency Synthesizer Concepts

Frequency Synthesizers, FS, form an essential part in any wireless communication device. Their tasks include e.g. clock signal alignment and recovery for data exchange over different frequency domains, carrier generation and clock multiplication, deskewing, modulation, and spectrum spreading. When used for carrier generation, parameters like frequency accuracy (or phase noise) and spurious tones, settling time, frequency (channel) step size, as well as power consumption characterize the performance.

Frequency synthesizers often employ oscillation devices. One option is the use of off-chip crystal oscillators. They have limited ability for frequency tuning, but provide very accurate, though low frequency signal sources. They are often used to provide reference signals. Being an off-chip component, they contribute to larger volume and higher manufacturing cost. L-C oscillators, on the other hand, are on-chip devices that output high frequencies over a wide spectrum. However, their on-chip passives have a low Q-value, making the synthesizer output susceptible to noise. Larger sizes of inductors and capacitors address this problem but increase the die size. Hence, L-C oscillators are put inside feedback loops to compensate for their frequency drifting.

In the following section, selected frequency synthesizer concepts used in communication applications are reviewed before the novel architecture is introduced.

Ring Oscillators

As illustrated in figure 3.1, ring oscillators have a straightforward implementation. They consist of a chain of inverters and a feedback of unity gain. Each inverter drives one other inverter and contributes with delay, τ_{inv}, to the today delay of the chain. In order to maintain oscillation, the number of inverters, M, has to be at least three and must be odd. To realize different clock frequencies and phases, the oscillation signal can be taken out after any of the inverters.

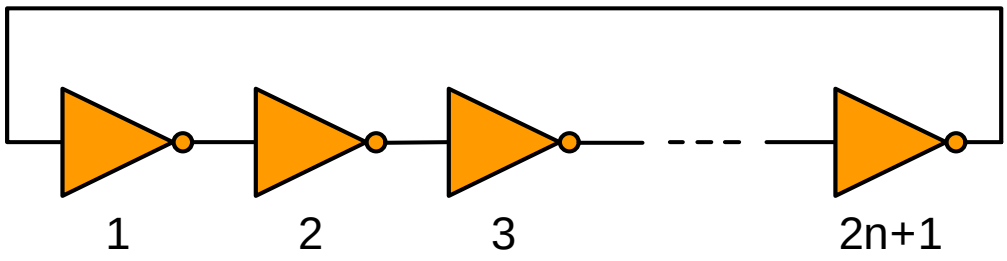


Figure 3.1: Ring oscillator using an odd number of inverters in a chain.

Assuming identical delay values for each of the M inverters of the chain, the ring oscillator frequency is determined by equation (3.1),

$$f_{osc} = \frac{1}{2M \cdot \tau_{inv}}, M = 3, 4, \ldots, (2n + 1) \qquad (3.1)$$

where $n \in \mathbf{N}$, $n > 0$. The oscillator output frequency can be varied by changing the number of inverters in the chain or adjusting the block delay τ_{inv}. Ring oscillators produce outputs that resemble pulse signals and hence, they are suited for digital processing. Each inverter also adds jitter to the output signal. As this is not compensated, ring oscillators are appropriate only for applications that have an inherent jitter tolerance. The phase of the output signal is not aligned to a reference, which excludes signal processing or communication applications using phase informations. However, the absence of off-chip components and the straightforward design and implementation of ring oscillators still make them an attractive choice.

Delay-locked Loop

The delay-locked loop, as depicted in figure 3.2, can be seen as an extension of the ring oscillator architecture. A chain of buffers with variable delay forms a delay line, which is driven by an input clock, CLK_{in}. Phase alignment between CLK_{in} and the loop output signal, CLK_{out}, is accomplished by adding delay to the input. Phase differences between delay line output and its reference, CLK_{ref}, are discriminated in the phase detector (PD). The output of the phase detector is typically integrated by a charge pump and processed by a loop filter to produce a control voltage, V_c. This voltage regulates the delay by either adjusting supply voltage or capacitive load of the buffers. As the loop has negative feedback, the output phase approaches the reference phase.

Delay-locked loops achieve clock synchronization between different circuit domains. Adding delay can also be used to generate multiple or quadrature clock phases. Another application of DLLs are clock multiplication or division which is particularly interesting when a clock is to be distributed with a lower rate on the board level in order to address signal to noise or power consumption problems.

The basic delay-locked loop is implemented in a straightforward design and comprises mainly digital elements. Hence, it does not require off-chip components, which in turn reduces implementation costs. Restricted phase capture ranges typical limit the application for DLLs. In [Sidir1997], a dual DLL is presented that offers an unlimited, i.e. modulo 2π phase shift option. More recent developments of delay-locked loops have been reported in e.g. [Suspl2003], [Zhuan2003], and [Chang2005].

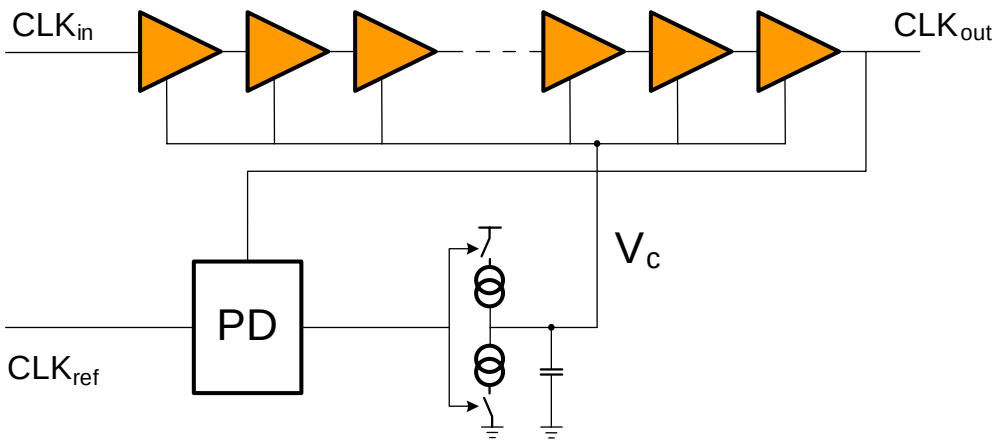


Figure 3.2: Block diagram of a delay-locked loop

Direct Digital Synthesis

As the name implies, these synthesizers generate their output waveform digitally. The points of the waveform, i.e. the phase increments, that are to be synthesized are stored in memory, typically in a fixed or programmable ROM. To access the predetermined phase values of the memory, a counter operating in wrap around mode selects an address where digital numbers are stored. These numbers correspond to amplitude values of the waveform that is to be generated. Digital-to-analog conversion of the ROM values produces an analog wave. The resulting signal is finally low-pass filtered and amplified to reduce spurious tones and to produce the required signal level.

Tuning of the direct digital synthesizer is achieved by changing the step size in the counter. This is effectively a division of the reference clock. A larger step size completes the full phase cycle faster and the output frequency increases. A smaller step size causes the cycle to take longer time for completion of a full cycle. Hence, the output frequency decreases. Changes of the counter value will instantly result in a step size change. There is no need for a settling time as in the case for feedback loop synthesizers. This makes the direct digital synthesizer a highly agile circuit.

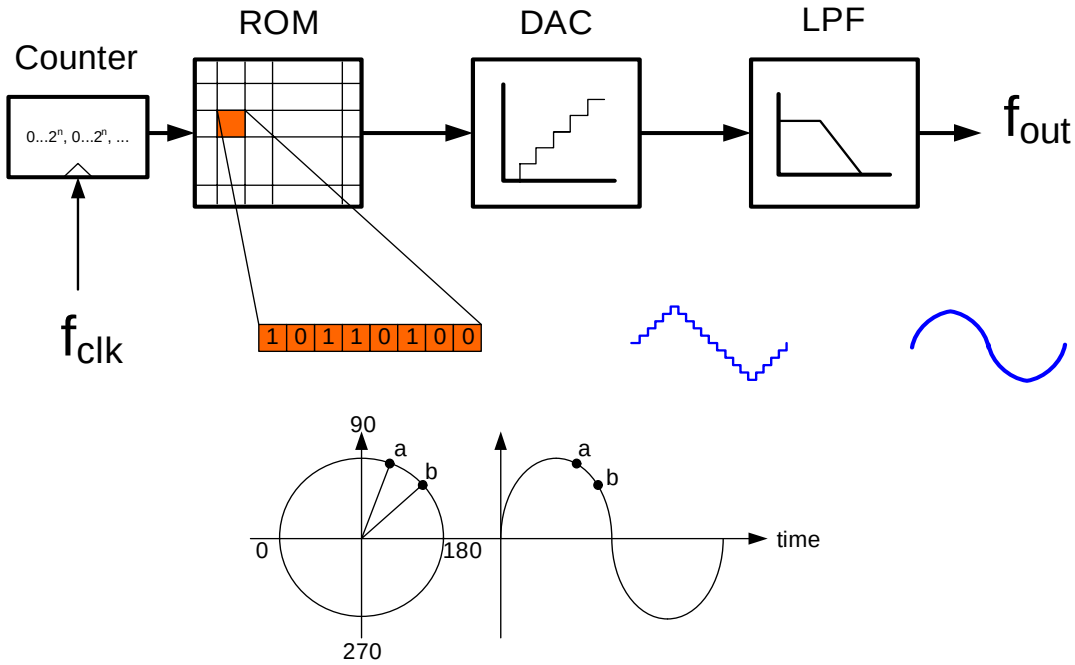


Figure 3.3: Direct Digital Synthesis Architecture based on read only memory

The frequency resolution at the output is determined by the number of points available in the memory accessed by the counter. A small phase step size conceptually requires the ROM to be large. Much research focuses on reducing the ROM size or even omitting it [Morte1999]. For generated waveforms of high amplitude resolution, a large number of bits in the DAC is required. That leads to increased costs regarding area and power consumption.

An inherent limitation to DDS synthesizers is their dependency on a reference clock. that is already larger than the maximum intended output frequency. To satisfy the Nyquist criteria, the reference clock has to be at least twice as high as the maximum generated frequency. This makes this synthesizer type unsuitable for RF applications where a high (carrier) frequency is to be generated from a low rate source within the circuit. Further information about recent direct digital synthesizers can be found in, [Mohie2002], [Vankk1998], [Calba2002], [Yamag1998], [Bella2000], [Jiang2002], [Madis1999], [Toros2003], [Nosak2001], [Richt2001] and [Morte1999].

Phase-locked Loop

A phase-locked loop, PLL, is a closed-loop control system that uses phase adjustments to achieve either frequency generation, phase alignment or both. The loop parameter is the phase difference between the oscillator output and a provided reference. A delay-locked loop operates by adding delay until two input signals are phase aligned. A phase-locked loop, however, increases or decreases the oscillator output frequency to reduce the phase difference to acceptable levels.

A block diagram of a PLL is shown in figure 3.4. A phase and frequency detector, PFD, discriminates amount and sign of phase difference. The amount is expressed as a pulse length, whereas the sign, whether the input leads or lags, is expressed as the pulse being present on either UP or DN signal. The phase error pulse of length Δt is converted into a voltage by integration with a charge pump, CP. For a leading input signal, the oscillator frequency is increased by raising the control voltage, V_c. For a lagging input, the oscillator control voltage is reduced by decreasing V_c. The succeeding loop filter, with transfer function F(s), extracts the DC component of V_c before biasing a voltage (or current) controlled oscillator, VCO (or ICO).

The VCO output is fed back to the detector via a divider stage to reduce the high rate signal to a frequency close to the reference. This division is accomplished by detection of zero crossing and omitting of pulses. Due to negative feedback, the PLL output frequency tracks the reference input rate with a multiple of factor N, i.e.

$$f_{OUT} = N \cdot f_{REF} \tag{3.2}$$

In order to tune the PLL to different output frequencies, the divider ratio is modified. The most straightforward implementation of rate changing is integer-N division, for instance presented in [Parke1998] and [Herna2002]. As the name suggests, the divider ratio is changed only with integer step size, carried out by e.g. a counter or pulse swallowing circuit.

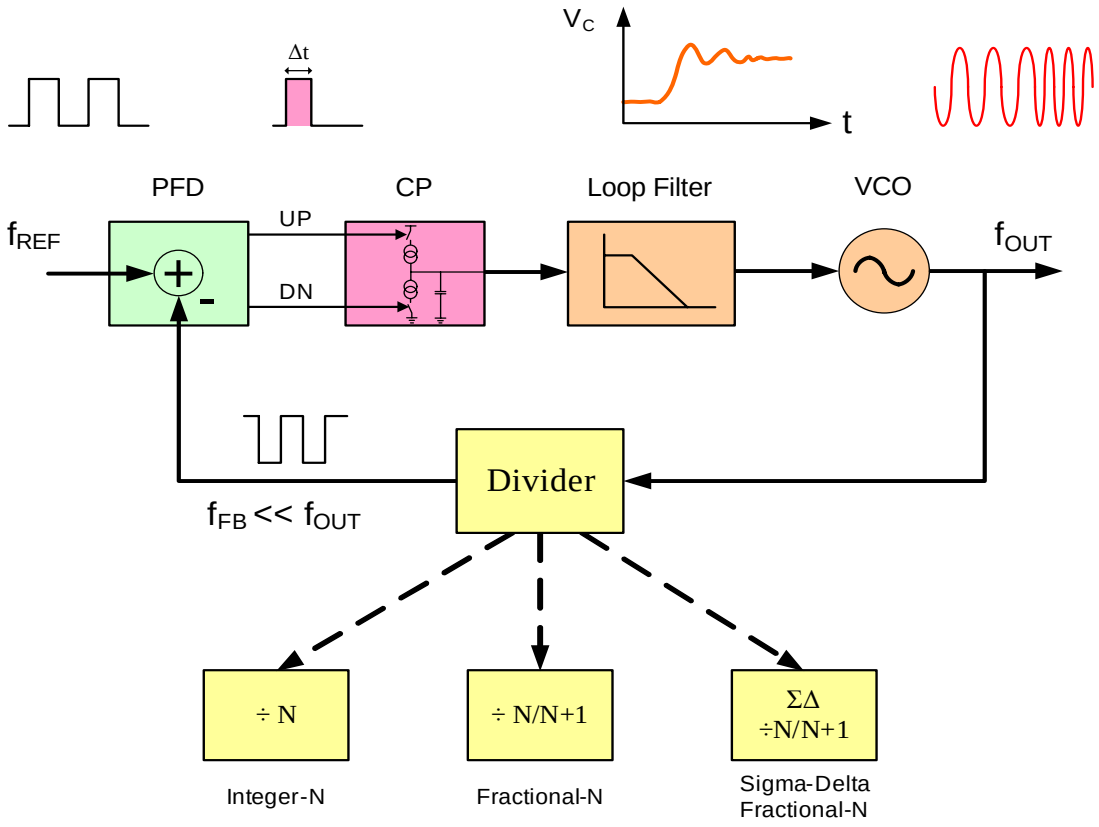


Figure 3.4: Architecture of a phase-locked loop and possible divider implementations.

A PLL is a system with contradicting design objectives. Modern communication applications need to use their available spectrum efficiently.They desire a high synthesizer output frequency and a small channel bandwidth. This in turn requires the PLL to provide a small step size at the output which is accomplished with a small reference input rate. A second important design objective is the realisation of output changes within in short time. The design contradiction lies in the loop dynamics of the PLL. Inside the closed loop bandwidth, the transfer function gain is high. This implies that ref-

erence changes at frequencies much below the loop bandwidth are tracked well by the oscillator. However, phase changes at frequencies outside the loop bandwidth are subject to much lower transfer function gain. Hence, they are not tracked well. A small f_{REF} also results in a slower settling time of the output. An alternative to equation (3.2) is that the division ratio could be chosen to be small. Though that would cause detector, charge pump and low-pass filter to operate at a high speed.

Fractional-N loops overcome much of this problem. The output frequency can be changed in smaller (not only integer) fractions of the reference input. In practice, the division ratio is an average between two integers, say N and N+1. The reference frequency can now be much higher, allowing a larger loop bandwidth and hence, faster settling. However, spectral spurs occur at the output at multiples of the changing rate between N and N+1, causing problems in transceiver applications. These spurs can be reduced by randomizing the division rate change. One possible option for this is sigma-delta (ΣΔ) modulation of the feedback division ratio e.g. presented in [Riley1993], [Filio1998], [Rhee2000], [Lee2001], [Tang2001], and [Ahola2003].

Another approach for fast frequency lock and small channel spacing is the dual-loop synthesizer, presented for instance in [Aytur1997], [Yan2001], and [Kan2002]. The output of a variable, low frequency loop is mixed with a fixed, high output frequency loop. Nonlinearities in the mixer or loop mismatches can, however, degrade the synthesizer noise performance due to side band spurs. A variation to this is the dual-PLL architecture, e.g. [Yuen1997], comprising two individual loops. During one PLL supplies the output signal, the other is locking to a new output frequency. Frequency agility is limited by the selecting switch. Drawbacks of this architecture are larger chip area and power consumption.

Table 2: Qualitatively Overview for selected frequency synthesizer concepts

	Phase Noise	Switching Speed	Tuneability	Complexity	Wireless Usability
Ring Osc.	High	--	Low	Low	Limited
DDS	Medium	High	High	High	No
DDL	Low	Medium	High	Medium	Yes
PLL	Low	Medium	High	High	Yes

Wireless communication applications, typically employing radio frequencies, demand synthesizers with low phase noise, fast channel switching, wide tuning bandwidth as well as low circuit complexity and power consumption. In order to find a

satisfactory design solution, a designer needs to trade off these different and sometimes contradicting design objectives. Table 2 qualitatively summarizes the presented frequency synthesizer concepts with respect to different performance factors. Feedback systems like delay- or phase-locked loops imply more complicated and power hungry circuits. However, they justify this with very low phase noise values that are required by many communication applications. More detailed descriptions about building blocks, loop analysis, noise impact and design trade-offs of phase-locked loops can be found e.g. in [Best1984], [Crawf1994], [Egan2000], and [Razav2000].

3.2 Frequency-Locked Loop

An alternative way to frequency synthesis is presented in this thesis. Owing to operation in different frequency bands and with different performance specifications, multi-standard applications require a large degree of flexibility. An overall guideline for this synthesizer architecture was therefore the possibility of uncomplicated configurability. The synthesizer targets the generation of frequencies in different bands by means of frequency multiplication from a highly accurate, low frequency reference. It does not aim for phase lock. Possible options for phase looking are briefly discussed later in this chapter.

3.2.1 Synthesizer Architecture and Principle

Wireless radio communication applications using frequency division or frequency hopping access technologies utilize only a limited number of frequencies for channel implementation. Hence, the synthesizer needs to generate a set of discrete channel centre frequencies.

The architecture of the frequency-locked loop, FLL, is presented in figure 3.5. It shows a loop employing negative feedback to stabilize its output frequency to a multiple of a given reference. This reference is split into two entities: a time signal of frequency f_{REF} and a digital value information, N_{REF}. Contrary to traditional PLLs, where the output is tuned by changes in the feedback divider, the FLL keeps the feedback ratio, N, at a constant value. Output frequency changes are performed by changing the digital reference word instead. This moves the loops tuning point into the detector and

simplifies divider implementation to an integer-N type with constant and low division ratio.

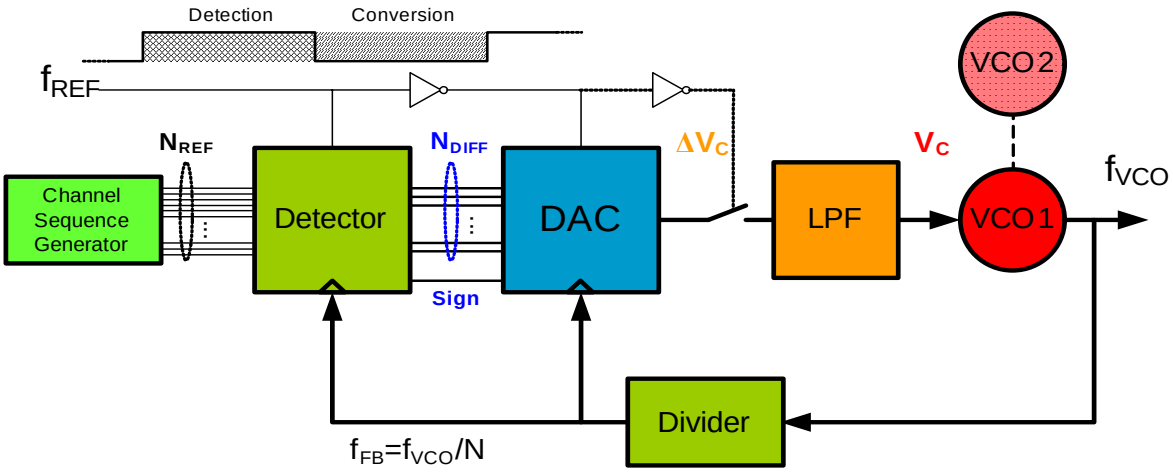


Figure 3.5: Frequency-locked loop block diagram with generic DAC

A consequence of the twofold reference is the straightforward implementation of the reference sequence. Synthesizer applications that require a repeated change of output frequency, e.g. spread spectrum or frequency hopping, need a predetermined sequence of output rates. In PLLs, this is implemented as a sequence of divider values in memory or as external command. The presented frequency-locked loop uses a set of multi-bit reference words that is provided by the *Channel Sequence Generator* in figure 3.5. It can simply be implemented as read only memory (ROM) or alternatively as part of the digital signal processing. Application to a different standard is simplified by modifying the word sequence of N_{REF} instead of implementing complex divider hardware.

Figure 3.6 shows definitions of detection and conversion phase as well as the relation of reference and feedback signals. The reference time period, $T_{REF} = 1/f_{REF}$, is divided into two phases. The duty cycle of T_{REF} forms the *detection phase* where possible frequency differences are discovered. The number of completed feedback periods, $T_{FB} = 1/f_{FB} = N/f_{VCO}$, that occur during each detection phase, is compared to the predetermined value N_{REF}. At the end of the detection phase, the detector stores a multi-bit word, N_{DIFF}, and the detection process is suspended. N_{DIFF} represents the amount of frequency (period) difference between N_{REF} and the feedback signal, making the detector a frequency to digital converter. One additional bit delivers the sign information, i.e. whether the loop output frequency is faster or slower than its target value.

The second phase, i.e. the remaining time of T_{REF}, is the *conversion phase*. A digital-to-analog converter (DAC) succeeding the detector converts N_{DIFF} into an analog voltage, ΔV_C, that subsequently controls the oscillator frequency. Using the time reference with f_{REF} as an enable signal for both DAC and detector ensures that only a completed detection result is further processed. The detector resolution limits how accurate a following control voltage can be produced. In the design and simulations presented in this thesis, a duty cycle time of $\alpha = 50\%$ is assumed. However, other values for α are possible, allowing for further design freedom.

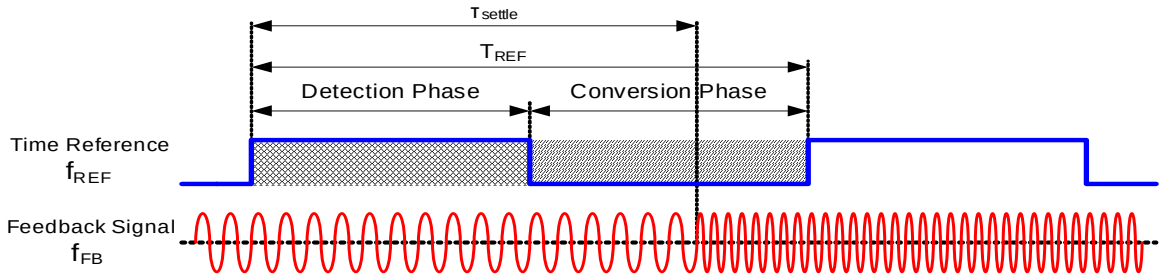


Figure 3.6: Definitions of synthesizer signals and phases.

The feedback signal is not only an input to the detector. It also serves as a clock signal to the digital parts in the architecture. Therefore, no additional clock needs to be provided externally, the synthesizer clocks itself.

The settling time τ_{settle} is composed of the detection phase, i.e. $\alpha \cdot T_{REF}$, and the time needed for digital-to-analog conversion. This D/A conversion time must be smaller than the duration of the conversion phase. Otherwise, the oscillator control voltage is altered during the following detection phase, which would distort the following detector result. To ensure that $\tau_{settle} < T_{REF}$, a sufficiently high clock rate must be chosen with the feedback division ratio.

After settling of the DAC output, the voltage change ΔV_C is low-pass filtered and added to V_C, the control voltage finally applied to the VCO, that had been unchanged until then. This control voltage V_C adjusts the oscillator output frequency. For operation in different frequency bands, V_C can be switched to one of several VCOs. This enables reuse of the synthesizer architecture and avoids the use of wide band oscillators. The reference value N_{REF} has to be adjusted accordingly for each targeted output band.

3.2.2 Detection Process

The detector identifies the number of completed feedback periods that occur during the detection phase. A straightforward implementation of the detector is the realization as a synchronous counter in a count-down mode as shown in figure 3.7. The counter is loaded with the current value of N_{REF} during the previous conversion phase. The feedback signal is used to trigger counting events, whereas the reference signal with frequency f_{REF} is used as an enable signal. Each N_{REF} value corresponds to a particular target frequency. At the end of the detection phase, counting stops and the remaining counter value and sign, representing a frequency difference, are stored in a register for further processing during the conversion phase. The detector can therefore also be seen as a frequency-to-digital converter with its resolution limited to $1T_{FB}$. Additional signals for load and reset commands need to be supplied by the controller circuit that also instructs channel or application changes.

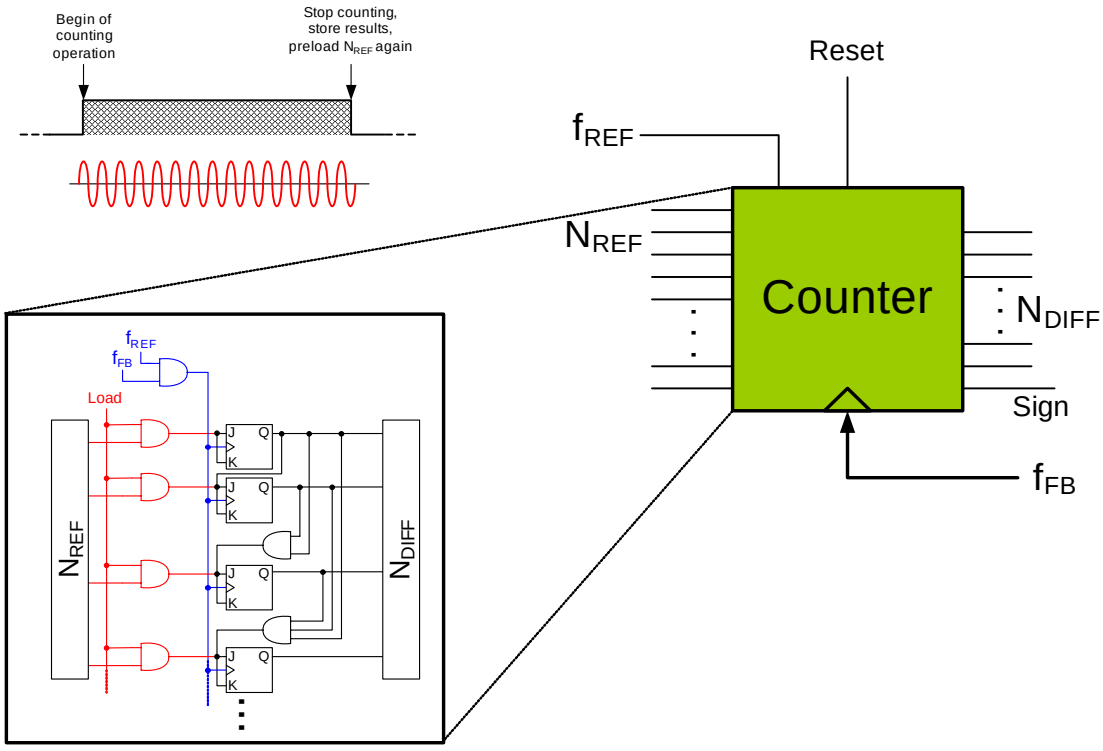


Figure 3.7: Detector implementation as counter in count-down mode. Prior to the detection phase, the counter is loaded with the current N_{REF} value.

Detector Functionality

The following derivations aim for a functional description of the detector. It should be noted that the reference inputs are considered to be ideal, i.e. the bit values of N_{REF} are assumed to be stable without glitches and f_{REF} originates from an external signal source such as a crystal oscillator or a SAW device. The effect of timing errors on the detector output will be illustrated later in this section. Considering figure 3.6, the number of completed feedback periods that can be counted during the detection phase, N_{cnt}, is determined by the ratio

$$N_{cnt} = \left\lfloor \frac{\alpha \cdot T_{REF}}{T_{FB}} \right\rfloor = \left\lfloor \frac{\alpha \cdot T_{REF}}{N \cdot T_{VCO}} \right\rfloor = \left\lfloor \frac{\alpha \cdot f_{VCO}}{N \cdot f_{REF}} \right\rfloor \tag{3.3}$$

with α again being the duty cycle factor, $0 < \alpha < 1$. Replacing periods with frequencies and taking the feedback division ratio N into account, the required bit width of the counter, B_m, is expresses as

$$B_m = \left\lceil log_2\left(\left\lfloor \frac{\alpha \cdot f_{VCOmax}}{N \cdot f_{REF}} \right\rfloor \right) \right\rceil \tag{3.4}$$

The value f_{VCOmax} in equation (3.4) is the highest designed oscillator output frequency, including possible frequency drifts. The ceiling function $\lceil \ldots \rceil$ in equation (3.4) originates from the assumption of binary processing.

For given values of α, T_{REF}, and N in equation (3.3), each value of N_{cnt} corresponds to a certain VCO frequency (though not vice versa, as the periods are counted in discrete time intervals). The values of N_{REF} are the expected, predetermined counter outputs within the possible range of N_{cnt}. At the end of the detection phase, the counter output $N_{DIFF} = N_{REF} - N_{cnt}$ represents a detected frequency difference. Larger VCO frequencies result in higher values of N_{cnt}. The maximum detected difference $N_{diff,max}$ is therefore given as

$$max(N_{DIFF}) = max(N_{REF} - N_{cnt}) = N_{cnt,H} - N_{cnt,L} \tag{3.5}$$

where $N_{cnt,H}$ and $N_{cnt,L}$ are the highest and lowest expectation values, respectively. Applying equation (3.3) to (3.5) leads to

$$max(N_{DIFF}) = \left\lfloor \frac{\alpha \cdot T_{REF}}{N \cdot T_{VCO,H}} \right\rfloor - \left\lfloor \frac{\alpha \cdot T_{REF}}{N \cdot T_{VCO,L}} \right\rfloor \tag{3.6}$$

Substituting frequencies for periods in equation (3.6) yields

$$\frac{\alpha \cdot (f_H - f_L)}{N \cdot f_{REF}} - 1 < max(N_{DIFF}) \leq \frac{\alpha \cdot (f_H - f_L)}{N \cdot f_{REF}} + 1 \qquad (3.7)$$

where f_H and f_L are the highest and lowest output frequencies for a particular band $\Delta f = |f_H - f_L|$ as shown in figure 3.8. The required bit width, B_{DIFF}, to represent possible differences at the detector output is then

$$\left\lceil log_2\left(\frac{\alpha \cdot (f_H - f_L)}{N \cdot f_{REF}} - 1\right)\right\rceil < B_{DIFF} \leq \left\lceil log_2\left(\frac{\alpha \cdot (f_H - f_L)}{N \cdot f_{REF}}\right)\right\rceil \qquad (3.8)$$

$$\left\lceil log_2\left(\frac{\alpha \cdot \Delta f}{N \cdot f_{REF}} - 1\right)\right\rceil < B_{DIFF} \leq \left\lceil log_2\left(\frac{\alpha \cdot \Delta f}{N \cdot f_{REF}} + 1\right)\right\rceil \qquad (3.9)$$

For a zero frequency difference, or differences smaller than the detector resolution, the counter output is zero. However, the VCO cannot be driven to the correct frequency by a zero voltage. N_{DIFF} therefore only represents a voltage change, ΔV_c, and not the final control voltage, V_c, itself. For the duration of detection and conversion, i.e. τ_{settle}, V_c is stored at the oscillator input.

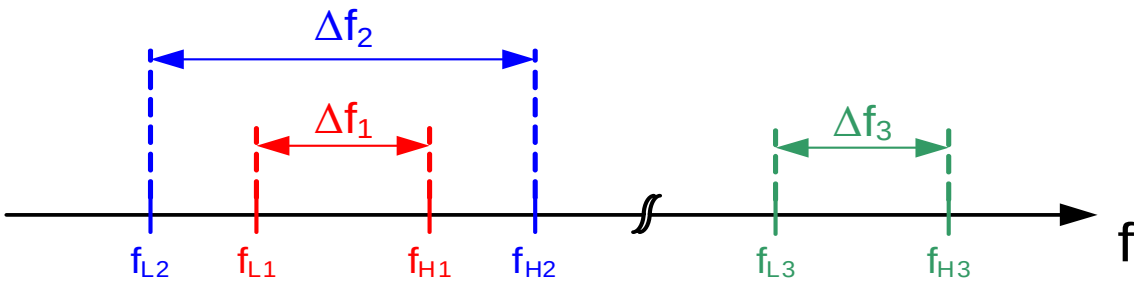


Figure 3.8: Definition of different spectra for frequency synthesis.

Application Trade-offs

The synthesizer architecture allows to trade off operational parameters to react to changing requirements from different applications. A first trade-off is that of settling speed, τ_{settle}, versus accuracy of the control voltage. As V_C is updated within one T_{REF}, the settling time is bound to the reference period. The most significant contribution to τ_{settle} is the detection phase ($\alpha \cdot T_{REF}$). Hence, the most effective way to reduce the set-

tling time of the synthesizer is to reduce T_{REF}, or an increase of f_{REF}, while N and α are kept constant. Shortening the detection phase also reduces the detector resolution, as fewer feedback periods are now counted. This will in turn reduce the accuracy of the analog control voltage. After hardware implementation, the bit width of the digital blocks is fixed, only the used range of processed values changes. If for instance only 10 of 12 available bits are used, then the 2 leading MSBs are zero. The digital reference N_{REF} and DAC conversion gain need to be adjusted to accommodate for the different voltage equivalent of one LSB. The time-accuracy trade-off also applies in reverse. A longer detection phase allows for higher detector resolution. This trade-off enables the synthesizer to operate with variable output frequency steps: For instance fast settling with coarse frequency step size (e.g. tracking of channel switching) and slow settling with small frequency variations (e.g. maintaining of a target output rate).

A second trade-off apparent from equation (3.8) is between settling speed and detection range, Δf. Also here it is assumed that α and N are kept constant. If another application requires a different detection range, say $\Delta f_2 = \beta \cdot \Delta f_1$, the synthesizer can accommodate this change if the reference frequency is modified to $f_{REF,2} = f_{REF,1}/\beta$. As f_{REF} translates into settling time, the trade-off is between wide band synthesis with slower settling and a small band, but fast settling operation. Again, the values of N_{REF} need to be adjusted accordingly to maintain detector resolution. Shifting the synthesizer application from Δf_1 to Δf_3, only influences internal counter bit width B_m, but not its B_{DIFF} if $\Delta f_1 = \Delta f_3$.

A third trade-off between Δf and detection accuracy becomes feasible if the counting step size is made variable. An increased oscillator range can be covered for larger counter steps. For instance, only every second feedback edge will trigger a counting event, while N_{REF} and f_{REF} are kept constant. A one LSB change would then represent a larger voltage step, degrading the resolution of the detector voltage. This is effectively a variation of the division ratio.

Detector Limitations

The detection process has inherent limitations. The frequency discrimination process is confined to the detection phase. During the conversion phase, the counter is inhibited, which means that is it blind to frequency changes at the output. This blind zone, δ_{bz}, is the time of the conversion phase and can be expressed as:

$$\delta_{bz} = (1 - \alpha) \cdot T_{REF} \tag{3.10}$$

This differs from the detection mechanism in phase-locked loops. Their detector output is updated with the reference rate. In order to drive the VCO, the steady state phase error in a PLL is set to a fixed, non-zero value, e.g. to π. Phase changes occurring after the steady state phase error will be accounted for in the following reference cycle. For the same reference frequency, the blind zone in the proposed architecture is therefore as large as in traditional PLLs.

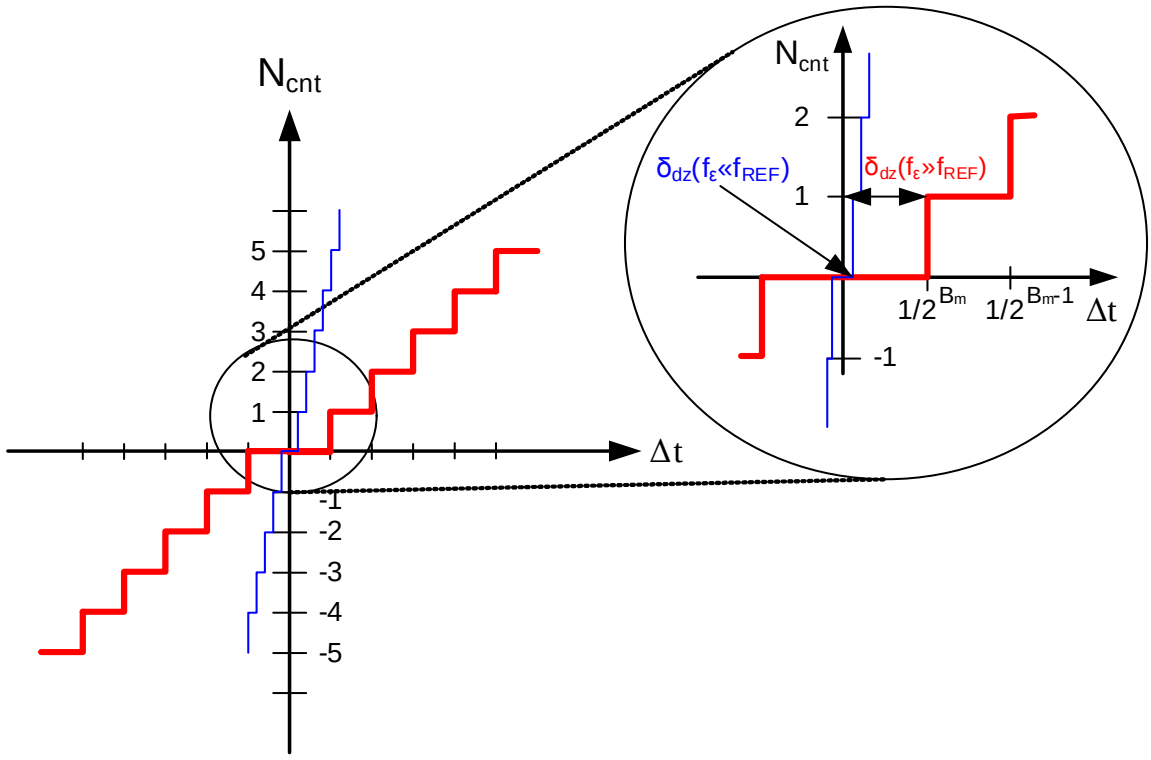


Figure 3.9: Dead zone δ_{dz} for different appearance rate f_{ε}, as well as detector output step size

Noise inflicting the synthesizer will alter the feedback period length T_{FB}, thereby impacting the counter result. The number of feedback periods occurring during the detection phase is compared to the digital reference value. If period errors appear at a rate f_{ε}, that is comparable to the reference signal, $f_{\varepsilon} \cong f_{REF}$, the timing error magnitude needs to exceed one T_{FB} in order to cause a detector output change.

$$\delta_{dz}(f_{\varepsilon} \approx f_{REF}) \geq T_{FB} = \frac{N}{f_{VCO}} \tag{3.11}$$

However, period errors that appear often compared to the reference signal, i.e. $f_\varepsilon >> f_{REF}$, will be summed during the detection phase, up to N_{cnt} times. This means that a period difference as small as T_{FB}/N_{cnt} causes the detector output to change.

$$\delta_{dz}(f_\varepsilon \gg f_{REF}) \geq \frac{T_{FB}}{N_{cnt}} = \frac{N^2 \cdot f_{REF}}{\alpha \cdot f_{VCO}^2} \tag{3.12}$$

The error δ_{dz} from equations (3.11) and (3.12) is defined as the dead zone of the detector. That means that δ_{dz} is the smallest detectable timing error. The property of higher sensitivity to errors that appear often during the detection phase is consistent to their higher impact on the oscillator output frequency. It should be noted that f_ε is the frequency of frequency error appearance, not the frequency difference itself. The effect of jitter will be illustrated in more detail below. High rate period errors with opposite sign will largely chancel out. Equations (3.11) and (3.12) provide a design guideline to fulfil accuracy requirements of target applications. Figure 3.9 depicts both, detector dead zone and its step wise output change due to period errors Δt.

As T_{FB} varies with the oscillator frequency, the synthesizer needs to be designed such that its resolution still fulfils the requirements for frequency track and hold operations at its lowest output rate and for all targeted applications.

Detector Timing Errors

So far, description of detector functionality assumed ideal conditions. Two types of timing errors impacting the detection process are identified. These error sources origin from phase offsets between the detector inputs and from jitter in the feedback signal.

For the following analysis, the inputs to the detector are assumed to be square wave signals. The analysis can, however, be extended to cover other signals such as sine waves, and no generality is lost. It will further be assumed that the reference time signal is provided by an ideal signal source, i.e. it is free from phase drifts and jitter components.

The feedback signal can, however, be subject to a time shift with respect to the reference. This results in a delay for the first triggering impulse in the counter and corresponds to a constant time shift during the i^{th} detection phase. Denoted as $t_\phi(i)$, this phase offset is depicted in figure 3.10. A second type of detector error arises from jitter, i.e. high frequency variations on each individual feedback edge during the i^{th} detection phase. Jitter errors are shown as coloured area in figure 3.10. These errors originate

from timing variations in oscillator and feedback divider. They are here denoted as $\delta_j(i)$, with j = (1, 2, … , k) being the number of feedback edged within the i^{th} detection phase. Though the magnitude of each jitter contribution is small compared to T_{FB}, the amount of jitter will sum up during detection. In worst case, the jitter components have equal sign and accumulate over $T_{REF}/2$, thereby contributing to detector errors.

Counting starts with the reference duty cycle at time t_0. Only rising feedback edges at $t > t_0$ trigger a counting event. Counting finishes at $t = t_3$, with the last accounted feedback edge occurring at $t_2 \leq t_3$. Outside the detection window, i.e. for $t > t_3$, the counter is idle. This limits possible jitter accumulation in the loop to a duration of $T_{REF}/2$, as the loop will appear open during the conversion period.

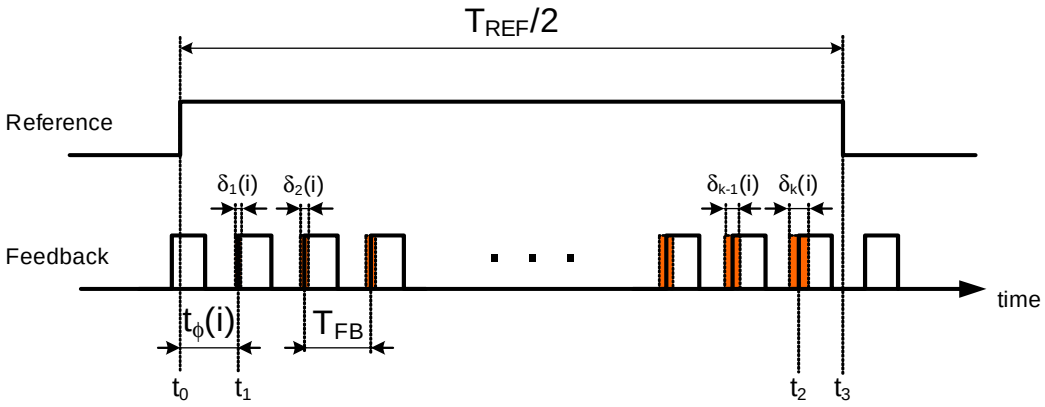


Figure 3.10: Time offset and jitter contribution in detector.

With the assumptions above, the number of actual trigger events, M, is determined by the two inequalities (3.13) and (3.14):

$$M \cdot T_{FB}(i) + t_{\phi}(i) + \sum_{k=1}^{M} \delta_k(i) < \frac{T_{REF}}{2} \tag{3.13}$$

$$(M+1) \cdot T_{FB}(i) + t_{\phi}(i) + \sum_{k=1}^{M+1} \delta_k(i) > \frac{T_{REF}}{2} \tag{3.14}$$

Solving (3.13) and (3.14) for M yields

$$M < \frac{T_{REF}}{2T_{FB}(i)} - \frac{\sum_{k=1}^{M} \delta_k(i)}{T_{FB}(i)} - \frac{t_\phi(i)}{T_{FB}(i)} \tag{3.15}$$

and

$$M > \frac{T_{REF}}{2T_{FB}(i)} - \frac{\sum_{k=1}^{M+1} \delta_k(i)}{T_{FB}(i)} - \frac{t_\phi(i)}{T_{FB}(i)} - 1 \tag{3.16}$$

From expressions (3.15) and (3.16), the number of rising edges in the presence of phase offsets and jitter errors is derived as

$$M(i) = \left\lfloor \frac{\frac{T_{REF}}{2} - t_\phi(i)}{T_{FB}(i) + \overline{\delta_M(i)}} \right\rfloor \tag{3.17}$$

where $\overline{\delta_M(i)}$ is the mean of the jitter components during the ith detection phase. Due to the large number of counting events, and assuming white Gaussian noise distribution for the jitter, this mean value is zero:

$$\overline{\delta_M(i)} = \frac{1}{M} \sum_{k=1}^{M} \delta_k(i) = 0 \tag{3.18}$$

Then, the jitter contribution in equation (3.17) can be neglected. However, if error sources cause the mean value to drift, e.g. due to temperature changes or power supply variations, then $\overline{\delta_M(i)}$ contributes to M(i). A deviation in M(i) due to timing errors can be observed and compensated if

$$t_\phi(i) + \sum_{k=1}^{M} \delta_k(i) \geq \frac{1}{2B_m} \tag{3.19}$$

Even a small change in jitter mean is identified, as its effect is amplified by a factor equal to the number of rising edges within the detection phase. The final detector output including timing uncertainties is given as:

$$N_{DIFF}(i) = N_{REF}(i) - M(i) \tag{3.20}$$

3.2.3 Conversion Process

With the beginning of the conversion phase, N_{DIFF} needs to be converted into an analog voltage. Digital-to-analog conversion can be realized with different converter architectures. An apparent DAC implementation is the addition of binary weighted voltages, e.g. using resistors or capacitors. But this requires the value of the passive component to double for each additional bit. A more effective way to convert digital information into an analog output voltage are for instance R/2R networks. The Thevenin resistance to ground seen from any point in the ladder towards the LSB is one R. This makes the converter independent of the absolute value or R. A change in the reference voltage changes the converter gain. However, matching of the resistor values is critical. Expensive laser trimming of the resistors is often needed to achieve accuracy requirements.

Using currents instead of voltages, adding is a property that comes for free. A current proportional to the sum of all input currents, will automatically flow through the summing node, avoiding the need of many passive components. The drawback, however, is the need for precisely weighted current sources and large current amplitudes in the branches representing the higher bit values.

The principle of adding currents is often used together with thermometer code, where monotonicity reduces the possibility of glitches at the output. Each source contributes with exactly the same amount of current and no precise binary weighting is needed. However, difficulties arise from the large number of required current sources. For instance, a 12 bit thermometer DAC requires 4096 individual sources, demanding large die area. Matching becomes a major challenge for high resolutions. More details about DAC architectures and their circuit implementations can be found for instances in [Johns1997].

In the proposed architecture, the DAC is implemented using a 1-bit converter and a digital sigma-delta ($\Sigma\Delta$) modulator as depicted in figure 3.11. Trading off resolution in time for that in amplitude, the $\Sigma\Delta$ modulator converts the parallel input bits of width B_{DIFF} of low frequency to a bit stream of width $B_{\Sigma\Delta} = 1$ at high output rate. The subsequent 1-bit converter integrates the stream of single bits, thereby simplifying the converter implementation. The resulting analog output corresponds to the correction voltage for the VCO and is provided at discrete time instances, τ_{DAC}.

The sigma-delta modulator and the discrete integrator offer high flexibility for parameter changes like conversion gain and resolution with low circuit complexity. This combination is therefore highly suitable for multi-standard applications. Single bit conversion has the additional advantage of being inherently linear. The conversion is

accomplished using mostly fast digital circuits, reducing the number of analog components that are susceptible to manufacturing tolerances and noise.

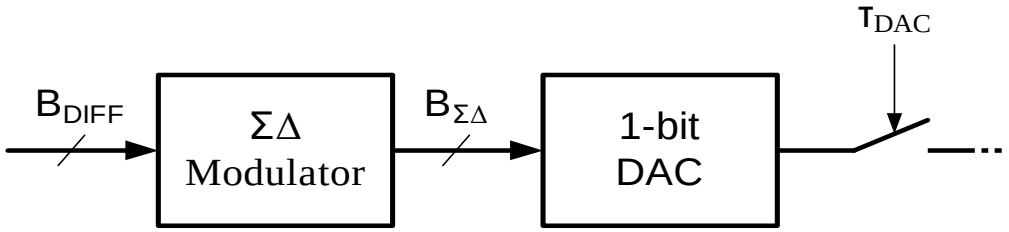


Figure 3.11: Proposed implementation of digital-to-analog converter using a digital sigma-delta converter and a 1-bit DAC

Sigma-Delta Modulator

The sigma-delta modulator is implemented as an error truncation noise shaper, as presented in [Norsw1997]. It comprises only digital blocks, i.e. an adder and a register. Both are clocked with the feedback signal, avoiding the need for additional external clock supplies.

As the objective of the modulator here is parallel to serial bit conversion, a first order architecture [Norsw1997] was chosen for simplicity as shown in figure 3.12. At system start up, register and adder are reset to zero. For the i^{th} conversion phase, N_{DIFF} is a constant adder input. Since the adder sums two values of equal bit width, its sum is 1 bit wider than the inputs. If the most significant bit (MSB) of the sum $y_j = 1$, then addition has reached the overflow threshold S_{th}

$$S_{th} = 2^{B_{DIFF}} \tag{3.21}$$

Then, the MSB is truncated from the sum and used as the 1-bit output y_j. All remaining bits representing the truncation error ε_j

$$\varepsilon_j = (N_{DIFF} + \varepsilon_{j-1}) - \left(y_j \cdot 2^{B_{DIFF}}\right) \tag{3.22}$$

are fed back via the register. The value of ε_j will be added to N_{DIFF} during the following clock event (j+1).

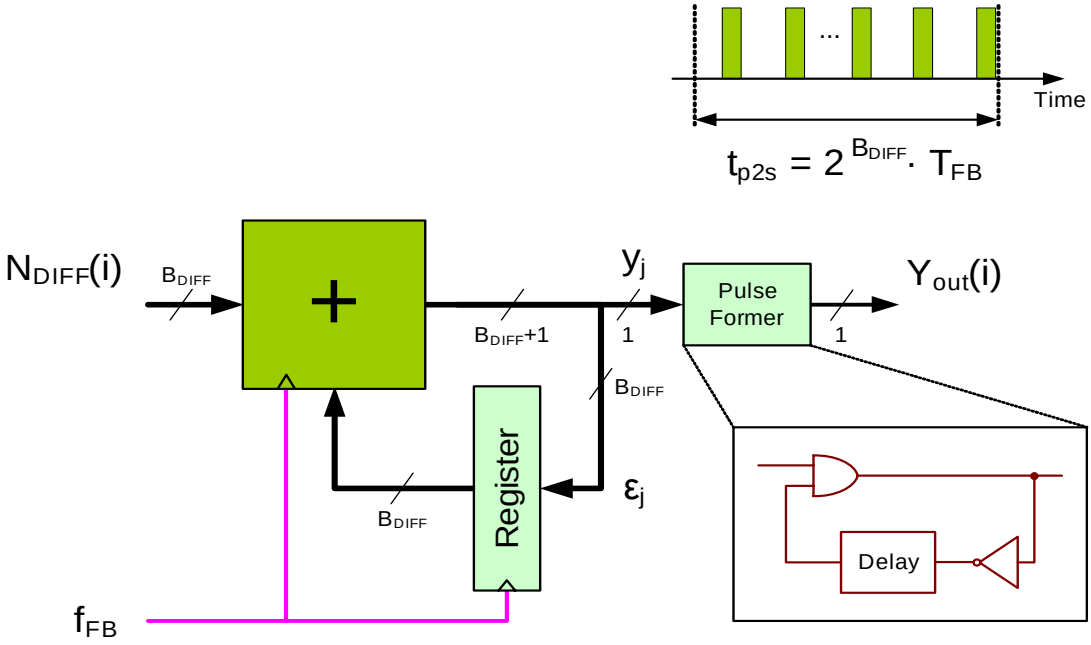


Figure 3.12: Implementation of parallel-to-serial bit converters with sigma-delta modulator and pulse former

Since the feedback signal is used to clock the modulator, the pulse width of y_j, and hence the integration duration in the 1-bit DAC, varies with f_{FB}. To unify the pulse width, a pulse former with a fixed and known delay is introduced as shown in figure 3.12. The modulator output $Y_{out}(i)$ is a serial pulse stream with

$$Y_{out}(i) = \sum_{j=1}^{2^{B_{DIFF}}} y_j(i) = N_{DIFF} \tag{3.23}$$

This stream contains exactly N_{DIFF} pulses within the time needed for parallel to serial bit conversion, t_{p2s}. After each t_{p2s}, the output bit pattern repeats itself and the register content returns to its initial, i.e. zero value. Hence the required time needed for parallel-to-serial conversion is

$$t_{p2s} = 2^{B_{DIFF}} \cdot T_{FB} \tag{3.24}$$

The statements above and equations (3.23) and (3.24) are verified with the following formal proof:

Condition 1: The number of input bits shall be *B*, and the number of performed clock cycles is assumed to be $n = 2^B$ with $B \in \mathbf{N}$.

Condition 2: The initial register value is zero.

Condition 3: The input value *X* to the digital sigma-delta modulator remains constant within each conversion phase, i, and it is a natural number limited by the bit width, i.e.

$$X(i) = \text{constant} \; \forall \; n, \; X \in \mathbf{N}, \; X \leq 2^B \tag{3.25}$$

The function performed by the bit truncation in the loop is the modulo-2^B operation (where modulo is also expressed by the "%" symbol) of the sum of input and previous register value during each clock cycle. This sum, S_{reg}, is stored again in the register and can be expressed as

$$S_{reg} = ((\,(X\%2^B) + X)\%2^B + X)\%2^B + \ldots \tag{3.26}$$

After n clock cycles, this sum becomes

$$S_{reg} = \left(\sum_{i=1}^{n} X_i \right) mod 2^B \tag{3.27}$$

From condition 3, X is constant and the S_{reg} can be rewritten as

$$S_{reg} = (X \cdot n)\%2^B \tag{3.28}$$

Inserting the value of n from condition 1 leads to

$$S_{reg} = (X \cdot 2^B)\%2^B = 0, \;\; X \in \mathbf{N} \tag{3.29}$$

This proves that the register content of the loop will return to zero after $n = 2^B$ clock cycles if its initial value is zero. Applying the contra-positive law, it can also be concluded that for any register value $S_{reg} \neq 0$, the number of performed clock cycles is not an integer multiple of 2^B

$$n = 2^B \rightarrow S_{reg} = 0 \quad \text{and} \quad S_{reg} \neq 0 \rightarrow n \neq 2^B \tag{3.30}$$

Each overflow of the modulo operation results in an output pulse $y_j > 0$. Therefore, the total number of output pulses Y_{out} from figure 3.12 within n clock cycles is

$$Y_{out} = \frac{n \cdot X}{2^B} \tag{3.31}$$

Applying again condition 1 leads to

$$Y_{out} = \frac{2^B \cdot X}{2^B} = X \tag{3.32}$$

Hence, the total number of output pulses within 2^B cycles is equal to the input value, proving equation (3.23). Q.E.D. Figure 3.13 depicts an architecture to for implementation of 1-bit DAC and integrator circuit.

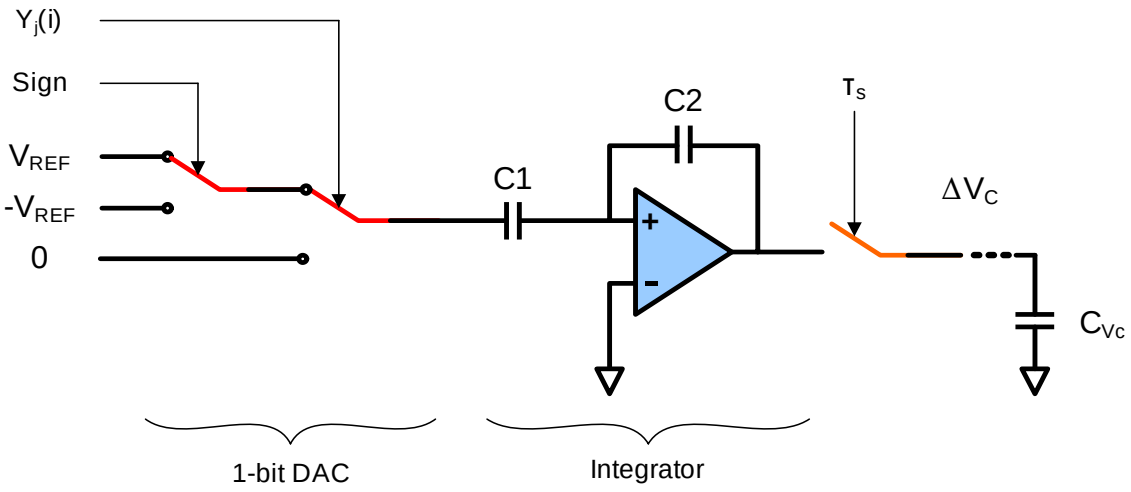


Figure 3.13: 1-bit DAC implementation (single ended example) using switches for inputs of $\pm V_{REF}$ and zero and an integrator.

3.2.4 Settling Time Limit

The serial bit stream y_j completes after $2^{B_{DIFF}}$ feedback clock cycles. D/A conversion and integration are performed concurrently with the bit stream generation. The final serial bit requires one additional clock cycle for integration. Hence, the sigma-delta modulator inhibits after $t = t_{p2s}$, whereas integration finishes one feedback cycle later at $t = t_{p2s} + 1 \cdot T_{FB}$. Using equation (3.24), the minimum settling time, τ_s, is therefore determined as

$$\tau_s = \frac{T_{REF}}{2} + T_{FB}\left(2^{B_{DIFF}} + 1\right) + \tau_{VCO} \tag{3.33}$$

Here, τ_{VCO} is the delay needed for the VCO itself to adjust to the new control voltage. The first term in equation (3.33) accounts for the detection phase, the second term for conversion into an analog voltage using the described sigma-delta modulator and a single bit DAC with integrator. Following the definitions of figure 3.6, the limit for the settling time is given as

$$\tau_{settle} = \tau_s < T_{REF} = \frac{1}{f_{REF}} \tag{3.34}$$

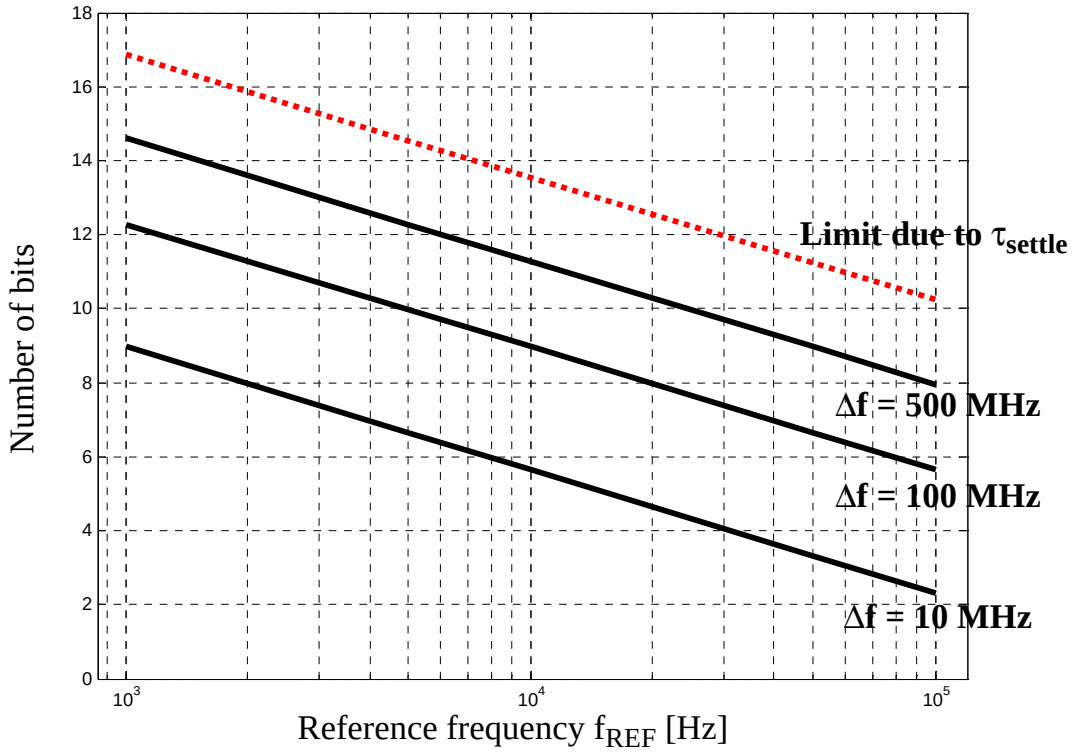


Figure 3.14: Maximum number of bits (red dotted line) according to equation (3.34) and detector bit width B_{DIFF} (black lines) due to f_{REF}. Simulation for parameters N=10 and f_{VCO}=2.4GHz.

The impact of equation (3.33) is shown in figure 3.14. The dotted red line indicates the maximum detector resolution in bits that can be converted within the settling time limit of equation (3.34). The three black lines show the detector output resolution re-

quirement of equation (3.8) for bandwidths Δf of 10 MHz, 100 MHz, and 500 MHz, respectively. Here, a division factor of N = 10, output frequency f_{VCO} = 2.4 GHz and $\tau_{VCO} \approx 0$ were assumed. The reference frequency range on the abscissa corresponds to settling time limits of 1 ms, …, 10 µs. Two conclusions can be drawn from figure 3.14. Firstly, sufficient conversion time margin exists to convert the detector bits of width B_{DIFF} into an analog voltage for a wide range of synthesizer bandwidths. Secondly, for a given settling time limit, figure 3.14 presents the maximum number of bits that can be counted and converted within the limit of equation (3.34).

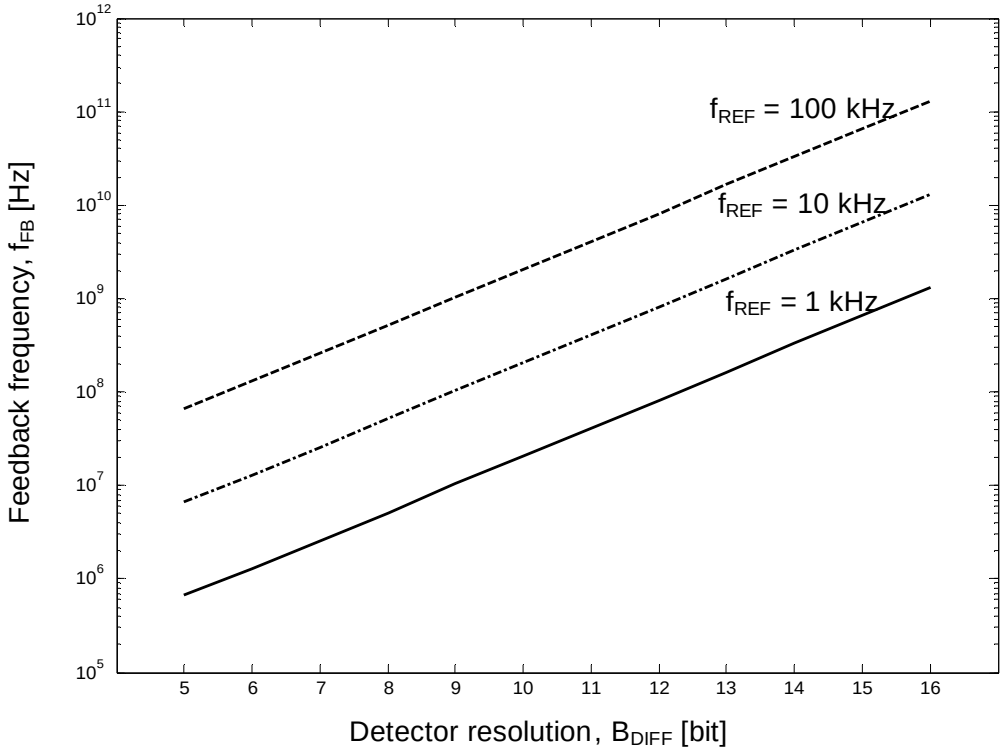


Figure 3.15: Minimum feedback rate versus detector resolution for various reference frequencies of 1 kHz, 10 kHz and 100 kHz, respectively.

The settling time of equation (3.33) can be rewritten using the actual output frequency, f_{osc}, and neglecting τ_{VCO}

$$\tau_S(f_{osc}) = \frac{1}{2f_{REF}} + \frac{N}{f_{osc}}\left(2^{B_{DIFF}} + 1\right) \qquad (3.35)$$

Equation (3.35) constrains the synthesizer output frequency to ensure that digital-to-analog conversion will complete during the conversion phase. Shown in figure 3.15

is the minimum output frequency versus detector resolution for three reference frequency values.

The settling time limit of equation (3.35) holds only true if the frequency difference between f_{osc} and the target frequency, $f_L < f_{target} < f_H$, varies within the designed bandwidth, i.e. $f_{diff} = |f_{osc} - f_{target}| \leq \Delta f$ so that

$$\tau_{settle}(f_{diff} \leq \Delta f) = \tau_s(f_{osc}) \tag{3.36}$$

For $f_{diff} > \Delta f$, the achievable frequency adjustment within one T_{REF} corresponds only to the maximum detector output. The remaining difference must be compensated for in the following reference periods, leading to

$$\tau_{settle}(f_{diff} > \Delta f) = N_f \cdot T_{REF} + \tau_s(f_{osc} \pm N_f \cdot \Delta f) \tag{3.37}$$

where N_f is determined by the integer ratio of actual to the designed frequency range

$$N_f = \frac{|f_{osc} - f_{target}|}{\Delta f} - 1 \;, \quad N_f \in N, N_f > 0 \tag{3.38}$$

Presented in figure 3.16, two ranges are defined with respect to settling time. Settling time within the *lock range* follows equation (3.36) regardless of f_{target}. The bands

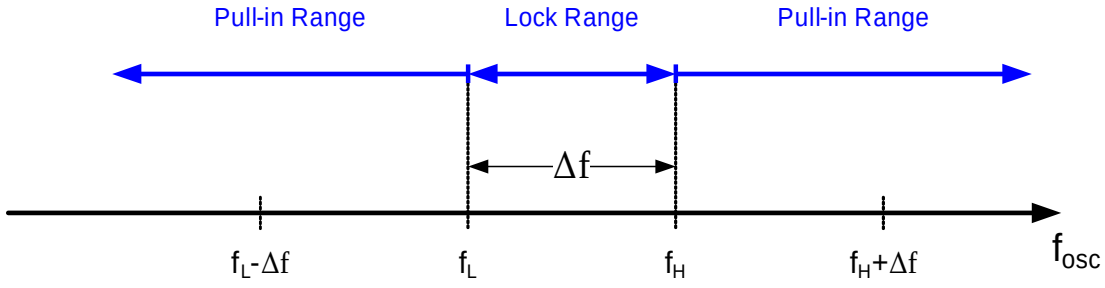


Figure 3.16: Application and detection range with defined settling time, and unlimited pull-in range with uncertain settling time.

outside the lock range are defined as *pull-in range*, as f_{osc} is slowly pulled back into the targeted frequency band. The settling time then follows equation (3.37).

Scenarios where f_{osc} is out of the designed band are for instance start up conditions, changes of synthesizer application or the presence of large supply voltage variations.

In theory, there is no limit of how far off f_{osc} can be from its target, suggesting an unlimited pull-in range. Only the time required to pull the oscillator back into the band $f_L < f_{osc} < f_H$ will increase. However, control voltage amplitude restrictions and speed constraints of the involved circuitry will put practical limits on the pull-in range.

Phase Lock & Pull-In Range

The presented frequency synthesizer does not lock to the phase of the reference signal. Direct application in wireless radio communications is therefore limited to noncoherent communication systems.

Phase lock can however be achieved with little additional effort. One alternative is to apply the control voltage change from the DAC output to the VCO with the rising edge of the reference signal, thereby synchronising reference and oscillator output. The VCO reaches its target frequency after an additional delay of τ_{VCO}. However, this τ_{VCO} is a function of frequency step size $\tau_{VCO} = f(\Delta f)$, leading to small variations of the total settling time and hence, to phase errors. Furthermore, changes of f_{VCO} will fall into the succeeding detection phase and cause counter errors.

A second way to achieve phase lock is the addition of a delay-locked loop at the oscillator output. This DLL does not require frequency tunability. It only adds delay to align the output phase of the frequency synthesizer to another reference input, allowing also application for coherent communication schemes. The tuning of phase delay will limit the final phase noise performance of this solution.

3.3 Simulations and Results

With the descriptions of the previous sections, the parameter trade-offs and limitations, what are the possible applications of the suggested frequency synthesizer? And how does the performance of this new architecture compare with existing synthesizers in a multi-standard and multi-band environment?

Figure 3.17 shows a revised architecture of the synthesizer shown in figure 3.5. The generic DAC is now replaced by a digital sigma-delta modulator and a 1-bit DAC. Its digital blocks are clocked by the feedback signal. The simulation results presented below refer to this architecture. In order to comply with output frequency tolerance limits

placed by the application, the control voltage, V_c, needs to satisfy a certain signal-to-noise ratio.

The output frequency tolerance, f_{tol}, and the VCO sensitivity, K_{VCO}, determine the largest acceptable voltage variation at the oscillator input. With a given input control voltage range, $\Delta V_{c\,max}$, the required control voltage accuracy, SNR_{Vc} expressed in dB, becomes

$$SNR_{Vc} = 20 \cdot log_{10}\left(\frac{K_{VCO} \cdot \Delta V_{cmax}}{f_{tol}}\right) \tag{3.39}$$

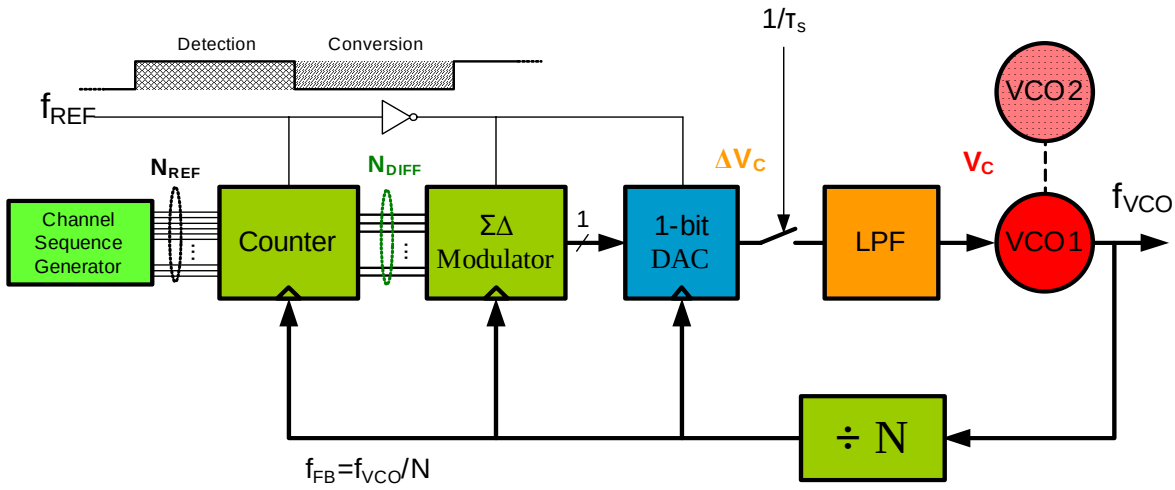


Figure 3.17: Revised architecture from figure 3.5: Frequency synthesizer comprising digital sigma-delta modulator and 1-bit DAC.

As K_{VCO} is defined as the ratio of output frequency range, Δf, to its input voltage range $\Delta V_{c\,max}$, equation (3.39) simplifies to

$$SNR_{Vc} = 20 \cdot log_{10}\left(\frac{\Delta f}{f_{tol}}\right) \tag{3.40}$$

This comes as no surprise, as the input resolution to the oscillator cannot be lower than its output resolution requirement. The same holds true for the preceding blocks of the frequency synthesizer. The required detector resolution must therefore provide at least a resolution of SNR_{Vc}. This resolution requirement is depicted in figure 3.18 for different values of K_{VCO} and a control voltage range of $\Delta V_{c\,max}$ = 1 Volt.

This synthesizer architecture targets applications covering multiple communication standards and different frequency bands. The proposed architecture is able to support several voltage controlled oscillators while all other building blocks of the loop are re-used. The author suggests to employ several VCOs, for instance one for each targeted frequency band. Using few oscillators each covering a moderate bandwidth instead of one wideband VCO obviously presents an area penalty. However, as seen from figure 3.18, this is offset by reduced resolution requirements. Furthermore, the design task is simplified and already existing IP from previous single standard applications can be employed.

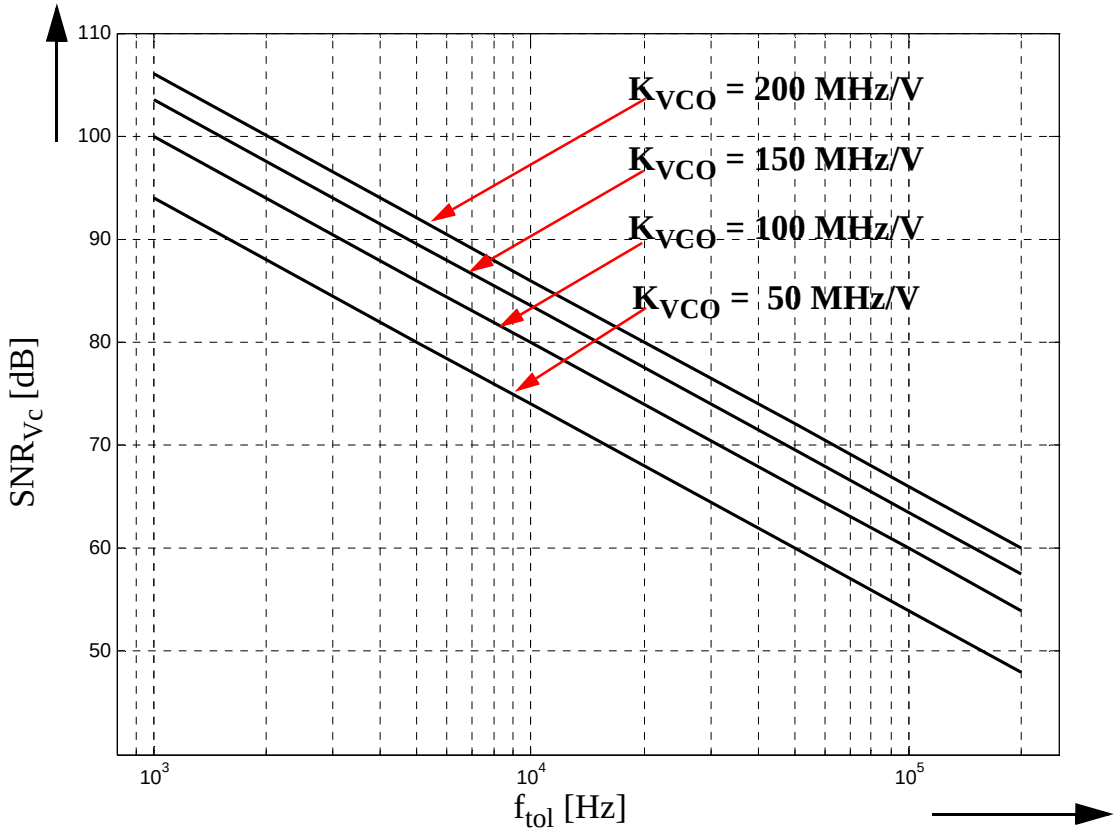


Figure 3.18: Required control voltage resolution, SNR_{Vc} in [dB], versus output tolerances, f_{tol} in [Hz], for various oscillator sensitivities, K_{VCO}, and a voltage range of $\Delta V_{c\,max}$ = 1V.

Table 3 lists synthesizer requirements for bandwidths, frequency accuracy and settling time limits for selected applications. Here, $\Delta V_{c\,max}$ = 1 Volt and a linear value for K_{VCO} sensitivity over the entire output range were assumed.

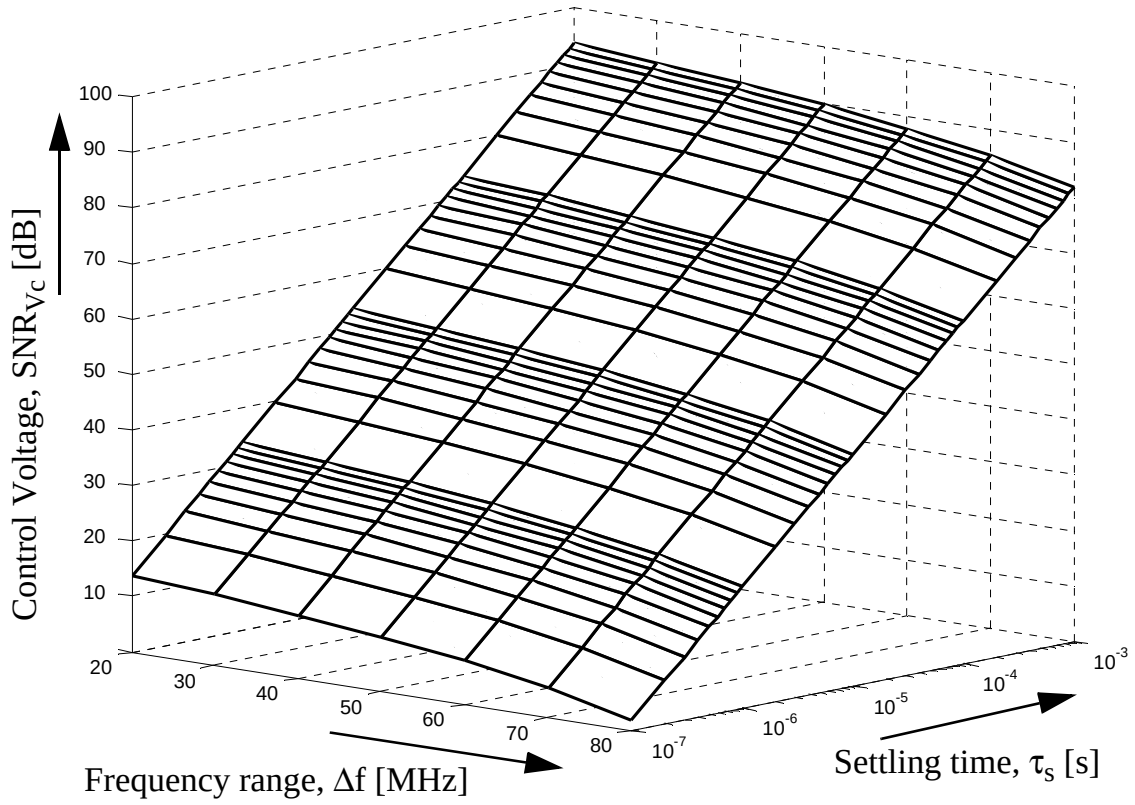


Figure 3.19: Design space for frequency synthesizer architecture, trading off settling time, frequency range and control voltage accuracy (SNR).

The design space of the frequency synthesizer is demonstrated in figure 3.19. The graph shows a mesh grid for SNR_{Vc} (in dB), that can be delivered by the architecture for given values of frequency range, Δf, and settling time limits, τ_s. The proposed architecture is suitable for all synthesizer applications that comply to the parameter space $\{SNR_{Vc}, \Delta f, \tau_s\}$ under the plotted surface. Its parameters can be traded off with sufficient control voltage resolution. A larger SNR_{Vc} is for instance possible for a longer settling time.

The resolution for very short settling times is restricted to only a few bits. This is not enough for sustaining a determined frequency by direct voltage control. However, the condition of fast adjustments is practical for implementation of coarse, long range frequency steps (band shifts). It also provides means for fast band selection at power start up. It should be noted that this graph does not include limitations posed by noise im-

pacting the analog circuitry, but rather presents the capabilities and flexibility of this synthesizer architecture.

Table 3: Synthesizer specifications for selected standards

	Application band	Frequency Accuracy	Settling Time Limit	SNR_{Vc}
Bluetooth	2400-2485 MHz	± 20 ppm (± 48 kHz)	312 µs	65 dB (11 bit)
802.11b	2400-2485 MHz	± 25 ppm (± 60 kHz)	224 µs	63 dB (11 bit)
Hiperlan2	5150-5350 MHz	± 20 ppm (± 103 kHz)	1 ms	66 dB (11 bit)

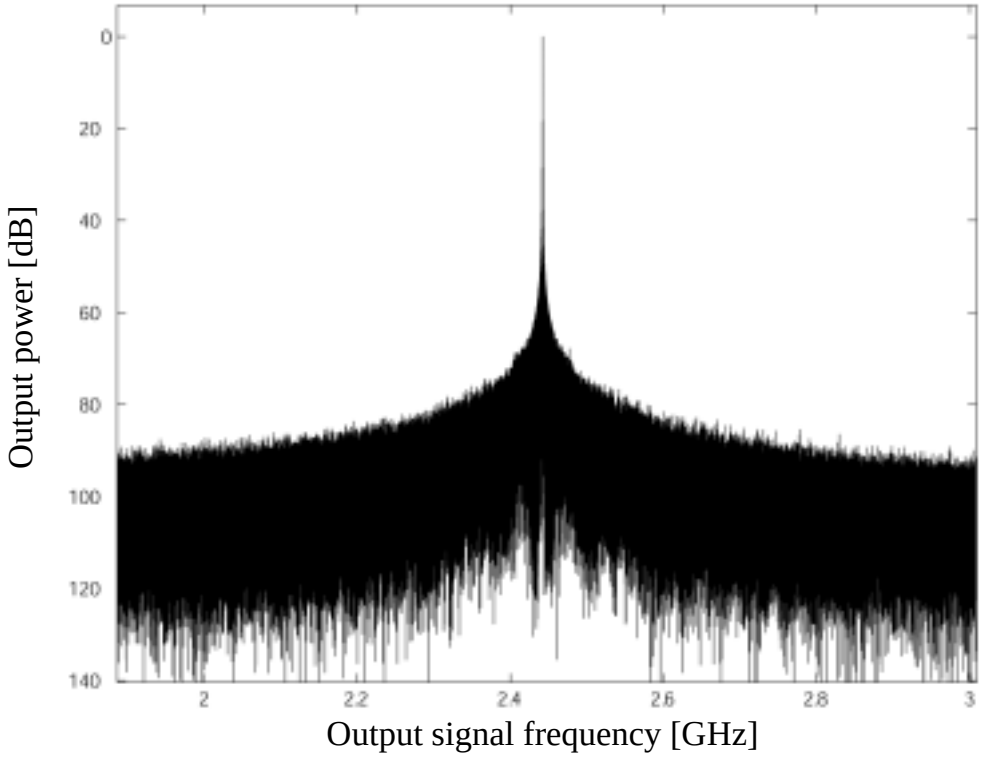


Figure 3.20: Simulated output spectrum of the frequency-locked loop for the example of f_{VCO} = 2.44 GHz, σ = 1 ps, f_{REF} = 100 kHz, and ΔN_{DIFF} = 1 LSB

Functionality and performance of the frequency synthesizer were simulated using Matlab and Simulink for applications in the ISM band. Figure 3.20 shows the synthesizer output spectrum for the example of output frequency 2.44 GHz and reference signal f_{REF} = 100 kHz. The detector output resolution in this simulation was 9 bit.

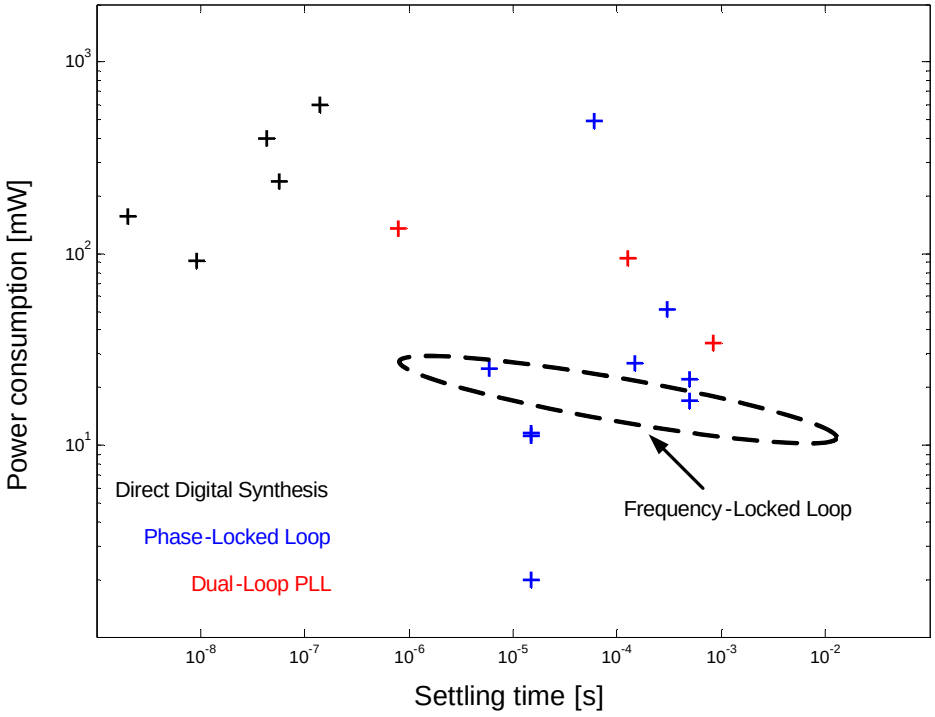


Figure 3.21: Estimated power versus settling time performance of frequency-locked loop architecture compared to reported phase-locked loops (blue), dual-loop PLLs (red) and direct digital synthesizers (black).

The oscillator was assumed to cover 85 MHz range with a control voltage range of 1 Volt. To examine the synthesizer performance in the presence of timing errors as derived in section 3.2.2, a detector error of ΔN_{DIFF} = 1 LSB in each detection phase and a jitter standard deviation in the feedback signal of σ_{jitter} = 1 ps were considered for this simulation. The time for the new control voltage to be computed was fount to be $\tau_{settle} \cong 7.2$ µs. Since this synthesizer does not perform phase alignment to the reference signal by more than 1 LSB of the detector resolution, only a modest phase noise performance of -90 dBc/Hz at a 5 MHz offset from the carrier was achieved.

The faster any synthesizer settles to a new target frequency, the more power is consumed. This is due to additional gain needed to speed up circuit operation. The power

consumption of the proposed synthesizer comprises digital operations, P_{dig}, [Dally1998], [Rabae1996], and power for analog circuits.

$$P_{dig} = C_{load} \cdot V^2 \cdot f_{clk} \cdot \gamma \tag{3.41}$$

Here, C_{load} is the capacitive load of the logic, V is the supply voltage, f_{clk} represents the operating frequency and γ is a switching duty factor with $\gamma < 1$, as not all gates switch at the same time. It is furthermore assumed that the power consumption for the VCO dominates over the analog integrator and the low-pass filter.

Counter and sigma-delta modulator comprise about the same number of gates running at speed f_{FB}. But they do not perform simultaneously, reducing the overall needed power. Figure 3.21 presents the estimated power consumption of the complete synthesizer versus its settling time performance. The detector accuracy was fixed to B_{DIFF} = 10 bits. Further parameters are described in table 4.

Table 4: Power estimation parameters and simulation values

Parameter	Value Range
Number of gates	300
Average fan-out/gate	2
Gate + fringing capacitance	$838 \cdot 10^{-5}$ pF/µm^2
Gate length, L	0.18 µm
Gate width, W	0.25 µm
Gate input capacitance	1.5 fF
Settling time, τ_{settle}	1 µs … 10 ms
Feedback clock, f_{FB}	2050 MHz … 205 kHz
Supply voltage, V	1.8 Volt
Switching duty factor, γ	0.5
Power of digital circuits	5 mW … 500 µW
VCO + Divider	10 mW

The settling time requirement determined the needed feedback rate. The estimated performance is compared to synthesizers reported in literature in recent years for

phase-locked loops and direct digital synthesizers [Yuen1997], [Crani1998], [Filio1998], [Vankk1998], [Yamag1998], [Morte1999], [Rhee2000], [Jiang2002], [Lee2001], [Tang2001], [Yan2001], [Herna2002], [Kan2002], [Wahee2002], [Fahim2003a], [Fahim2003b], [Toros2003]. It can be observed that the estimated power consumption of the digital processing blocks approaches the value of the VCO only for settling times close to 1 μs. For longer settling times, the VCO dominates the power consumption by at least one order of magnitude.

4. Multi-Standard ADC

This chapter begins with definitions and a brief introduction of data converters. This is followed by descriptions of the concept and motivation for a dual-standard ADC. The identification of converter performance requirements and the sigma-delta modulator architecture are then derived from standard specifications and sigma-delta properties. The design of a decimation filter, needed to complete the sigma-delta ADC is mentioned before simulation results are presented.

4.1 Data Converter Introduction

Natural signals in our world, like for instance electromagnetic waves, light, or sound are of analog, continuous nature, yet most processing of these signals is done in the digital realm. Hence, data converters are needed to mediate between these domains. The output of an analog-to-digital converter (ADC) is characterized by bit representations of time discrete, i.e. sampled signal levels. A digital-to-analog converter (DAC), on the other hand, defines analog output levels to corresponding digital inputs. The number of analog-digital data pairs is called the resolution of the converter, and is expressed in bits. An N-bit resolution implies that 2^N digital words are mapped to the same number of distinct analog levels (or vice versa). Figure 4.1 shows transfer characteristics and converter errors at the example of a 3-bit DAC. The ideal transfer characteristic of data converters is a straight line representing a linear gain. The accuracy of data converters is the difference between expected (ideal) and actual transfer response. The unit of accuracy is also given in bits, with the full scale input as reference. Factors limiting the accuracy are offset, gain and linearity errors.

An offset error is defined as the actual output value that is present at inputs that are expected to produce a zero output. Offsets, given in units of least significant bits (LSBs), result in constant, i.e. DC shifts of the transfer curve and usually refer to analog signals. A gain error is the difference between predicted and real output value at full scale inputs, after offsets are removed. It can also be thought of as a difference in slope to the ideal line. Illustrations of gain and offset error are given in figure 4.1a. The ideal deviation between any two consecutive levels is one LSB. The differential nonlinearity (DNL) expresses errors between any two consecutive symbols and describes the largest difference from 1 LSB. For instance, a DNL error of ±0.2 LSB results in actual output steps of 0.8 or 1.2 LSB. Since digital levels always change with multiples

of LSBs, DNL errors refer only to the analog parameters. A second linearity error is the integral nonlinearity (INL). It describes the maximum deviation from a straight line passing through the end points of the actual input/output characteristics. Both, DNL and INL are defined after offsets and gain errors have been removed. They are illustrated in figure 4.1b. Nonlinearities cause corruptions of the desired signal by inducing harmonics and intermodulation products and by gain reductions. This can severely impact the performance of data converters and the entire communication system.

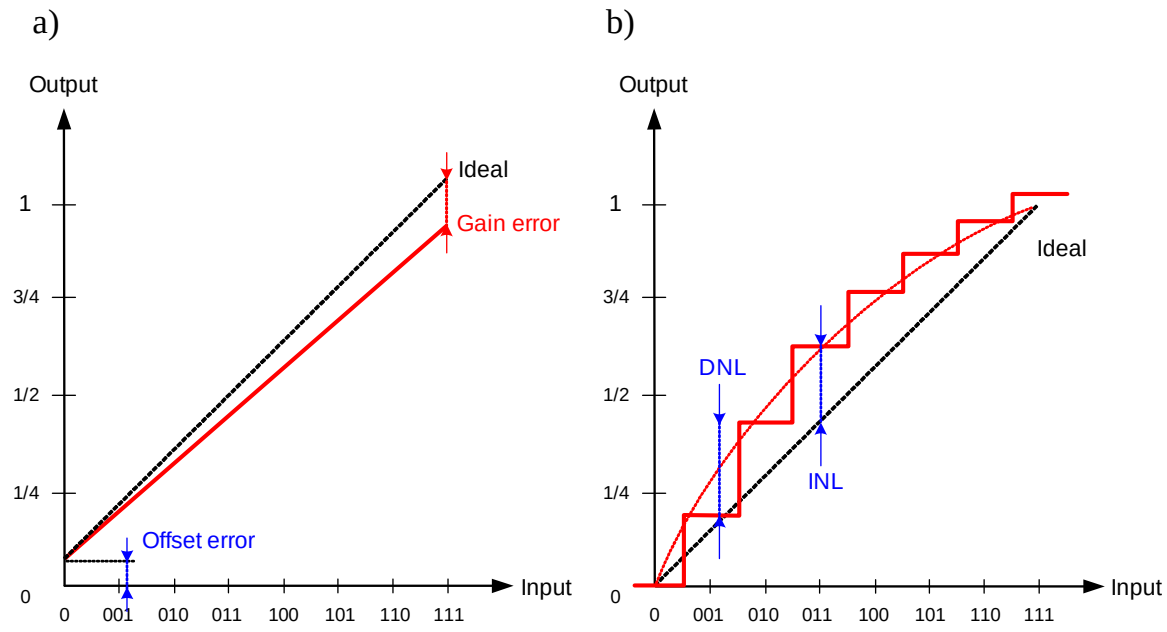


Figure 4.1: Data transfer characteristic and definitions of converter errors for a 3-bit example. (a) offset and gain error, (b) differential (DNL) and integral (INL) nonlinearity errors.

Further important performance parameters of data converters are sampling rate, i.e. the maximum rate at which data can be converted continuously, and the dynamic range, DR. The dynamic range here denotes the ratio of maximum input signal amplitude to the input level at which the converter exhibits a signal-to-noise ratio of one. The low end of the DR is usually limited by the noise performance, whereas the upper end is restrained by nonlinearities.

In the process of analog-to-digital conversion, quantization noise is added. With the assumption that no quantizer overload occurs and that the quantization error signal is a random variable uniformly distributed between the $\pm\Delta/2$, the signal-to-noise ratio (SNR) is given by

$$\mathrm{SNR} \approx 6.02 \cdot N + 1.76\mathrm{dB} \qquad (4.1)$$

Here, N is the number of bits and Δ is the quantization level $\Delta = V_{peak\text{-}to\text{-}peak} / 2^N$, i.e. 1 LSB. Hence, the number of quantization levels determines the power of quantization noise that is present in the data conversion system. Each additional bit reduces the quantization noise power by about 6 dB. Further details on data converter background and quantization noise can be found for instance in [Razav1995], [Johns1997], and [Razav1998].

4.2 Dual-Standard ADC

Modern communication devices are required to support more than one mobile application. This section describes an analog-to-digital converter capable to operate in both GSM (Global System for Mobile communication) and DECT (Digital Enhanced Cordless Telecommunication) standard. A mobile terminal supporting both applications enables wireless access in high concentrations of locally confined mobile users (DECT) as well as continuous mobile connection while travelling fast and over large distances (GSM). This contributes to improved access capabilities and user comfort as well as to reduced terminal costs.

The suitability of sigma-delta data converters for multi-standard applications derives from their ability to employ the same architecture for different combinations of input signal bandwidth and sampling speed. Their potential for high resolution, obtained from oversampling and noise shaping, makes these converters an attractive choice for input signals of narrow bandwidth. In addition, requirements for analog prefiltering are relaxed and the processing power of advanced digital signal processors (DSPs) can be used for post-processing steps.

A complete sigma-delta converter comprises a modulator and a decimation filter. The modulator oversamples the input signal and moves its quantization noise to higher frequencies. The decimation filter removes the high frequency components and thereby most of the quantization noise. It also reduces the sample rate. This chapter focuses on the design of the modulator part of the ADC. The decimation filter was not part of the implementation and is only briefly touched upon later.

4.2.1 ADC Performance Specifications

The requirements of the analog-to-digital converter derive from the specifications and test requirements provided by the communication standards and the choice of radio front-end. A suggested design for the receiver for GSM and DECT is the wideband-IF architecture presented in section 1.4. This architecture combines a high degree of integration with multi-standard capabilities due to channel select filtering at baseband.

The sensitivity, S, of a receiver is defined as the minimum signal level that can be detected in the presence of a strong in-band signal while maintaining an acceptable signal-to-noise ratio. It can be expressed as [Razav1998]:

$$S = 10\log(kT) + 10(\log BW) + 10\log(F) + SNR_{min} \tag{4.2}$$

where k is the Boltzman constant ($1.384 \cdot 10^{-23}$ J/K), T is the temperature in Kelvin, BW is the bandwidth of the system, and F is the noise factor of the system, defined as

$$F = \frac{SNR_{in}}{SNR_{out}} \tag{4.3}$$

The term $10 \cdot \log(F)$ is also called the noise figure, NF, and expresses the noise contribution in dB. At room temperature (T = 300 K), $10 \cdot \log(kT)$ equates to -174 dBm and presents a typical resolution limit for measurement equipment. SNR_{min} in equation (4.2) is the minimum signal-to-noise ratio required by the baseband processor to correctly demodulate the received symbols. SNR_{min} was estimated to 6 dB.

Due to finite matching and insertion loss, the processing in the receiver chain imposes sensitivity degradation of the received signal. Each receiver stage contributes to this degradation. When the noise figure (NF_m) and gain (A_{pm}) of each stage are known, the overall noise figure of an m-stage receiver can be estimated using Friis equation [Friis1944]:

$$NF_{total} = 1 + (NF_1 - 1) + \frac{NF_1 - 1}{A_{p1}} + \frac{NF_2 - 1}{A_{p2}} + \ldots + \frac{NF_m - 1}{A_{pm}} \tag{4.4}$$

Equation (4.4) shows that the noise contribution of each stage is reduced by the gain of the preceding stage. This indicates that the noise contribution in the first stages is most critical. If a stage exhibits a power loss, the noise is effectively amplified.

Using the specifications given in [ETSI1996a], [ETSI1996b], as well as the receiver block specifications for a wideband-IF receiver architecture presented in [Rudel2000],

the signal-to-noise requirements are found to be 80-100 dB and 60-80 dB for GSM and DECT mode, respectively. The necessary converter resolution for GSM is hence about 13 to 16 bit, whereas in DECT mode, only 10 to 13 bits are needed. After down-conversion to baseband and channel select filtering in previous receiver stages, the ADC needs to process two signals of bandwidths 100 kHz for GSM and 700 kHz for the DECT mode. Table 5 summarizes the specifications for both operating modes.

Table 5: Specifications for GSM and DECT receiver [ETSI1996a], [ETSI1996b]

Parameter	GSM	DECT
RF Band	1710-1785 MHz 1805-1880 MHz	1880-1930 MHz
Signal Band	100 kHz	700 kHz
Sensitivity (BER = 10^{-3})	-100 dBm	-83 dBm
Largest Blocker	-26 dBm	-33 dBm
Input Noise	-120 dBm	-112 dBm
Carrier to Noise Ratio	9 dB	10.3 dB
Needed SNR_{ADC}	80-100 dB (13-16 bit)	60-80 dB (10-13 bit)

4.2.2 Converter Architecture

The ADC is part of the back-end in a receiver chain, converting the analog baseband signal to the digital realm. The peak signal-to-quantization noise ratio (SQNR) of a sigma-delta modulator can be estimated as [Rabii1999]

$$SQNR_{peak} = \frac{3}{2}\frac{(2L+1)}{\pi^{2L}}(OSR)^{2L+1}(2^B-1)^2 \qquad (4.5)$$

where B is the quantizer‘s resolution in bits, L is the modulator order and OSR is the oversampling ratio. From equation (4.5) it can be concluded that modulators of low order imply low circuit complexity but require a high sampling frequency to obtain the same SQNR. On the contrary, higher modulator orders effectively increase SQNR by improved noise shaping and demand lower sampling rates. They are therefore suitable for wideband applications. But as presented in [Riebn1991], they also imply problems with loop stability and increase circuit complexity. Several studies on modulator archi-

tectures have been reported, e.g. [Karem1989], [Karem1994], [Medei1998], [Gothe2003]. Based on equation (4.5), the oversampling ratios (and hence the sampling frequencies) that are needed to achieve the required ADC resolution are determined for both modes.

Table 6: Frequency requirements for different modulator orders in GSM and DECT mode.

Resolution		GSM (100 kHz)			DECT (700 kHz)		
		L = 2	L = 4	L = 6	L = 2	L = 4	L = 6
62 dB (10 bit)	OSR	32	16	8	32	16	8
	f_s	6.4 MHz	3.2 MHz	1.6 MHz	44.8 MHz	22.4 MHz	11.2 MHz
74 dB (12 bit)	OSR	64	16	8	64	16	16
	f_s	12.8 MHz	3.2 MHz	1.6 MHz	89.6 MHz	22.4 MHz	22.4 MHz
86 dB (14 bit)	OSR	128	32	16	128	32	16
	f_s	25.6 MHz	6.4 MHz	3.2 MHz	179.2 MHz	44.8 MHz	22.4 MHz
98 dB (16 bit)	OSR	256	32	16	N.a.	N.a.	N.a.
	f_s	51.2 MHz	6.4 MHz	3.2 MHz	N.a.	N.a.	N.a.

Besides operation in two different communication applications, implementation costs need to be minimized. A leading design guideline for the converter was therefore the ability to re-use as much of the architecture as possible for both standards to obtain a hardware efficient realization. Operation in GSM or DECT mode is accomplished by modification of parameters like oversampling ratio, feedback gain and quantizer resolution.

Table 7: Operating Mode Summary

Mode	Signal Bandwidth	Sampling Frequency	OSR	Quantization in 2^{nd} loop
GSM	100 kHz	13 MHz	64	1 bit
DECT	700 kHz	26 MHz	16	3 bit

The architecture of choice was a fourth-order, double loop 2-2 MASH architecture as reported in [Karem1989] and [Baher1992]. This structure exhibits stability behaviour like a second order modulator. Based on the frequency requirements listed in Table 6, the sampling rates were chosen to be 13 MHz for GSM and 26 MHz for the DECT mode. Table 6 would suggest a DECT sampling rate of 44.8 MHz. But this high

rate would also cause an increased power consumption and involve a more elaborated clock generation circuitry. To compensate for the lower sampling frequency, a 3-bit quantizer in the second modulator loop is used for the DECT mode. The parameters for both modes of operation are summarized in Table 7.

Figure 4.2 depicts a block diagram of the implemented architecture. The modulator consists of two loops, each comprising a second order modulator. The digital output of the first loop is fed into an error cancellation logic. It is also converted back to the analog domain with a 1-bit digital-to-analog converter. This 1-bit DAC is basically a switch and not shown in figure 4.2. The weighted input of the quantizer then subtracted from its output to obtain the quantization noise. This quantization noise is further processed in the second modulator loop. The quantization noise contributions from both loops are subtracted in the digital error correction logic to obtain fourth order noise shaping.

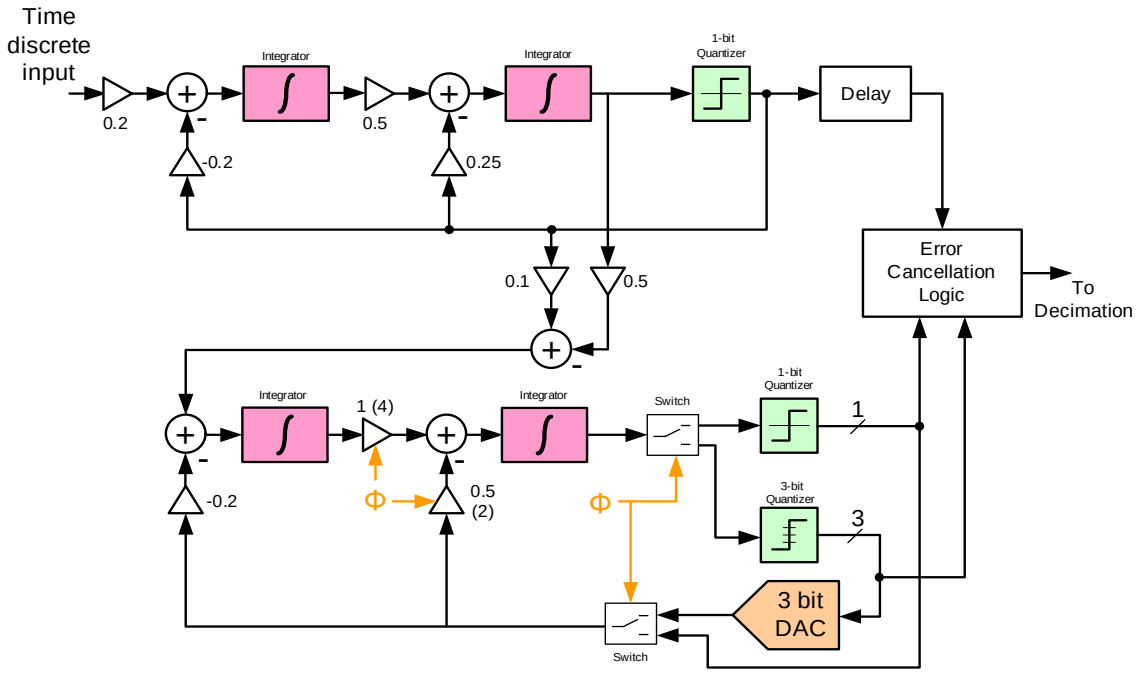


Figure 4.2: Sigma-delta modulator architecture: Fourth-order, 2-2 MASH architecture for GSM and DECT mode

The integrator stages employ fully-differential, switched capacitor operational transconductance amplifiers (OTAs). The input to the first integrator also serves as a sampling instance of the modulator. In order to the limit kT/C noise contribution, a sampling capacitor of 2 pF is used. This in turn requires a larger driving capabilities in

the OTA. In DECT mode, the fourth integrator needs to drive a 3-bit quantizer which constitutes a large capacitive load. It therefore also requires a larger slew rate. A 2-stage OTA implementation is therefore chosen for the first and fourth integrator. The integrators in the second and third stage exhibit relaxed slew rate requirements. They are implemented using folded cascode OTAs.

All modulator blocks are dimensioned for operation at 26 MHz. During operation in GSM mode, the clock frequency is reduced to 13 MHz. An externally supplied mode selection signal, Φ, selects a 1-bit quantizer (GSM) or a 3-bit quantizer (DECT) in the second loop. Φ also adjusts the gain parameters prior the fourth integrator to accommodate the different driving capabilities in the feedback. With signal Φ adjusting the modulator to the different requirements of the two modes, a large extent of hardware sharing is achieved.

4.2.3 Decimation filter

In the previous section, the modulator part of the sigma-delta ADC was described. After modulation, noise from the quantization process is still present in the modulator output signal. It is only shifted to higher frequencies. A combination of digital filters is used to remove high frequency components. Furthermore, the number of samples to be processed in the DSP is reduced using a decimation filter. Decimation by a factor of M is the reduction by simply taking every M^{th} sample and discarding the rest. (The actual word originates from punishing an army, i.e. the beheading of every 10^{th} soldier, during the times of the Roman Empire.) The signal needs to be low-pass filtered prior to decimation to avoid aliasing due to emergence of images.

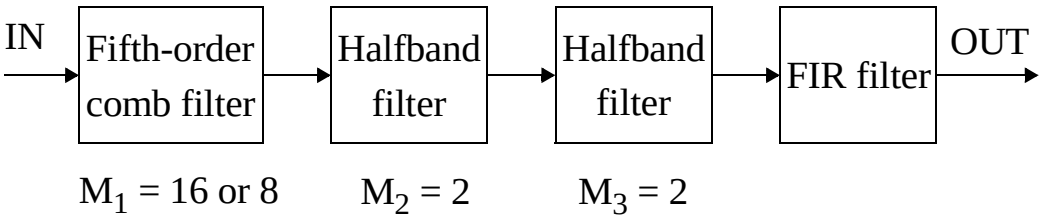


Figure 4.3: Multi-stage, linear phase decimation filter with programmable decimation rate M_1

The decimation filter was not part of the implementation, nor has the author of this thesis a contribution in this field. The filter structure is merely mentioned here for completeness of the overall ADC.

Whereas sampling rate and resolution of the overall sigma-delta converter are determined by the analog modulator, power consumption of the whole ADC is governed by the digital filters. It is possible to removed the quantization noise and undesired adjacent channels in one single filter stage followed by an decimator. This requires many filter taps and results in high power consumption. By using a multi-stage approach instead, the complexity of the decimation filter is reduced and the subsequent filter stages operate at a lower sampling rate.

Cascaded-Integrator-Comb (CIC) filters [Hogen1981] are an efficient implementation of the first filter stage. To meet the requirements of both ADC modes, a low power, fifth-order CIC filter stage with programmable decimation stage was designed [Gao2000]. Here, M = 16 for GSM and M = 8 for DECT mode.

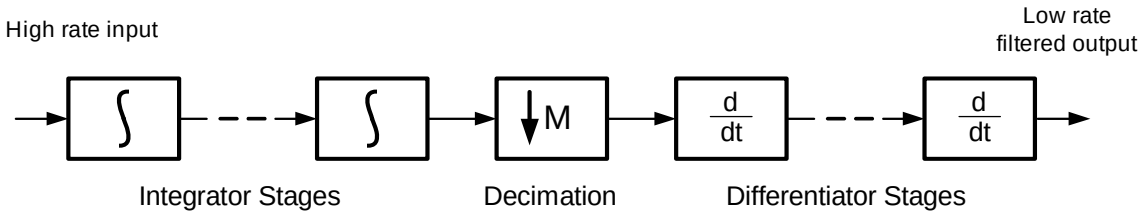


Figure 4.4: Architecture of a Cascaded-Integrated-Comb filter as presented in [Hogen1981] with decimation after integration stages

4.3 Simulations Results

The signal-to-noise pulse distortion ratio (SNDR) was determined by sweeping the input signal amplitude from V_{in} = 10 µV to V_{in} = 1 mV. Figure 4.5 presents the SNDR for both modes, resulting in a peak SNDR of 97 dB for GSM and 82 dB for the DECT mode when circuit nonidealities were included.

Figure 4.6 presents a layout view of the fourth order 2-2 MASH sigma-delta modulator. The regions of the modulator blocks are highlighted. The circuits were laid out using common analog layout techniques to address performance reduction arising from matching problems (due to temperature or manufacture drifts) and noise. These techniques included the composition of larger devices out of several small devices, maintaining constant perimeter-to-area ratios of components, the implementation of dummy units, and a common-centroid layout. Unoccupied die area was filled with metal to provide on-chip bypass capacitance for the power supply network. Furthermore, guard

rings were used to protect sensitive active devices. Despite these techniques for careful layout, the chip returned not functioning. Hence, only simulation results, as summarized in Table 8, are given.

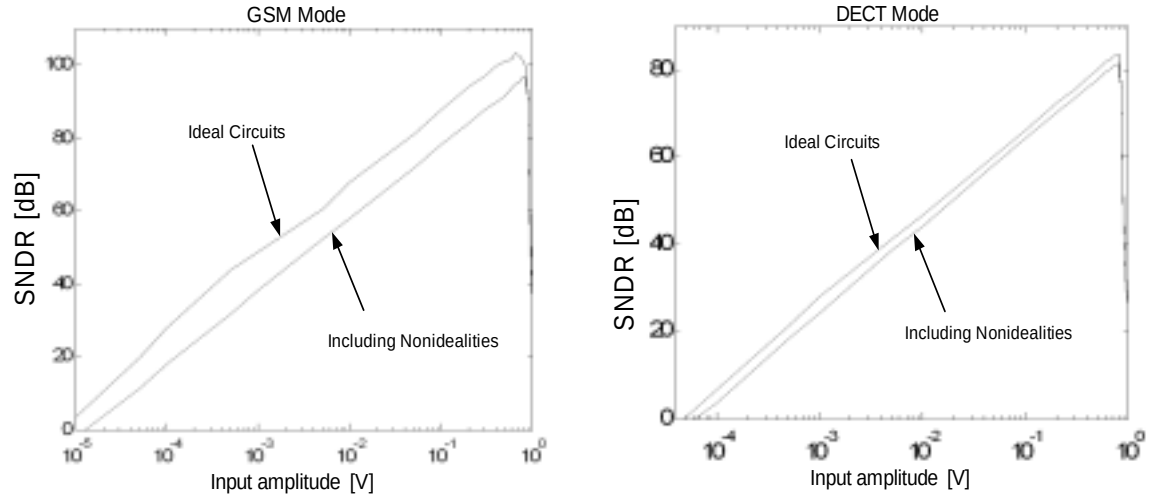


Figure 4.5: SNDR versus input amplitude for GSM and DECT mode.

The area of the core is $1.3 \cdot 0.7$ mm^2, whereas the total area of the chip (including pads) is about $2 \cdot 2$mm^2. The chip was designed in a 0.35 µm, double poly, 3 Volt CMOS process. The power consumption of the core area was determined to be 13 mW and 19 mW for GSM and DECT mode, respectively.

Table 8: Simulation Results for Dual-Mode ΣΔ-ADC

Mode	SNDR	Quantizer	Power
GSM	97 dB (16 bit)	1-bit/1-bit	13 mW
DECT	82 dB (13 bit)	1-bit/3-bit	19 mW

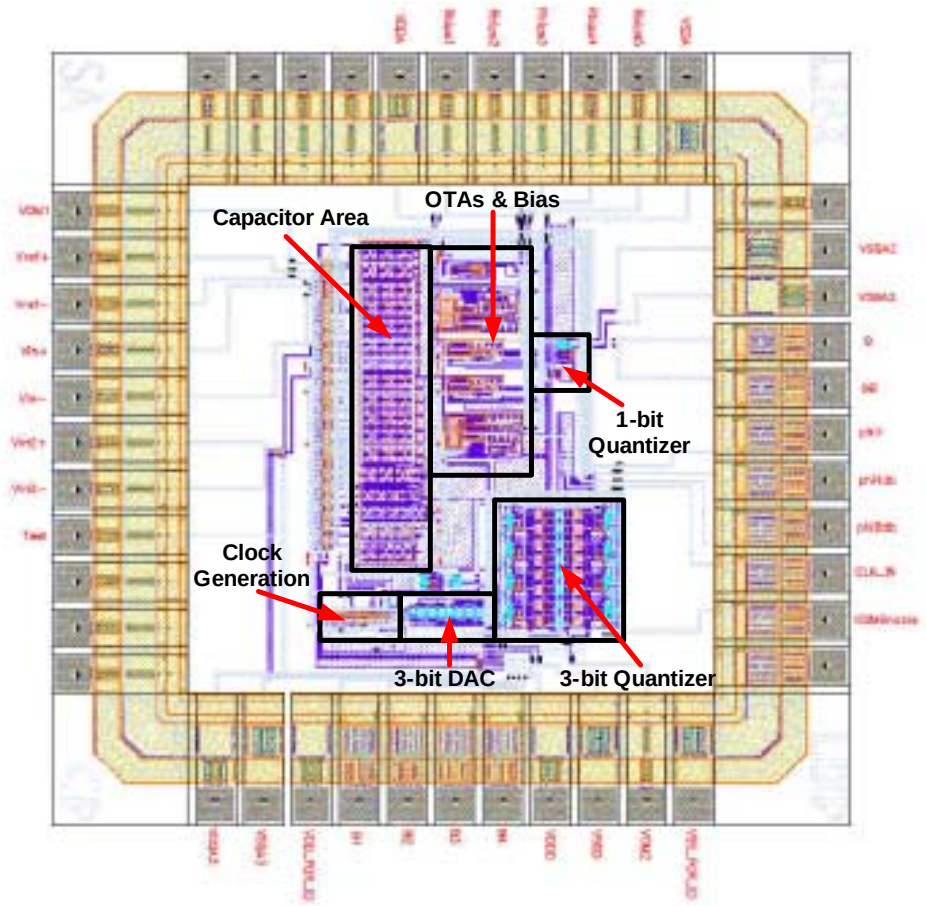


Figure 4.6: Layout view of fourth order sigma-delta modulator.

5. Summary and Conclusion

Frequency synthesizers form essential parts of any modern wireless radio communication device. Being a small part of a whole transceiver chain, they generate the local oscillator signal needed for both transmission and receiving of communication data.

This thesis presents a synthesizer architecture based on a frequency-locked loop for wireless radio communications. In particular, it targets multi-standard applications with operation in several different frequency bands. Its main objectives are two-fold: Firstly, the synthesizer is to provide flexibility in loop parameters such that employment in several standards becomes feasible. This is achieved by decoupling reference input signal and oscillator output. Instead, the output frequency is controlled by a digitally given reference word. Settling time and output frequency accuracy are regulated with a variable reference signal. Secondly, implementation costs are to be reduced for operation in a multi-standard environment. This is accomplished by reusing most of the synthesizer hardware.

The frequency-locked loop, its building blocks and performance were described and analysed. A digital scheme is employed for detecting differences between target and actual output frequency. A target frequency is represented by a digital number, whereas the actual frequency in the feedback path is determined from the number of periods within a given time frame. Operation in a different application is accomplished by adjusting the digital reference word, whereas the feedback division factor remains constant. This results in a flexible detector output range and is the key to multi-standard operation. The digital information representing frequency differences is subsequently converted into an analog voltage. This is carried out by means of a digital sigma-delta modulator and a 1-bit digital-to-analog converter, both clocked by the synthesizers own feedback signal. The combination of modulator and 1-bit DAC produces inherently linear D/A conversion at little hardware expense. Using different VCOs and adjusting conversion gain values, the same loop architecture can be employed for a multitude of frequency bands. Since much of data processing is done in the digital domain, the settling time performance will benefit from future technology scaling.

The presented synthesizer generates frequencies in different bands, but in the presented form, it does not lock its phase to the reference and is hence suitable for non-coherent communications schemes. Also, phase noise performance is yet inferior compared to phase-locked loops dedicated to one standard. In order to achieve phase lock and comparable phase noise performance, an additional locking circuit, e.g. a delay-

locked loop, needs to be applied. This will also enable operation in coherent communications. This locking scheme, however, does not anymore require frequency tuning capabilities. It is hence available at less implementation costs.

The synthesizer parameters like settling time, output frequency accuracy and oscillation bandwidth can be traded-off for each other, allowing for flexible application of the presented architecture. A three dimensional space formed by these parameters was derived. It was shown that the new synthesizer architecture is relevant for all applications that fall within this parameter space. Simulation results were given for the example of operation in the licence free ISM band (2400 - 2483.5 MHz).

It can be concluded that, compared to traditional phase-locked or delay-locked loops, this architectures is a suitable alternative for frequency synthesis in a multi-standard environment. The author suggests its use when several frequency bands are to be incorporated in a multi-standard application. The proposed architecture is also suitable as a tuning circuit for band acquisition at power start up.

As with many designs, this synthesizer leaves opportunities open for further improvement and continued research. Most importantly, an integrated circuit implementation of the complete architecture has yet to be demonstrated. Furthermore, the detection principle could be extended to include phase lock to an external signal in future versions of this synthesizer.

A fourth order sigma-delta modulator for a dual-standard analog-to-digital converter was also presented in this thesis. Being the back-end in a radio receiver, an ADC converts the symbols that are detected by the analog front-end into the digital realm. Demodulation and reconstruction of the original user data are implemented with the use of digital signal processors.

Using sigma-delta modulation provided necessary converter resolution. But it also enabled application versatility. Adjusting sampling frequency and quantizer resolution, the modulator allows a large degree of hardware sharing while meeting the specifications of both, GSM and DECT standard. Compared to an implementation using two individual converters, required power and die area are significantly reduced. The modulator circuit was designed in a 0.35 μm CMOS process using a 3 Volt supply.

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