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SDR Implementation of Convolutional Encoder and Viterbi Decoder

Dr. Rajesh Khanna[1], Abhishek Aggarwal[2]

Professor, Dept. of ECED, Thapar Institute of Engineering & Technology, Patiala, Punjab, India[1]

PG Student [VLSI], ECED, Thapar Institute of Engineering & Technology, Patiala, Punjab, India[2]

ABSTRACT: This paper represents the SDR implementation of convolutional encoder and Viterbi decoder. In this paper there are two parts where one part is based on the VHDL simulation of encoder and decoder and second part is based on hardware, in which all these simulations are implemented on SDR (an FPGA). This paper has taken random bits as input bits to the transmitter. Convolutional encoder of ½ has been used in this paper. This paper uses the AWGN channel for analysis and different roll-off factors for RRC filter are also used.

The motive of the paper is to analyze the bit error rate for different roll-off factors and to analyze the VHDL simulation with real time implementation on SDR.

KEYWORDS:QPSK, RRC, convolutional codes, viterbi decoder, AWGN, SDR.

I.INTRODUCTION

Communication is the process of conveying messages at a distance or simply a process of exchanging information. But this communication can't be error free as long as noise channel exists. Somehow this error can be decreased at the user end by increasing energy per bit but this decreases bit rate. Energy per bit cannot be increased after a certain limit. Error free communication can be done by using another way also. This way includes the addition of redundant bits. This is also known as error-correcting codes (ECC). These redundant bits are systematically generated and the sender adds these bits to its messages[1]. This allows the receiver to detect and correct a limited number of errors occurring anywhere in the message without the need to ask the sender for additional data. Although these extra bits reduce the bit rate of the transmission and its power but the advantage is that error of probability is reduced.

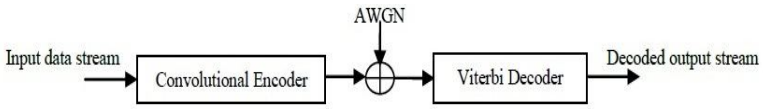

Figure 1: Block Diagram of Encoder and Decoder

II. REVIEW OF PREVIOUS ARCHITECTURES

SDR implementation is usually a real time application in wireless communication. In wireless communication, AWGN (Additive White Gaussian Noise) channel introduces most of the noise in real data.

S.NO	ARCHITECTURE	RESULT
1.	Convolutional Encoder and Viterbi Decoder in DSP platform[6]	Flexible platform but slow in speed.
2.	Convolutional Encoder and Viterbi Decoder in microcontroller platform[7]	Slow speed.
3.	FPGA based Convolutional Encoder and Viterbi Decoder. [8]	Complexity of Viterbi decoding algorithm increases.

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There are the various architectures which have already been used to implement the convolutional encoder and Viterbi decoder. The last architecture used was FPGA based. In this case, a highly complex Viterbi Decoder loses its advantages when going to decode the transmitted bit on low-noise channel [1]. The last architecture used was FPGA based. In this case, a highly complex Viterbi Decoder loses its advantages when going to decode the transmitted bit on low-noise channel.

1. Transmitter

(A) LFSR

A linear-feedback shift register is used to generate random output bits. LFSR is mostly driven by XOR.

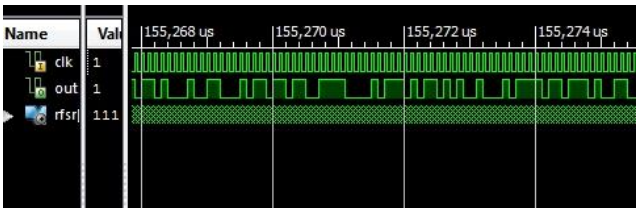

Figure 2: Implementation of LFSR to get random sequence

(B) Convolutional Encoder

Convolutional codes are used to check and correct the errors. It can take a single bit or multiple bits as an input which gives matrix of encoded outputs. Bit sequence can be altered in Digital modulation communication systems because of noise and other external factors. To minimize the noise factor, certain additional bits are added to the encoded output which makes the bit error checking more successful and it will also yields more accurate results. This transmission of more number of bits than the original one is used to get the original signal even in the vicinity of noise. Convolution codes are considered to be best codes for controlling error and gives better performance.

If 'k' are the number of input bits to be encoded, 'n' are the number of output bits encoded and 'm' are the number of shift registers used then (n, k, m) is used for expressing convolutional codes.

Mostly, the value of n and k is smaller and k is less than n, but the number of shift registers takes larger value.

Figure 3indicates the block diagram of convolutional encoder. The (2, 1, 8) convolutional encoder consists of seven shift registers and two exclusive-or gates. In the starting all the shift registers are rest for initialization. They are programmed in such a way that all seven shift registers are connected in series to do shifting and updating operation on every clock pulse. Two exclusive-or gates are used to obtain the encoded output. After every clock pulse a matrix of encoded output is obtained which consists of two bits according to generator polynomials are obtained [2]. The encoded bits are not only dependent on the current input bit but also influenced by the inputs bits given to the first shift register seven clock pulses before.

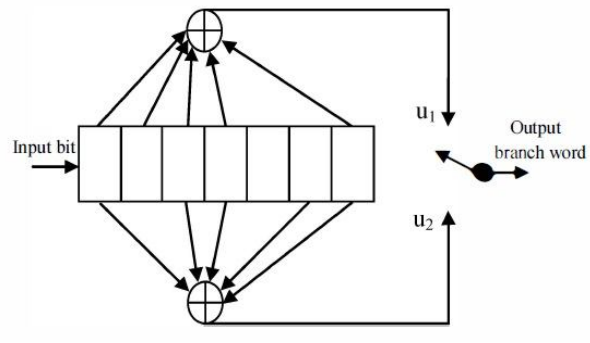

Figure 3: Convolutional Encoder

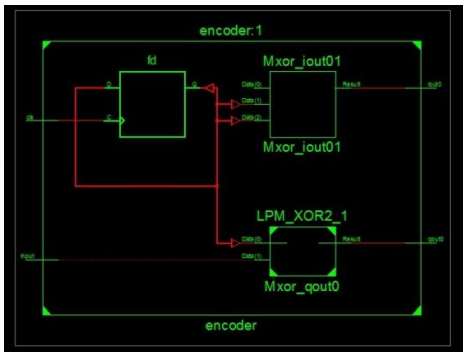

Figure 4: Proposed Encoder

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(C) QPSK Modulation

QPSK modulation has been used in this paper so that the effect of transmitted bits can be analyzed efficiently over the AWGN noise channel. QPSK modulation requires normalization and raised root cosine filter. RRC filter has been designed using MATLAB FDA tool and converted into HDL.

(D) AWGN Channel

In wireless communication, AWGN (Additive White Gaussian Noise) channel introduces most of the noise in real data. It is actually a mathematical model that represents physical phenomena in which the impairment is the linear addition of white noise with a constant spectral density [3].

To simulate AWGN channel in VHDL, two random functions have been generated which gives two variables. Then by using Box-Muller method, the noise signal is calculated.

$$X = \sqrt[2]{-2\ln(rand_1)}\cdot\cos(2\pi\ rand_2)$$

The implementation is done under 3 steps:-

- Generation of two random variables.
- Use given equation (Box-Muller method) to generate noise.
- Adjustment of AWGN that depends on SNR and input signal.

Figure 5: Example of an AWGN channel

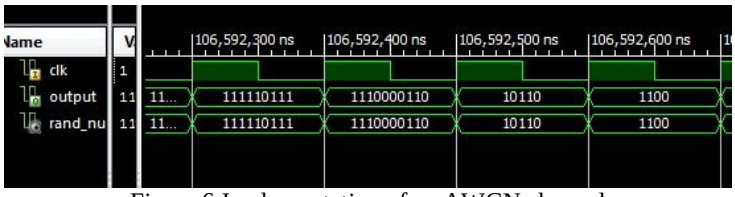

Figure 6:Implementation of an AWGN channel

2. RECEIVER

(A) VITERBI DECODER

The encoded input bits are convolutional encoded. These encoded bits are then passed through QPSK modulation. The modulated information bits is then has to be received at the receiver end. During this the noise is added by AWGN channel. At the receiver end Viterbi decoder is used to decode the bits and get the input bits. in the decoder process, there are various steps involved. Quantization, synchronization, branch metric computation, state metric update, survivor path recoding, output decision generation are the various blocks involved in this Viterbi Decoder. Add control and select (ACS) is the block which receives two branch metrics and the state metrics. The state metric of the state is updated with the selected value and the survivor path information is recoded in the survivor path storage module. [5]

3. SOFTWARE DEFINED RADIO(SDR)

SDR represents a design paradigm for radios where large portion of functionality is implemented through FPGA device. Through this radio will be having the ability to alter its operating parameters to analyze new features and capabilities. An SDR approach reduces the RF and emphasizes Digital Signal Processing to enhance overall flexibility. SDR is having various advantages like ease of manufacture, ease of design, using advanced signal processing technique, multimode operation, and flexibility to use additional functionality etc.

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III. RESULTS AND DISCUSSION

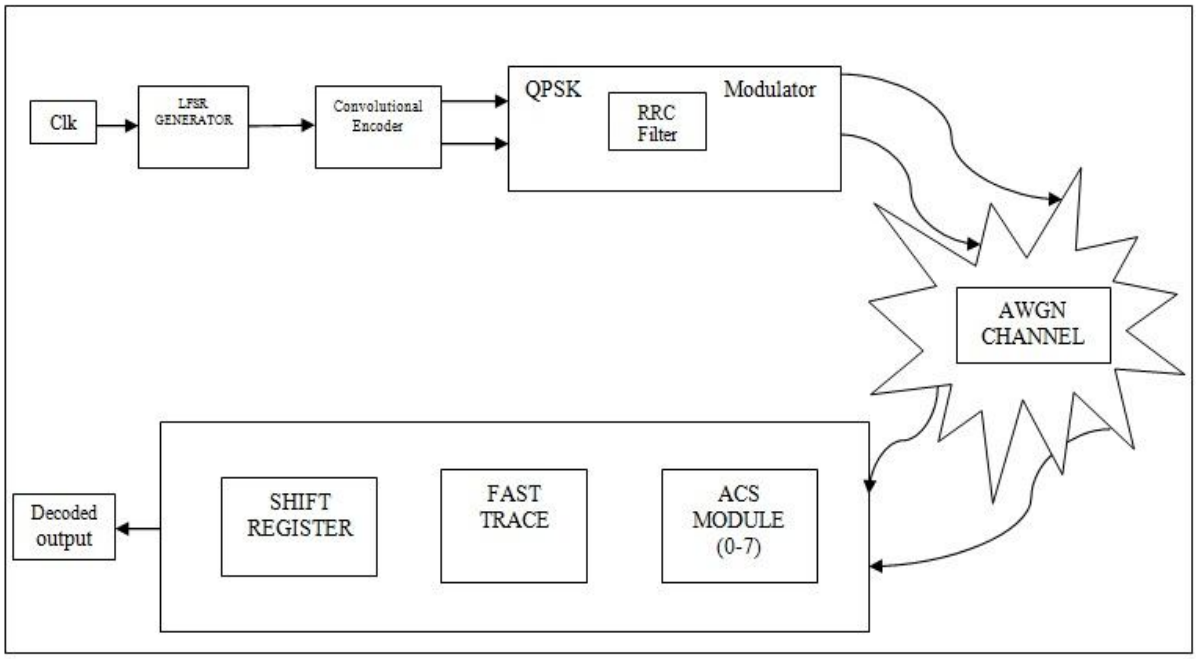

Figure 7: Proposed Encoder and Decoder

This paper implements proposed encoder and decoder shown in figure 7.

The simulation has been done in following steps:-

1. The random sequence was generated using LFSR register.
2. This random sequence was given input to the convolutional encoder.
3. The output of the encoder was fed to the QPSK modulator which consists of RRC filter.
4. For 0, 1, 1.5, 2 roll factors RRC filter was generated. The encoded output was fed to this filter.

```
Device utilization summary:
---------------------------

Selected Device : 3s500epq208-5

 Number of Slices:                      489  out of   4656    10%
 Number of Slice Flip Flops:            395  out of   9312     4%
 Number of 4 input LUTs:                685  out of   9312     7%
    Number used as logic:               677
    Number used as Shift registers:       8
 Number of IOs:                           4
 Number of bonded IOBs:                   4  out of    158     2%
 Number of GCLKs:                         1  out of     24     4%
```

Figure 8: Device Utilization Summary

5. The filtered output was fed to the AWGN channel block which results in the addition of transmitted signal with AWGN channel.
6. The noisy transmitted bits were fed to the Viterbi decoder blocks.
7. The bits are passed with ACS module, survivor path and trace path module and results in the decoded output.

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8. Input to the encoder and output from the decoder and clock pulse is checked on the result screen.

Figure 8 shows the device utilization summary of the proposed encoder and decoder.
Less than 10% of the total device available has been used by this proposed encoder and decoder.

The HDL implementation uses the multipliers, adders, subtracters, 1, 6, 8, 16, 18, 32 bit registers, comparators and xor gates. This paper makes the efficient use of all the resources.

```
=========================================================================
Final Register Report

Macro Statistics
# Registers                                          : 388
 Flip-Flops                                          : 388
# Shift Registers                                    : 7
 2-bit shift register                                : 4
 29-bit shift register                               : 1
 6-bit shift register                                : 1
 7-bit shift register                                : 1

=========================================================================
```

Figure 10: Final Synthesis Report

Final HDL synthesis report results in the use of overall 388 registers and 7 shift registers. This paper uses the minimum number of resources for the implementation of encoder and decoder.

BIT ERROR RATE SIMULATION

BER is calculated by using the various roll off factors for RRC filter.

(i) When $\alpha = 0$

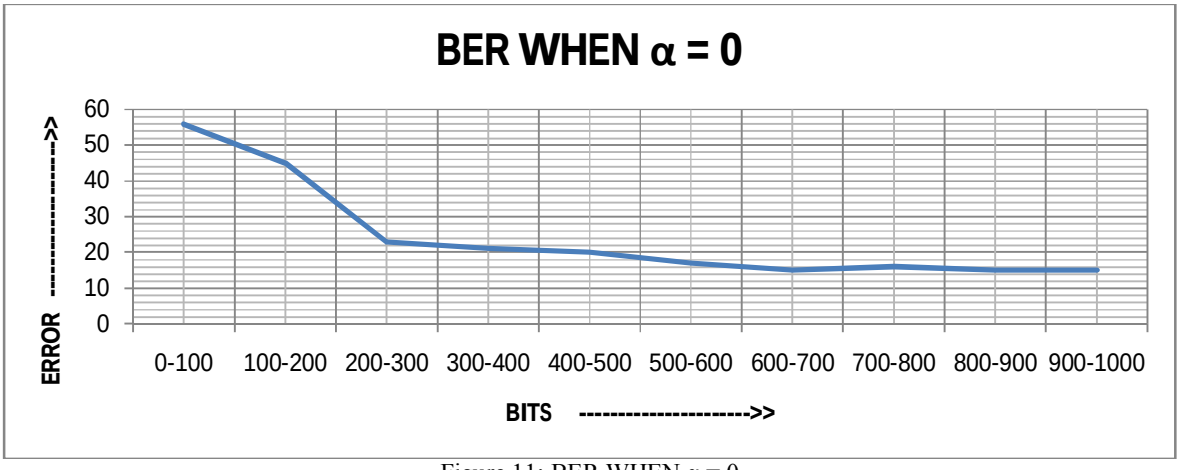

Figure 11: BER WHEN $\alpha = 0$

This simulated graph represents that error is maximum when the bits transmitted is less. As the rate of transmitting the bits increases the error decreases. At around 1000 bits error reduces to around 17 in 900-1000 bits.

(ii) When $\alpha = 1$

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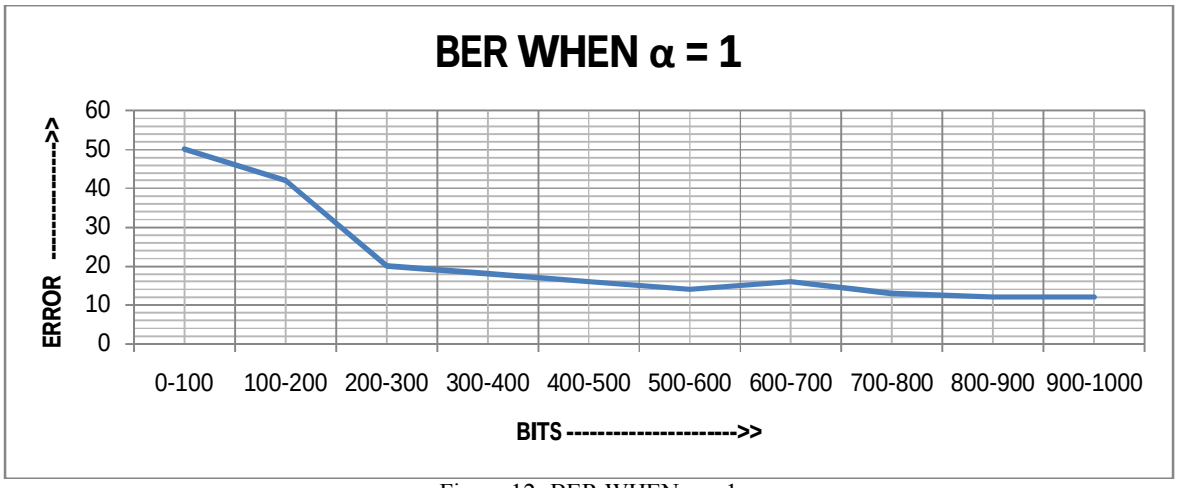

Figure 12: BER WHEN α = 1

This simulated graph represents that error is maximum when the bits transmitted is less. As the rate of transmitting the bits increases, the error decreases. At around 1000 bits error reduces to around 12 in the interval of 900-1000 bits. This also shows that as the roll off factor of RRC filter increases then ERROR PER 100 BITS decreases. If the roll-off factor is more increased then what happens. It is shown in next figure.

(iii) When α = 2

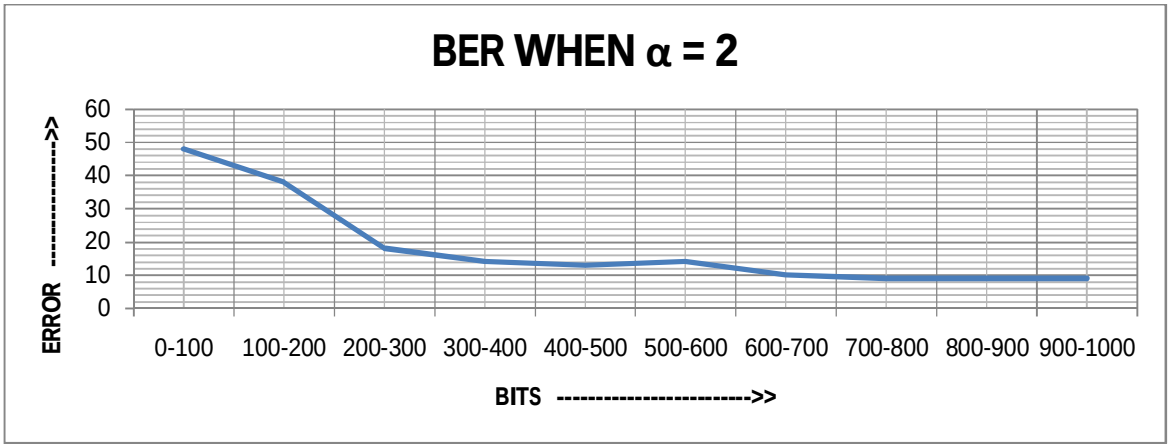

Figure 13: BER WHEN α = 2

This simulated graph represents that error is maximum when the bits transmitted is less. As the rate of transmitting the bits increases, the error decreases. At around 1000 bits error reduces to around 10 in 900-1000 bits. So minimum error is seen when roll-off factor is 2.

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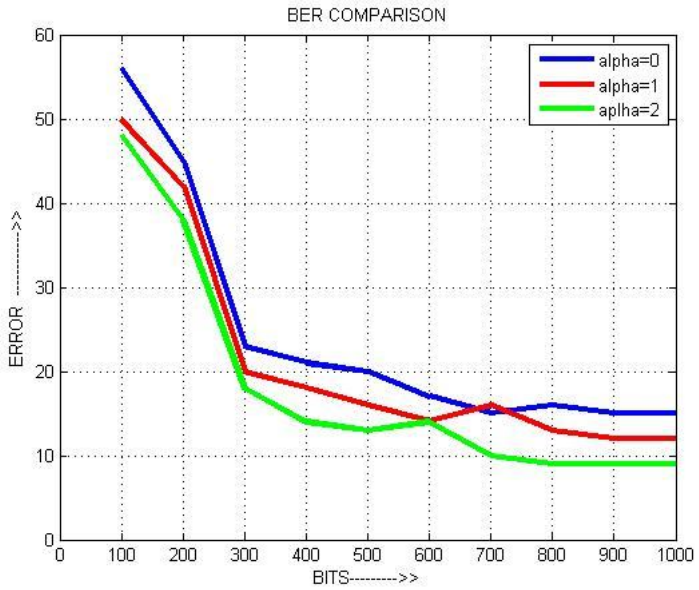

The comparison plot clearly shows that as the roll off factor increases, the BER decreases.

SDR IMPLEMENTATION:-

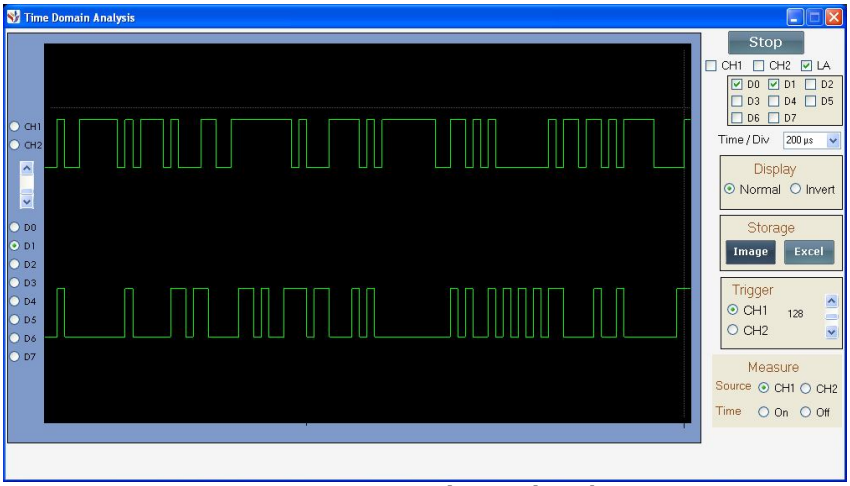

Figure 14: SDR implemented graph

The HDL code is run over FPGA. Figure 14 shows the result after running code over SDR. This shows first stream as random input stream. And next to be the output stream.

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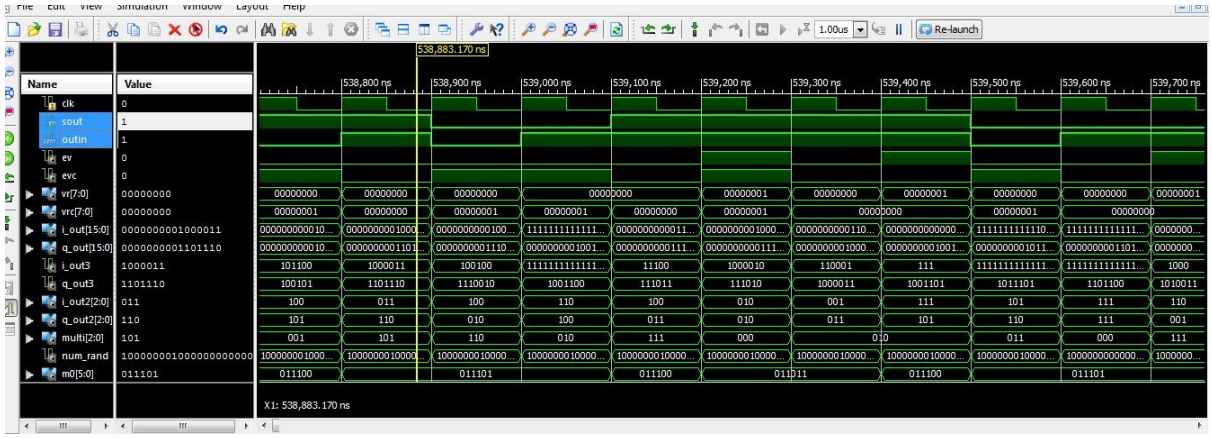

Figure 15: Final Output

IV. CONCLUSION

This paper has described the SDR implementation of Convolutional Encoder and Viterbi Decoder over AWGN channel. Using QPSK modulation RRC filters got used and depending upon the various roll-off factors BER over every 100 bits got analyzed. The timing summary after analysis got is minimum period is 27.362ns (i.e. maximum frequency is 36.547 MHz). Maximum input arrival time before clock is 4.213ns and maximum output required time after clock is 4.182ns.

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