An Analysis of Time Interleaved-ADC through Literature Review

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Abstract- In this research survey work we have presented the performance analysis of TI-ADC in order to enhance the performance it is very important to prepare a survey so we have done through a literature survey. In many mix-signal systems, analog-to-digital converters (ADCs) play an important role for digitizing analog signal. To design high-speed and high-resolution ADCs, multichannel ADC structure is adopted in numerous applications. And time-interleaved ADCs (TI-ADCs) are the most frequently used multi-channel ADC structure, as the sampling rate of TI-ADCs can be boosted multiple times. Time-interleaving can also achieve better power consumption for GHz ADCs compared to traditional ADC architectures. On the other hand, due to the process, voltage and temperature variations, the ADC channels are not identical and the performance of the TIADC is limited by the offset, gain and timing mismatches among the ADC channel. The analog-to-digital converters (ADCs) and calibration scheme for timing skew in time-interleaved analog-to-digital converters. It detects the relevant timing error by subtracting the output difference with the sum of the first derivative of the digital output. The least-mean-square (LMS) loop is exploited to compensate the timing skew. Since the calibration scheme depends on the digital output, all timing skew sources can be calibrated and the main ADC is maintained.

Keywords:- Time-interleaved ADCs (TI-ADCs).

I. INTRODUCTION

An analog-to-digital converter (ADC, A/D, or A to D) is a device that converts a continuous physical quantity (usually voltage) to a digital number that represents the quantity's amplitude. The conversion involves quantization of the input, so it necessarily introduces a small amount of error. Instead of doing a single conversion, an ADC often performs the conversions ("samples" the input) periodically. The result is a sequence of digital values that have been converted from a continuous-time and continuous-amplitude analog signal to a discrete-time and discrete-amplitude digital signal.

An ADC is defined by its bandwidth (the range of frequencies it can measure) and its signal to noise ratio (how accurately it can measure a signal relative to the noise it introduces). The actual bandwidth of an ADC is characterized primarily by its sampling rate and to a lesser extent by how it handles errors such as aliasing.

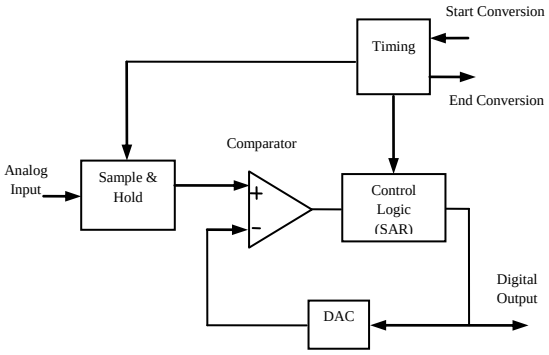

Fig.1 Block Diagram of Analog to Digital Converter

The dynamic range of an ADC is influenced by many factors, including the resolution (the number of output levels it can quantize a signal to), linearity and accuracy (the quantization levels match the true analog signal) and jitter (small timing errors that introduce additional noise). The dynamic range of an ADC is often summarized in terms of its effective number of bits (ENOB), the number of bits of each measure it returns that are on average not noise.

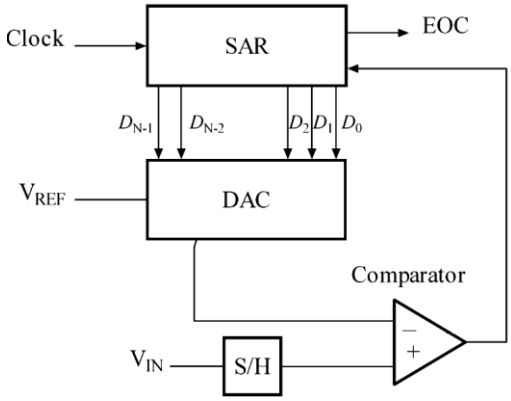

Fig .2 Diagram of Successive Approximation Register with Digital-to-Analog converter

An ideal ADC has an ENOB equal to its resolution. ADCs are chosen to match the bandwidth and required signal to noise ratio of the signal to be quantized. If an ADC operates at a sampling rate greater than twice the bandwidth of the signal, then perfect reconstruction is possible given an ideal ADC and neglecting quantization error. The presence of quantization error limits the dynamic range of even an ideal

ADC, however, if the dynamic range of the ADC exceeds that of the input signal, its effects may be neglected resulting in an essentially perfect digital representation of the input signal.

Analog-to-digital conversion consists of two operations.

1. *Sampling*
   (Discretizing in time)
2. *Quantization*
   (Discretizing in amplitude)

Types of ADCs

1. *SAR*
2. *Sigma-delta*
3. *Algorithmic*
4. *Single-slope*
5. *Time-to-digital*

Time-domain analysis

Sub-ADC output is (ignoring quantization)

$$\boldsymbol{y_i\,[n]\ =\ x\,((nN\ +\ i)T_s\,)} \qquad (1)$$

where Ts is sampling period, N is interleaving factor, and $\boldsymbol{i\ =\ 0,\ldots,N\ -1}$

Time-domain analysis

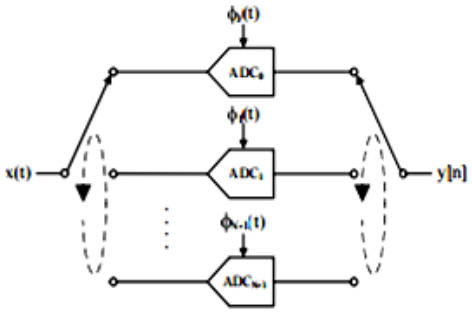

Fig. 3.Time-domain analysis for ADC

Output multiplexer combines these streams such that

$$\boldsymbol{y[n]\ =\ y_i\,n\ -\ i\,N\ \ where\ i\ =\ n\ mod\ N} \quad (2)$$

II. FREQUENCY-DOMAIN ANALYSIS

This is less intuitive that can take the discrete-time Fourier transform (DTFT) of the (upsampled) sub-ADC outputs and the time-interleaved ADC output. A time-interleaved ADC (TIADC) consists of M channel ADCs, which have the same sampling rate but different sampling phases, as a single converter operating at an M times higher sampling rate. Time skew calibration method for time-interleaved ADCs is presented. By comparing the mean value of the multiplication of signals in two adjacent channels, the time skew can be estimated. Subsequently, a capacitor array based digitally controlled delay block placed in sampling clock path is adopted to compensate the time skew.

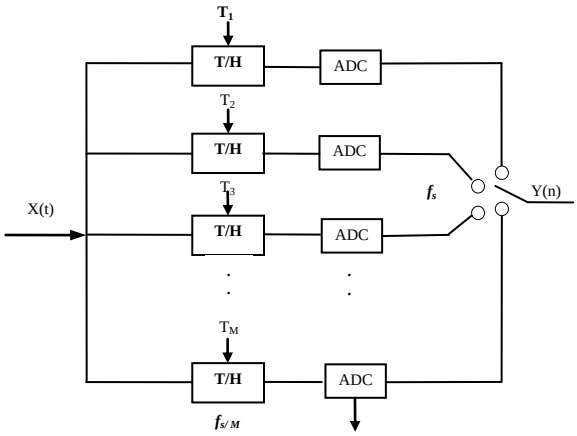

Fig. 4. The structure of time-interleaved ADCs

III. LITERATURE SURVEY

Qiu Lei Yuanjin Zheng ; Di Zhu ; Siek, L.[1] researcheda statistic based time skew calibration method for t ime-interleaved ADCs. By comparing the mean value of the multiplication of signals in two adjacent channels, the time skew can be estimated. Subsequently, a capacitor array based digitally controlled delay block placed in sampling clock path is adopted to compensate the time skew. In addition, the precision of calibration is further improved through using a monotonic small capacitor array. In a 4-channel 1GS/s 12-bit TI-ADC system, the spurious free dynamic range (SFDR) can be improved to 77.5dB with 0.25ps LSB in the digitally controlled delay block.

Slim, H.H. ; Inst. for High Freq. Eng., Tech. Univ. Munchen, Munich, Germany ; Russer, P. [2] presented the sampling rate of state of the art analog to digital converters (ADCs) limits the base-band frequency range of real-time time domain electromagnetic interference (TD-EMI) measurement systems to 1 GHz. In this paper, a time interleaved sampling architecture is introduced to overcome this limitation and to extend the baseband of the time-domain EMI receiver. Using three parallel time-interleaved ADC converters a TD-EMI measurement system with 3 GHz base bandwidth has been realized. The misalignment effects are studied and an automatic calibration routine is introduced. The 40 dB spurious free dynamic range required by the CISPR standards is achieved.

Wen-Jun Shi [3] described that time-interleaved analog-to-digital converters (TIADC) is effective on increasing the system sampling rate. But the gain, offset and time mismatches among the sub-ADCs introduce undesirable noise into the system and degrade the overall performance seriously. This research work describes a post calibration method with digital filter banks to remove the gain and time mismatch errors. These digital filters, whose coefficients are according to authors ighted least square (WLS) criteria, are carried out with poly-phase structure. Simulation results show that this method can significantly improve the spurious

free dynamic range (SFDR) and signal to noise ratio (SNR) of TIADC system.

Chung-Yi Wang [4] investigated a timing-skew calibration technique which equalizes the phase spacing's among multiphase clocks. The scheme uses simple sample-and-hold circuits controlled by the multiphase clocks to sample a common reference input. Phase spacing is measured by counting the number of zero crossings between two adjacent sampling sequences. A zero-crossing detection scheme is proposed. It has better immunity against the offsets of the comparators used in the detector. A digital calibration processor is also proposed. It examines the outputs from the zero-crossing detectors, and then adjusts the delays of clock buffers in order to minimize timing skews. The proposed calibration scheme does not demand stringent requirement for the reference input. Its application to a eight-channel 6-b time-interleaved analog-to-digital converter is demonstrated.

L. Chi Ho, P. J. Hurst and S. H. Lewis [5] proposed an 11-bit 160-MS/s four-channel time-interleaved double-sampled pipelined ADC implemented in a 0.35-μm CMOS process is described. Digital calibration is used to correct mismatch errors between channels as authors ll as the memory errors that arise from the use of double sampling. The signal-to-noise-and-distortion ratio is improved from 45 to 62 dB after calibration with an 8.7-MHz input. The spurious-free dynamic range is increased from 47 dB to 79 dB.

Y. C. Lim, Y. X. Zou, J. W. Lee, S. C. Chan, [6] presented a multichannel filtering approach for TIADC mismatch compensation. Authors applied the generalized sampling theorem to directly estimate the ideal output of each sub-ADC using the outputs of all the sub-ADCs. If the WLS technique is used as the optimization tool, the dimension of the matrix to be inversed is N times N. For the same number of coefficients (and also the same spurious component performance given sufficient arithmetic precision), their technique is computationally less complex and more robust than the filter-bank approach. If mixed integer linear programming is used as the optimization tool to produce filters with coefficient values that are integer powers of two, their technique produces a saving in computing resources by a factor of approximately (100.2N(M- 1)/(M-1) in the TIADC filter design.

IV. PROBLEM DESCRIPTION

The problem with a statistic based calibration technique is analyzed. Compared with the previous published techniques, an effective time skew detection method, and with the digitally controlled delay block, the precision of the calibration can be further improved by decreasing the size of unit capacitor in the delay block. In addition, the calibration technique can be readily extended to TI-ADCs with more than four-channels. This study is to use digital and mixed signal processing methods to reduce mismatch errors. Since the intended time-interleaved ADC should have a very low power consumption, the signal processing methods should be as power efficient as possible. Another preferable property of the methods should be the ability to study in the background, i.e., without interrupting the normal conversion process.

V. PROPOSED METHDOLOGY

Analog-to-digital converters (ADCs) have been one of the key electronic components in electronic devices that require interaction with the real world since the early days of digital signal processing systems. The three main performance metrics used to evaluate and categorize the ADCs are their speed, resolution and power. The research in the ADC area has been driven by new applications that constantly demand higher speeds and resolutions. In one group of applications, with a steady increase in performance of digital circuits, there is a trend of performing more signals processing in the digital domain, and the ADCs are being moved closer to the chip input. This means that more information about the analog signal needs to be captured, which translates into more stringent speed and resolution requirements for ADCs.

In many mix-signal systems, analog-to-digital converters (ADCs) play an important role for digitizing analog signal. To design high-speed and high-resolution ADCs, multichannel ADC structure is adopted in numerous applications [1-3]. And time-interleaved ADCs (TI-ADCs) are the most frequently used multi-channel ADC structure, as the sampling rate of TI-ADCs can be boosted multiple times. Due to process variation, there are mismatches between the channels, such as offset mismatch, gain mismatch, time skew and bandwidth mismatch, which result in the performance degradation. Many approaches have been published to mitigate the mismatches in timed-interleaved ADCs [3-4][9-13]. In [4], a multi-channel filter was utilized to compensate time skew and bandwidth mismatch. However, no mismatch parameter estimation block is used and the filter coefficients are fixed. It therefore cannot be adjusted with environmental changing.

VI. CONCLUSION AND FUTURE SCOPE

The timing skew calibration scheme for TIADC has been analyzed. It detects the relevant timing error by the ratio of the output difference and the sum of the first derivative of the channel ADCs. Since the detection depends on the digital output, all timing skew sources can be calibrated and the main ADC is maintained. The calibration technique can be readily extended to TI-ADCs with more than four-channels. In the future TI-ADC plays an important role in technology as communication is growing day to day and also this field has become a basic necessity for every human being for any communication purpose.

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