Design of Low Power Two Stage CMOS Operational Amplifier

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Abstract: ***The trend towards low voltage low power silicon chip systems has been growing quickly due to the increasing demand of smaller size and longer battery life for portable applications in all marketing segments. The supply voltage is being scaled down to reduce overall power consumption of the system. The objective of this project is to implement the full custom design of low voltage and low power operational amplifier. In this paper a well defined method for the design of a two-stage CMOS operational amplifier is presented. The op-amp which has been designed, exhibits a unity gain frequency of 8MHz, a gain of 70dB with 75^0 phase margin and power consumption is 19.5µW. The simplest frequency compensation technique employs the Miller effect by connecting a compensation capacitor across the high-gain stage. Both the theoretical calculations and computer aided simulation analysis have been given in detail. Design has been carried out in Tanner tools. The simulation results in a tsmc 0.18um CMOS process from a 1.8V voltage supply demonstrate the designed has a gain 70dB.***

Keywords: 2 stage CMOS Operational amplifier, Stability, Frequency Compensation, Low power.

1. Introduction

Research in analog-circuit design is focused on low voltage, low-power battery operated equipment to be used in portable equipment, wireless communication products, hearing aids, and consumer electronics. A reduced supply voltage is necessary to decrease power consumption so this would reduce battery size and weight and enable longer battery life time. For the same reason, low-power circuits are also expected to reduce thermal dissipation, of increasing importance with the general trend in minimization.

Operational amplifiers are an integral part of many analog and mixed signal systems. In designing an op-amp, numerous electrical characteristics, e.g. gain bandwidth, slew rate, common mode range, output swing, offset, all have to be taken into consideration. Furthermore, since op-amps are designed to be operated with negative-feedback connection, frequency compensation is necessary for closed-loop stability. Power dissipation can be reduced by reducing either supply voltage or total current in the circuit or by reducing the both. As the input current is lowered though power dissipation is reduced, dynamic range is degraded. As the supply voltage decreases, it also becomes increasingly difficult to keep transistors in saturation with the voltage headroom available. Another concern that draws from supply voltage scaling is the threshold voltage of the transistor. A decrease in supply voltage without a similar decrease in threshold voltage leads to biasing issues. In order to achieve the required degree of stability, generally indicated by phase margin, other performance parameters are usually compromised. As a result, designing an op-amp that meets all specifications needs a good compensation strategy and design methodology.[1]

CMOS Op-amp can be used efficiently for practical consequences for example designing of a switched capacitor filter, analog to digital converter etc. In this case the designs of the individual op amps are combined with feedback and by various parameters that affect the amplifier such as input capacitance, output resistance, etc.[3]

Outline of paper

This paper is organized as follows. Section 2 presents the two stage amplifier. Section 3 reviews the 2 stage CMOS Op amp design with compensation capacitor. Its specifications are briefly clarified. Section 4 presents the simulation results of the proposed op-amp and finally in Section 5 give my concluding remarks.

2. The two stage CMOS op amp

Two-stage OP-AMP mainly consists of a cascade of Voltage to Current and Current to voltage stages. The first stage consists of a differential amplifier converting the differential input voltage to differential currents. These differential currents are applied to a current mirror load recovering the differential voltage. The second stage consists of common source MOSFET converting the second stage input voltage to current. This transistor is loaded by a current sink load, which converts the current to voltage at the output.

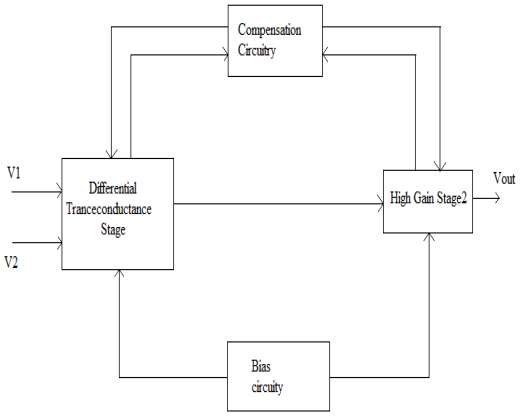


Figure 1: A general two stage CMOS Op-amp

Figure 1 shows the specific two-stage CMOS op-amp. The second stage is also nothing more than the current sink inverter.[15] The common source second stage increases the DC gain by an order of magnitude and maximizes the output signal swing for a given voltage supply. This is important in reducing the power consumption. If the Op-Amp must drive a low resistance load the second stage must be followed by a buffer stage whose objective is to lower the output resistance and maintain a large signal swing. Bias circuit is provided to establish the operating point for each transistor in its quiescent stage. Compensation is required to achieve stable closed loop performance.

Table1. Comparison of various op amps topologies

It can be seen from Table 1, the telescopic and two-stage topologies seem to be more suitable for the design. If pure telescopic, it will suffer from low output swing and medium gain despite meeting the specification. While as for the multi-stage topology, especially more than two stages, the stability will increase. In order to obtain a high enough gain, two fully differential auxiliary operational amplifiers act like a booster. Hence, we'll depict the two stage topology method for the amplifier design in this paper [15].

Referred paper work

PARAMETER	*[5] 2012*	*[6]*	*[7] 2010*	*[8] 2009*	*[9] 2005*
SUPPLY(V)	3.3	1	1.5	3.3	1.8
CMOS TECHNOLOGY	.35	.25	.18	.35	.18
GAIN(db)	80	-	92.5	65	60
UGB(MHz)	10	-	2.36	-	2.82
-3DB(Hz)		-	-	127	-
PHASE MARGIN(Degree)	49	-	81.3	-	63.5
POWER DISSIPATION(µW)	41.4	100	50	2000	37.8
ICMR(max) (V)	3				
ICMR(min) (V)	0.4				

3. Two stage CMOS Op amp design

The key criterion of this report is to operate with lower power supply and achieving less power consumption, low settling time, and reasonable gain. The operational amplifier drives the small capacitive loads also.

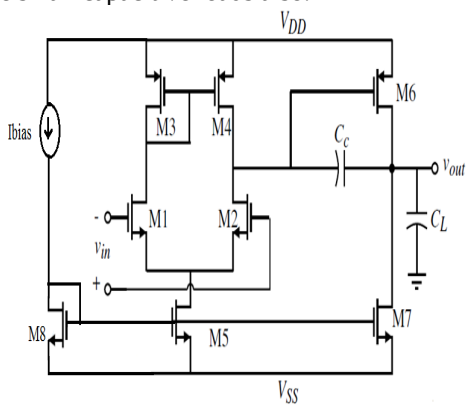


Figure2.Topology chosen for this paper

This circuit Consists of a cascode of Voltage to Current and Current to voltage stages. First stage consists of a differential amplifier of NMOS transistor (M1,M2) converting the differential input voltage to differential currents. Which are applied to a current mirror load of PMOS transistor(M3,M4) recovering the voltage. [15]

The second stage consists of common source MOSFET converting the second stage input voltage to current. This transistor is loaded by a current sink load, which converts the current to voltage at the output. C_L is the load capacitor and C_c is the compensation capacitor required for stability.

Specification Names	*Values*
Supply VDD	1.8V
VSS	-1.8V
Gain	>65db
Gain Band Width	10MHz
Slew Rate	50V/µs
Input Common Mode Range	0.4-3V
CL	1PF

Table 2: Custom Design Specifications of the amplifier

4. Simulation and Results

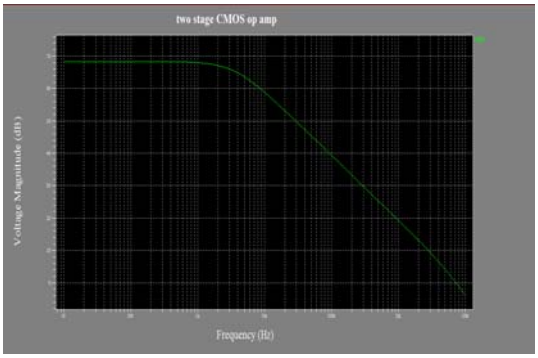
The CMOS operational amplifier is simulated on T-spice software for 0.18µm Technology for obtaining different parameter such as UGB (Unit gain bandwidth), gain, phase margin etc. These parameters are shown below.

Specification	*Results*
Technology	0.18µm
UGB	8MHz
C_L	1pf
Supply Voltage	±1.8V
Gain	70db
Phase Margin	75º
Power cons.	19.5µW

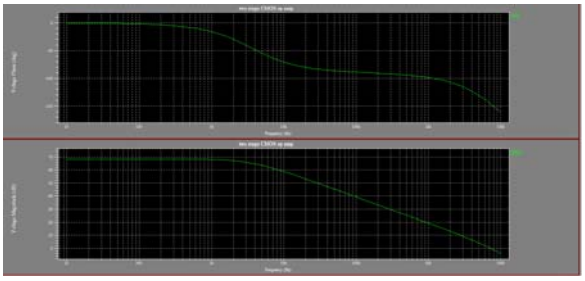
Simulated results waveforms

4.1 Gain Measurement

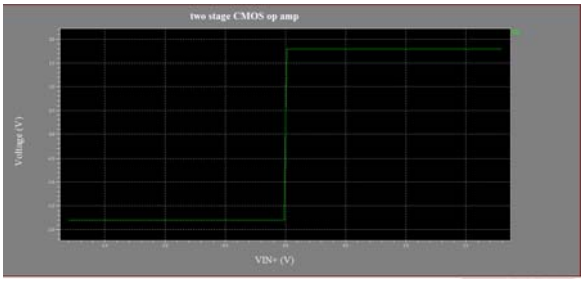
The gain obtained for this CMOS Operational Amplifier is about 70db.



4.2 Phase margin



4.3 Output Swing



5 . Conclusion

We have proposed a 2 stage CMOS op-amp and analyzed its behavior. Simulation results confirm that the proposed design procedure can be utilized to design op-amps that meet all the required specifications. The simulation is done with Tspice software. The design is on 0.18µm technology. The unit gain bandwidth achieved for the design is 8MHz, the gain is 70db and phase margin is of 75degree to ensure a good stability. The total power consumed is 19.5µW.

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