CHIP SET FOR REAL-TIME VIDEO SIGNAL PROCESSING

Nobuyuki YAGI, Ryoichi YAJIMA, Kazumasa ENAMI
NHK (Japan Broadcasting Corporation)
Science and Technical Research Laboratories
1-10-11,Kinuta,Setagaya-ku,Tokyo 157,Japan

Nobuyuki SASAKI, Kouji HOSHINO, Kazuhiro HARUKAWA
Toshiba Corporation
Komukai Works
1,Komukaitoshiba-cho,Saiwai-ku,Kawasaki 210,Japan

Shigemi MIKAMI
NHK (Japan Broadcasting Corporation)
Engineering Administration Department
2-2-1,Jinnan,Shibuya-ku,Tokyo 150,Japan

Hideki YAMADA
Toshiba Corporation
Semiconductor Division
580-1,Horikawa-cho,Saiwai-ku,Kawasaki 210,Japan

ABSTRACT

Two LSIs for real-time video signal processing have been developed; One a video-signal processing LSI (called the **Picot**) which can process dynamic images (time-varying images) at video rate (14.3MHz); and the other a network LSI (called the **Picot-net**) which connects a number of Picots and makes possible multi-processing. The **Picot** and the **Picot-net** have an architecture suitable for image signal processing. They are convenient for multi-processor systems, and efficient processing can be achieved in proportion to the number of Picots.

These LSIs make possible image-signal processing, including convolution, gray level transformation, geometrical transformation, noise reduction, edge detection, and histogramming. They can thus be applied to medical imaging, robot vision, video CODEC, broadcasting, and a variety of other fields.

I. INTRODUCTION

In broadcasting, video signal processing is conventionally done by using dedicated hardware such as video switchers and special effects equipments. But it is now desirable to achieve new video effects in a short period. This requires universal systems[1]. For this purpose, the authors developed an experimental real-time video signal processing system (called the RTVP)[2]. The RTVP is a multi-processor system which processes monochrome dynamic images at a 7.16MHz sampling frequency. On the basis of results obtained with this experimental system, the authors have developed two LSIs, the **Picot** and the **Picot-net**, which process color dynamic images in real-time at a clock rate of up to 14.3MHz.

For robot vision, picture transmission, etc., real-time processing of dynamic images is required. To meet this demand, LSIs like the ISP-II[3], RISP-II[4], VSP[5], etc. have been developed. The **Picot** and **Picot-net** can, of course, be used in these applications.

The **Picot** does all computations in parallel and pipeline fashion at a speed of 14.3 MHz, employing multiple internal buses and a sophisticated control system. The **Picot-net** works as a crossbar network to build up multi-processors, which allows arbitrary inter-connection, including broadcasting and gathering. Each LSI has 30K gates on chips 14.95 x 14.95 mm in area, made with a 1.5um double-layer metal CMOS gate array, and is mounted on a 223 pin-grid-array(PGA). The power consumption of each chip is about 1.0 W with a single 5V power-supply. Packages are shown in Fig.1.

This paper describes the architecture and application of the **Picot** and the **Picot-net**.

II. CONCEPT

To develop the chips, the authors set up the following design targets.

(1) A wide range of application. They can be applied to image signal processing for broadcasting, industrial, and medical purposes, etc.

(2) Microprogrammable. They have sequencer so that all functions can be controlled by programs.

(3) Video rate processing. A sampling frequency of 13.5MHz(CCIR digital TV standard[6]) or 14.3MHz(4fsc) is used for NTSC signal in the studio system.

(4) Real-time processing. Even if conditional branching occurs, these chips can process continuously.

(5) Efficient parallel processing. Except for simple processing, it's almost impossible for a single processor to do real-time processing. In order to make it easier to do multi-processing, functions to achieve synchronism between processors should be added. To make full use of the processors, arbitrary connections between them should be configured.

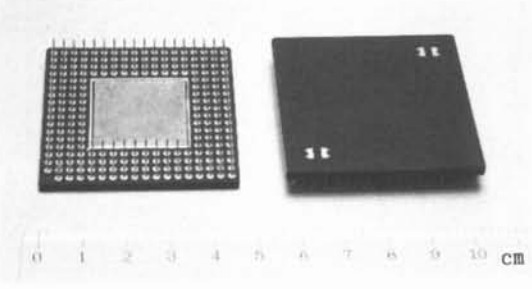


Fig.1 The **Picot** and the **Picot-net**

III. ARCHITECTURE OF THE Picot

A. Block diagram

Fig.2 is a block diagram of the **Picot** which includes a 16bit ALU (arithmetic logic unit), a 16b x 16b multiplier, a 22b HAU (horizontal addressing unit), a 22b VAU (vertical addressing unit). These can be connected by multiple buses without any limitation, and can do highly parallel processing. The use of the buses permits various paths, such as pipeline operation from the ALU to the multiplier, and parallel operation of the HAU and VAU. These operations are controlled by a microprogrammable sequencer suited to video signal processing. Programs are stored in an external program memory (4Kw x 32b). Besides program memory, data memory up to 16Mw (4096 x 4096 pixels) can be connected.

B. Input/Output

The **Picot** has two input-ports and a output-port for video signals. One of the inputs has a variable delay function of maximum 7 pixels. To achieve larger delays, a built-in line memory controller can be used. This outputs read/write clocks and reset pulses to drive line memories available on the market, and permits delays of up to 1024 pixels. These input-ports with variable delays are convenient for interpixel, interline, and intra-image processing. The word length of the input/output is 17bits which are added with a sync bit to 16b data. This allows the synchronous use of more than one **Picot**.

C. Arithmetic Circuits

The ALU has absolute value, maximum value and minimum value calculation functions, which are indispensable for video signal processing, as well as ordinary ALU functions. The ALU executes in 16bit (2's complement), and clips data automatically by hardware when an overflow or underflow occurs. This mechanism prevents black-to-white inversion which is conspicuous.

The multiplier carries out multiplications in 16bit x 16bit, and provides a 16-bit output. By the adoption of the 2nd-order Booth algorithm, the operation can be completed within a single clock cycle.

D. Addressing Circuits and Data Memory

The **Picot** can have a data memory besides a program memory of up to 16Mw (1w=16bits). This makes it possible not only to address standard TV but also HDTV, remote sensing images , etc. Addressing is carried out by the HAU and VAU. The HAU and VAU have identical circuit configurations, consisting of a full adder and

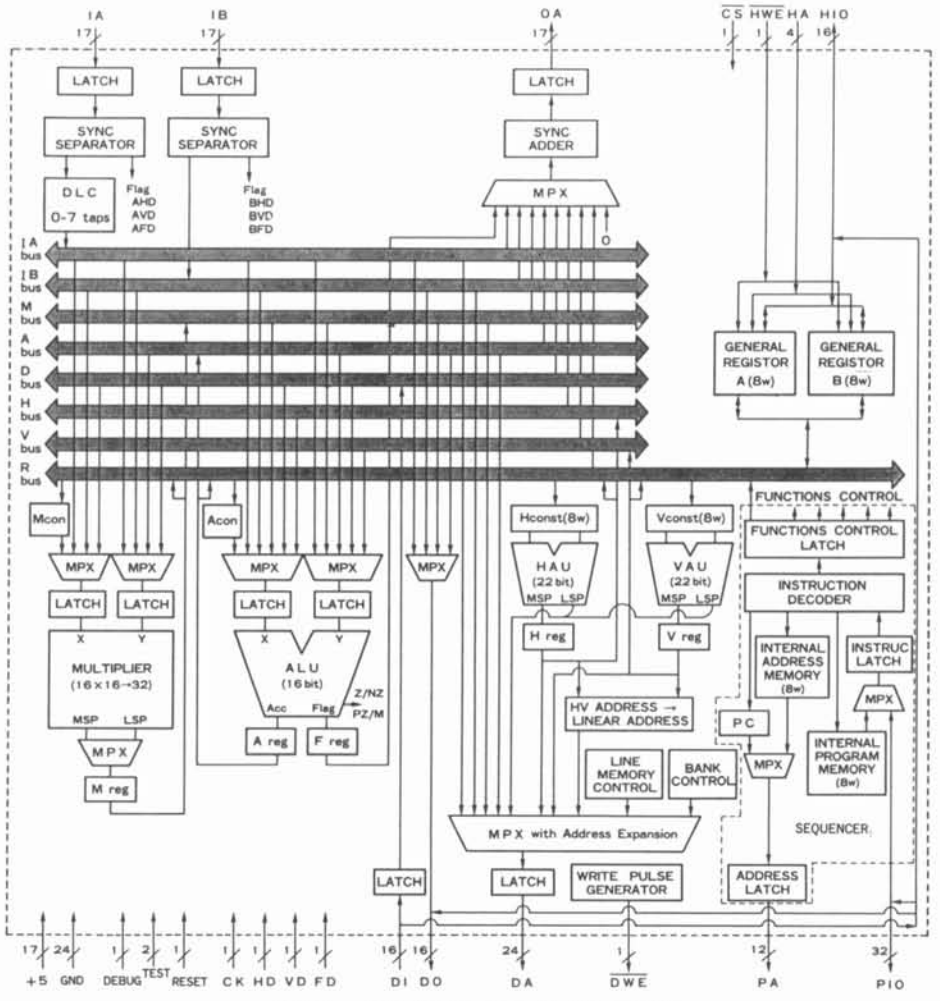


Fig.2 Block diagram of the **Picot**

two comparators. In accordance with comparisons, the results of the arithmetic operation can be replaced with replacement-value-registers. For clipping, maximum and minimum values should be set. This makes it easy to clip data when the data range goes out of the active zone in geometric transformations or graphic generations. Arithmetic operations are carried out in 22bit (integral part 16bits and decimal part 6bits, 2's complement). This makes it possible to keep adequate precision and dynamic range, even in geometric transformation. The data memory can be accessed by the HAU and the VAU at a rate of 14.3MHz. Moreover, the data memory can also be used as a 256 look-up tables (16b input/16b output) , which can be used for a nonlinear arithmetic function.

E. Control System

The **Picot** employs a sophisticated control system oriented to video signal processing. This control is executed by a microprogrammable sequencer.

In most video signal processing , the same operations are performed on all pixels within a frame (or in a line), and the sequencer has an appropriate control system.

The sequencer has a 'REPEAT' instruction, as well as 'CONTINUE' and 'JUMP' instructions, which the sequencer jumps its own address. The sequencer always checks two conditions, including the flags of arithmetic operations, sync signals, and branches three ways. This improves its real-time characteristics. To work at more than 14.3MHz, the sequencer has the structure of a three-stage pipeline (prefetch, decode, and execute). But unlike the ordinary pipeline system, the **Picot** has the ability to keep processing orderly, even when branching occurs. In most micro-processors and DSPs, operations can be executed only in a cycle in which instructions for the arithmetic units, such as the ALU and multiplier, exist. But the **Picot** executes pre-set arithmetic operations, even in cycles in which the instructions for the arithmetic units do not exist.

By these means, we could limit the microprogram width to 32 bits, otherwise more than 100bits would be necessary to control all the operational units in the **Picot** at any time. However we didn't lose real-time processing.

The **Picot** has an interface to receive a program, to receive and send data, and to receive control data from the host computer. The Picot has two sets of 8w general registers (1w=16bits). Communication between the **Picot** and the host computer can be done through them.

One of these sets faces the **Picot**, and the other the host computer at all times. The general registers on the Picot side can be used as a 'general' register, literally. The host computer gives the start address and parameters on the general registers on its own side. On condition that the **Picot** issues the 'RESTART' instruction and vertical blanking comes, register sets are switched over. The **Picot** loads the start address to the program counter of the sequencer, and executes from this value. If parameters are necessary, they are taken from the general registers. By making use of general registers, it is possible to return the data to the host computer. Moreover, the host computer can write and read the program memory and data memory when the **Picot** is reset. By combination with a universal micro-processor, various processing can be realized.

IV. ARCHITECTURE OF THE Picot-net

Fig.3 is a block diagram of the **Picot-net**, which consists of a crossbar network (32-input 48-output, 2b word length), a sequencer, and an interface for the host computer.

The network achieves arbitrary connection between inputs and outputs. It is possible to broadcast a single input to more than one output or concentrate more than one input to a single output. Thus both pipeline and array processing can be done at the same time. Switching between connections is done by fields (half frame in interlacing), as a rule, but it can also be done by pixels or lines.

The **Picot-net** is controlled by a microprogrammable sequencer. The control system is similar to the **Picot**. The control of the network needs a 240-bit micro-instruction width. But the connection between processors is usually set by fields or by lines. So it was decided to control in such a way that a single output is connected to a certain input by a single instruction. To set all connections, 48 instructions are necessary. However, once the setting has been done, the route remains fixed until switching is done by a new instruction. The micro-instruction is stored in a memory built in the LSI. There are two sets (64W x 16b

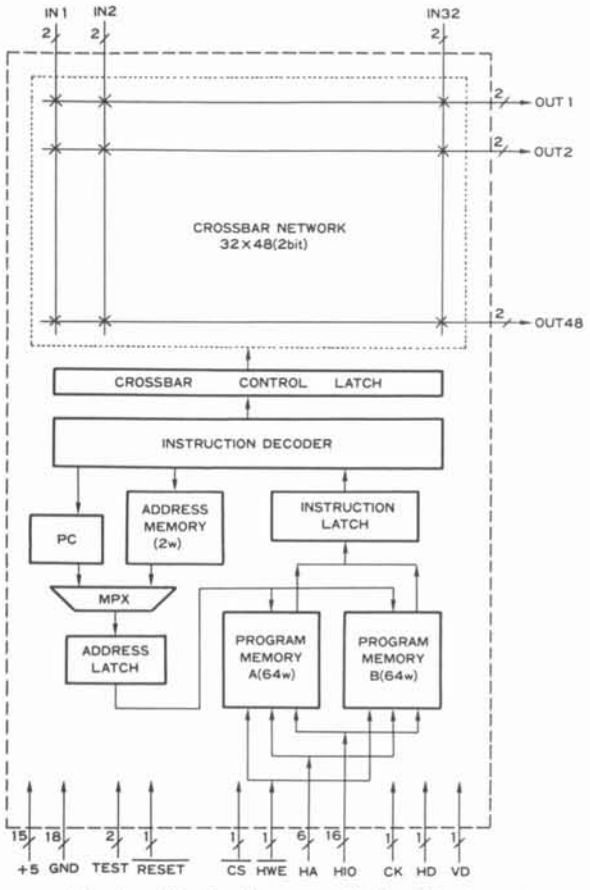


Fig.3 Block diagram of the **Picot-net**

each) of this program memory in the **Picot**.

The interface between the **Picot-net** and the host computer has a protocol similar to that of the **Picot**. Therefore the **Picot-net** can be connected to the same host bus as the **Picot**.

V. APPLICATIONS

The configuration of a typical video signal processing system using **Picots** and **Picot-nets** is shown in Fig.4, in which 16 **Picots** and 9 **Picot-nets** are used up to 16 digital video signals can be input and up to 16 processed image can be output. The throughput of the system is about 250MIPS. Each **Picot** has 512K x 16b SRAM for data memory (DM), a line memory (LM), and 4K x 32b SRAM for program memory (PM). The general register, data memory and program memory of the **Picot** and the **Picot-net** should be mapped to the memory space of the host computer. The HIO can also be used as a data bus. The address bus is connected with the use of a tri-state buffer.

Fig.5 shows an example of operations, that is a noise reducer using a one-frame delay. Processing is switched frame by frame. At the first frame, Picot1 reads the image out of the data memory and sends it to Picot2. Picot2 adds the input IB (previous frame) and input IA (current frame) and outputs the result to OA, and at the same time, writes it in the data memory. At the next frame, the processing in Picot1 and Picot2 is exchanged. The continuous and dotted lines show the flow of processing for each odd and even frame.

Table 1 shows the performance of the **Picots** in processing the image of 512 x 512 pixels.

VI. CONCLUSION

Picot and **Picot-net** LSIs which can be used for the multi-processing of video signals at a rate of 14.3MHz has been developed. By means of arithmetic functions suited to video signal processing and sophisticated control mechanisms, it is possible to process video signals in real-time. The LSIs can be used in a wide range of applications such as robot vision, picture transmission, broadcasting, etc. By using Picots and Picot-nets, it is possible to configure a highly efficient multi-processing system and to construct a small image processing system.

ACKNOWLEDGMENTS

The authors would like to thank Dr. H.Sue of Toshiba Corp. for his kind cooperation, and J.Kutsuzawa, K.Kobayashi, K.Akechi, and K.Kanai of NHK, and A.Yamada and S.Funabashi of Toshiba Corp. for suggestions.

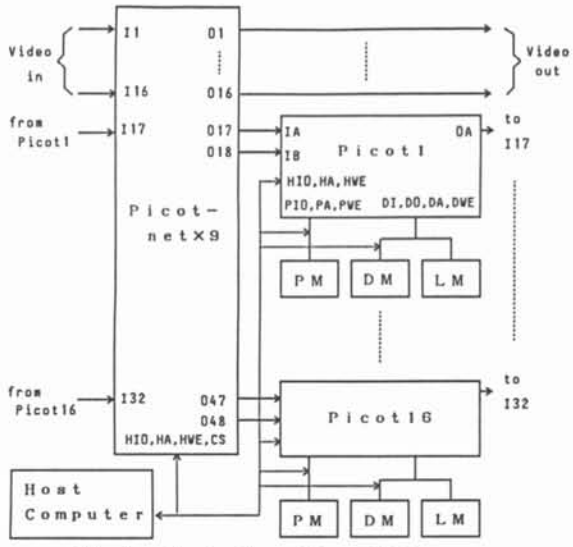
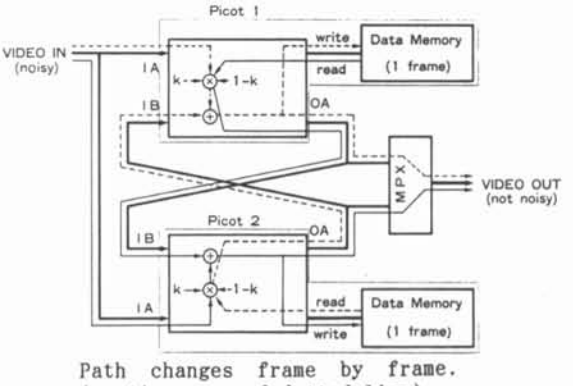


Fig.4 Typical configuration



Path changes frame by frame. (continuous and dotted line)

Fig.5 Example of operation

Table 1 Performance of the **Picots**

Interframe differenciation	20ms(1Picot)
Noise reduction(2x2)	80ms(1Picot), 20ms(4Picot)
Convolution(3x3)	180ms(1Picot), 20ms(9Picot)
Binarization, Gray-scale conversion	20ms(1Picot)
Maximum detection(3x3)	180ms(1Picot), 20ms(9Picot)
Affin transform	20ms(1Picot)
Ensemble between images	20ms(1Picot)

REFERENCES

[1] K.Murakami, K.Enami, N.Yagi: A proposed Universal Signal-Processing System, SMPTE.J., pp527-531, vol.96, No.6, Jun.1987

[2] K.Enami, N.Yagi, K.Murakami: Architecture of a Real-Time Video Signal Processor, ICASSP86, pp793-796, Apr.1986

[3] Y.Kobayashi, T.Fukushima, S.Miura, et al: A BiCMOS Image Signal Processor with Line Memories, THPM15.2,ISSCC87, Feb.1987

[4]K.Aono, M.Maruyama, T.Mori, et al: Implementation of a Bipolar Real-Time Image Signal Processor - RISP-II, IEEE J. vol. SC-22, No.3, pp403-408

[5] M.Yamashina, T.Enomoto, T.Kunio, et al :A Realtime Microprogrammable Video Signal LSI, THPM15.3,ISSCC87,Feb.1987

[6] Encoding Parameters of Digital Television for Studios, CCIR Rec.601, 1982