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Switchable PLL Frequency Synthesizer and Hot Carrier Effects*

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Abstract

In this paper, a new strategy of switchable CMOS phase-locked loop frequency synthesizer is proposed to increase its tuning range. The switchable PLL which integrates two phase-locked loops with different tuning frequencies are designed and fabricated in 0.5 μm n-well CMOS process. Cadence/Spectre simulations show that the frequency range of the switchable phased-locked loop is between 320 MHz to 1.15 GHz. The experimental results show that the RMS jitter of the phase-locked loop changes from 26 ps to 123 ps as output frequency varies. For 700 MHz carrier frequency, the phase noise of the phase-locked loop reaches as low as −81 dBc/Hz at 10 kHz offset frequency and −104 dBc/Hz at 1 MHz offset frequency. A device degradation model due to hot carrier effects has been used to analyze the jitter and phase noise performance in an open loop voltage-controlled oscillator. The oscillation frequency of the voltage-controlled oscillator decreases by approximately 100 to 200 MHz versus the bias voltage and the RMS jitter increases by 40 ps under different phase-locked loop output frequencies after 4 hours of stress time.

Keywords: CMOS Phase-Locked Loop, Voltage-Controlled Oscillator, Hot Carrier Effects, Jitter, Phase Noise

1. Introduction

Phase-locked loops (PLLs) have been widely used in high speed data communication systems. The design, underlying principle of operation and applications are described in numerous publications and text books [1-8]. Present day frequency synthesizers need a broad tuning range for the PLL which sometimes limit the operation of the communication systems. In this paper, we propose a switchable PLL, which combines two relatively narrow bandwidth PLLs into a single chip and uses a frequency detector to decide which PLL to choose according to the reference frequency. As a result, the switchable PLL can work over a wide tuning range and at a high frequency. It also achieves a short locking time without sacrificing the jitter and phase noise performance.

In submicron CMOS devices, the performance of integrated circuits is influenced by the hot carrier effect due to increased lateral channel electric field which results in circuit degradation. Thus, jitter and phase noise may also be affected. Xiao and Yuan [9] have studied hot carrier effects on the performance of voltage-controlled oscillator (VCO). More detailed studies on hot carrier effects in CMOS VCO which is one of the modules of the PLL have been conducted by Zhang and Srivastava [10,11]. In this work, hot carrier effect has been considered and its effect on phase noise and jitter of the CMOS phase-locked loop integrated circuit has been studied.

2. Switchable PLL Design

The design of a switchable PLL is shown in **Figure 1**. Two PLL frequency synthesizers are integrated in a single chip design, one is working in high frequency range and the other is working in low frequency range. Both PLLs include phase-frequency detector (PFD), charge pump (CP), second order loop filter, current starved VCO and 1-by-8 divider. The input range is from 40 MHz to 144 MHz and output range is from 320 MHz to 1.15 GHz. The charge pump and second order low pass loop filter are used to make the system stable and minimize the high frequency noise. The phase frequency detector is designed by using NOR gates and D-flip flops.

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The current starved single-ended voltage control ring oscillator is shown in **Figure 1**. The MOSFETs M1 and M4 operate as an inverter. MOSFETs M7 and M8 operate as a current source, which control the current flowing into the inverter. The oscillation is obtained by charging and discharging the capacitance in each stage of the VCO. To investigate hot carrier effects, VCO circuits in both PLLs are using two modes of operations. The two operation modes are the stress mode and the oscillation mode. V_{mode} control signal realizes the switches of the two operation modes. In both modes, V_{DD} is 5 V. When V_{mode} = 0 V, VCO is working in oscillating mode and is like a normal one. When V_{mode} = 5 V, the transistors connected to V_{mode} are on and act as switches. Thus, a 5 V voltage appears at the drains of transistors M1-M6 as a V_{stress} and hot carriers are injected into their drains. The VCO is not oscillating in stress mode at this stage. After a certain period of stress time, the measurements of jitter, phase noise and oscillation frequency can be obtained and compared by switching between oscillating and stress modes.

The divider-by-2 cell circuit is built in C^2MOS, which is implemented with only 9 transistors as shown in **Figure 2** [12]. Three inverting buffers are used to drive the divider after VCO. There are three cells of divider-by-2 which are connected in series to make 1-by-8 divider work. It can work up to a maximal frequency of 1.5 GHz clock signal.

As shown in **Figure 3**, the switch includes a local oscillator, frequency detector (FD) and a two input multiplexer (MUX). The same kind of VCO as used in PLL design is working as a local oscillator but the difference is that local VCO doesn't have stress mode and the oscillation frequency is locked at 80 MHz. The FD compares the signal from the local VCO with the input reference signal. When the input frequency is higher than 80 MHz, the output of the FD is high which means the

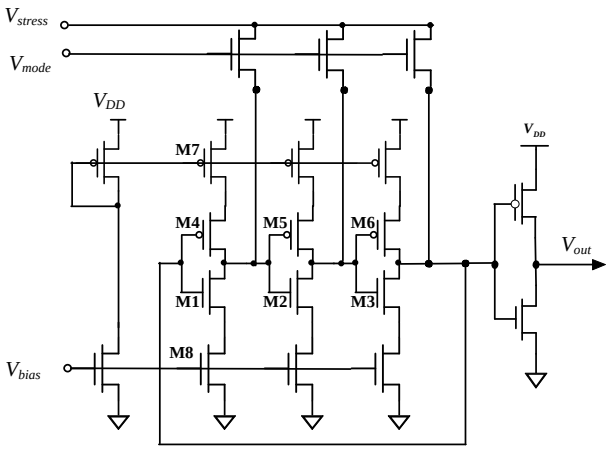

Figure 1. Single-ended CMOS VCO.

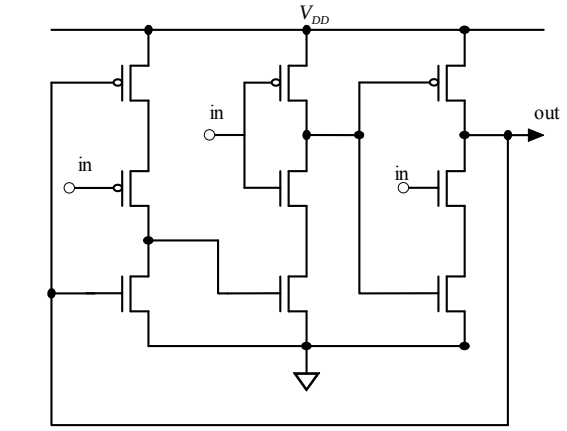

Figure 2. A divide by 2 cell circuit. Note: All three inputs (in) are connected and act as a single input.

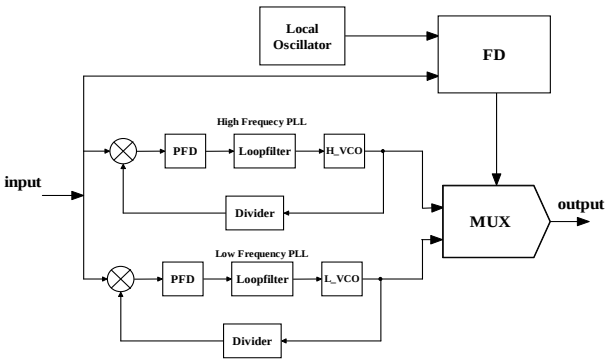

Figure 3. Single-ended CMOS VCO.

high frequency PLL (H_PLL) output signal will go out via the MUX. On the other hand, when the input signal frequency is lower than 80 MHz, the output of the fre-quency detector is low and the low frequency PLL (L_PLL) output signal will go out via the MUX.

The FD circuit schematic is shown in **Figure 4**. The structure of the detector is same with the PFD in each PLL. The RC circuit transfers the output ac signals of PFD to relatively high and low dc voltage signals and comparator compares these two signals to give high or low voltage, which drives the MUX.

Figure 5 shows the loop filter circuit with PFD and charge pump. **Figure 6** shows the schematic of a phase-frequency detector. "Clk" in PFD is from the divider and in FD it is from the "input" in **Figure 3**. **Figure 7** shows the D-flip-flop circuit used in PLL design. The D-flip-flop is a controllable flip-flop that is built with inverters and transmission gates.

3. Hot Carrier Effects (HCE)

As device size shrinks to sub-micron, MOSFETs experience high electric fields with large drain to source

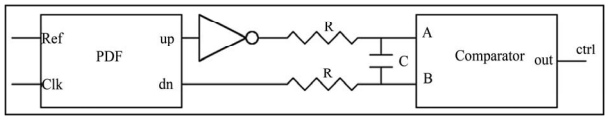

Figure 4. Frequency detector architecture.

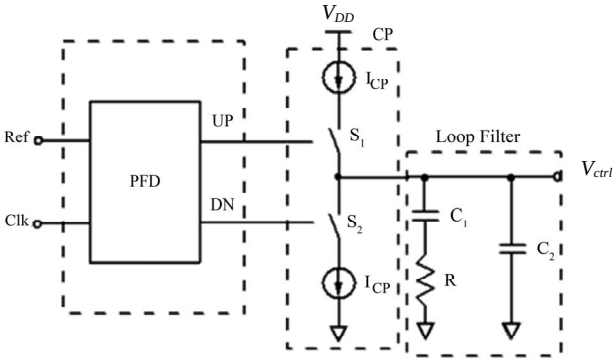

Figure 5. A loop filter with PFD and charge pump.

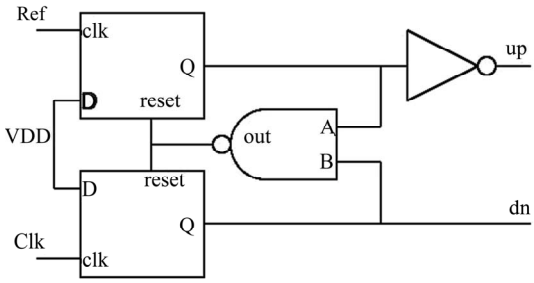

Figure 6. Schematic of a phase-frequency detector (PFD).

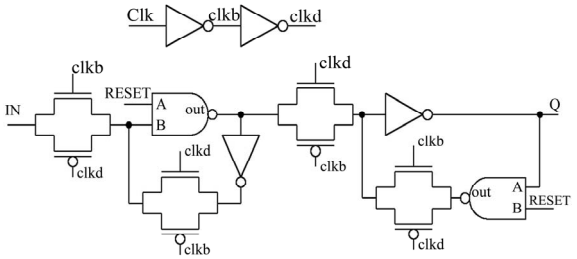

Figure 7. D-flip-flop.

voltage. While the velocity saturation occurs in high electric field, the kinetic energy of the carriers continues to increase. These carriers are known as hot carriers. Hot carriers can cause interface traps and oxide trapped charges. The small geometry devices can be especially influenced and it should be taken into account when dealing with high frequency applications [13]. Hu *et al.* [14] developed a physical model of HCE. When hot electrons gain the energy over 3.7 eV, the interface traps are generated. The interface traps reduce the mobile carrier mobility and density of carriers in the MOSFET which effectively results in increase of the MOSFET threshold voltage. Here the hot carrier effects are investigated under a few hours of stress on MOSFETs. The stress is from external bias voltages on the gate and drain. A few hours of stress generates the degradation of device para- meters.

The parameters of the MOSFETs determine the features of PLL circuit and the stress of hot carrier injection affects the device parameters including the increase of threshold voltage V_t and the decrease of electron and hole mobilities, μ_0.

Zhang and Srivastava [11] have described an experimental model for the degradation of MOS trans- istors due to hot carrier injection. The threshold voltage shift (ΔV_t) from its original value is presented as follows:

$$\Delta V_t = At^m \tag{1}$$

In Equation (1), A is the degradation constant, which is strongly affected by the gate to source stress voltage (V_{GS}) and drain to source stress voltage (V_{DS}). The power, *m* mainly depends on V_{GS} and less on V_{DS}.

The n-MOSFET and p-MOSFET have the same channel length in ring oscillator of **Figure 1**. The oscillation frequency is given by,

$$f_0 = \frac{1}{2nt_D} = \frac{I_D}{nC_L V_{DD}} \tag{2}$$

where V_{DD} is the supply voltage t_D is the delay time of a single inverter and n is the stage number of the ring oscillator. C_L is the load capacitor and I_D is the drain current of M1, M2 and M3 given by Equation(3). V_{DD} is 5 V and *n* is 3 in this circuit.

$$I_D = \frac{1}{2}\mu_o C_{OX}\frac{W}{L}(V_{BIAS} - V_t)^2 \tag{3}$$

In Equation (3), μ_o is the electron mobility, C_{OX} is gate oxide capacitance per unit area, W/L is the channel width to length ratio of n-MOSFET, which decides the frequency of VCO output. V_{BIAS} is the bias voltage and V_t is the threshold voltage. Thus, the gain of VCO output frequency is given by,

$$K_V = \frac{\partial f_0}{\partial V_{BIAS}} = \frac{\mu_o C_{OX}}{n}\frac{W}{L}\frac{V_{BIAS} - V_t}{C_L V_{DD}} \tag{4}$$

From Equation (4), it is shown that the drain currents of n-MOSFETs M1, M2 and M3 affect the frequency and the frequency gain of the VCO. It means that the device parameters of those n-MOSFETs have impacted the VCO performance by hot carrier injection. The hot carrier effects can be modeled by modifying n-MOSFETs parameters, μ_0 and V_t.

3.1. VCO Jitter

The jitter proportionality constant κ is given by [12],

$$\kappa \approx \sqrt{\frac{8}{3\eta}} \cdot \sqrt{\frac{kT}{P} \cdot \frac{V_{DD}}{V_{char}}} \tag{5}$$

where T is the temperature in Kelvin and k is the Boltzmann constant. η is the proportionality constant relating the delay of the VCO which is 0.75 for sub-micron MOSFETs. V_{char} is the characteristic voltage of the device, $V_{char} = \Delta V / \gamma$. γ is the noise ratio between the saturation and linear regions, and is $4/3$ for a short channel device. ΔV is the overdrive voltage on the gate given by,

$$\Delta V = V_{DD}/2 - V_t - \Delta V \tag{6}$$

P is the power dissipation given by,

$$P = nV_{DD}I_{DD} \tag{7}$$

The variability of VCO jitter accumulates as a function of ΔT, interval time between the reference clock and the observed clock. ΔT is equal to 6.7 ns due to difference in delay between the signal input of oscilloscope and the trigger input. We use the threshold crossing time, $\sigma_{\Delta T}$ to quantitatively denote the deviation of the jitter as follows,

$$\sigma_{\Delta T} = \kappa\sqrt{\Delta T} \tag{8}$$

3.2. VCO Phase Noise

Jitter and phase noise are different ways to express the same phenomenon. The method described in subsection 3.1 can be used to model VCO phase noise. For CMOS single-ended VCO, the expression of phase noise is given by [15,16],

$$L\{\Delta f\} \approx \frac{8kT \cdot V_{DD}}{3\eta \cdot P \cdot V_{char}} \cdot \frac{f_0^{\,2}}{\Delta f^{\,2}} \tag{9}$$

4. Analysis

Figure 8 shows the output of the switchable PLL at different frequencies where 320 MHz waveform is the low frequency PLL (L_PLL) output and 1.12 GHz waveform is the high frequency PLL (H_PLL) output.

Figure 9 shows the variation of PLL output frequency versus control voltage, with and without hot carrier effects. Both the oscillation frequency and frequency range of the PLLs decrease. For the worst case, the over-lapping frequency range, which is 250 MHz without hot carrier effects, decreased to 200 MHz.

The function of RC in the frequency detector is to translate the FD output pulses into dc voltages, which are shown in **Figure 10**. If the input frequency is less than the reference frequency, which is output of the local oscillator defined as 80 MHz, the output is at low level; while if the input frequency is higher than the reference frequency, the output is at high level. But if the input frequency is closer to the reference frequency it will take more time to obtain the dc output. **Figure 11** shows this phenomenon.

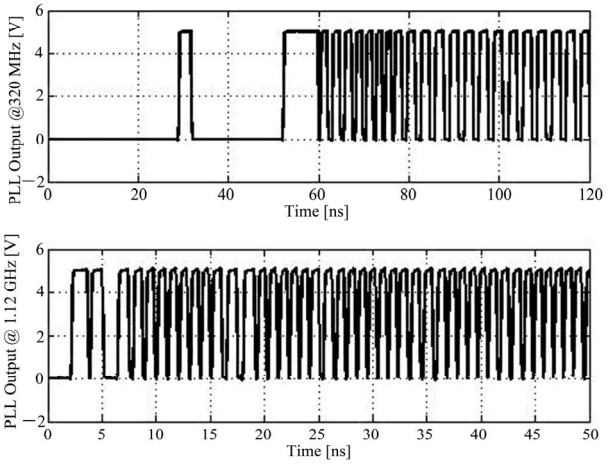

Figure 8. Switchable PLL outputs at different frequencies.

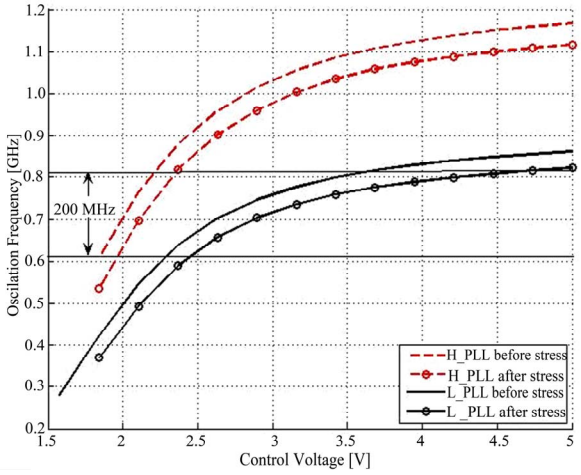

Figure 9. Hot carrier effects on frequency synthesizer.

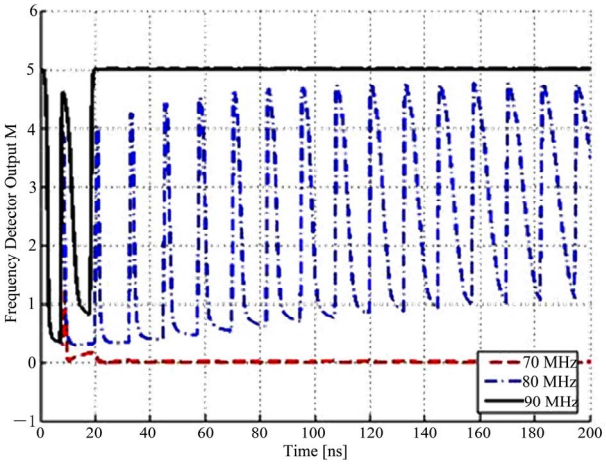

Figure 10. Frequency detector output.

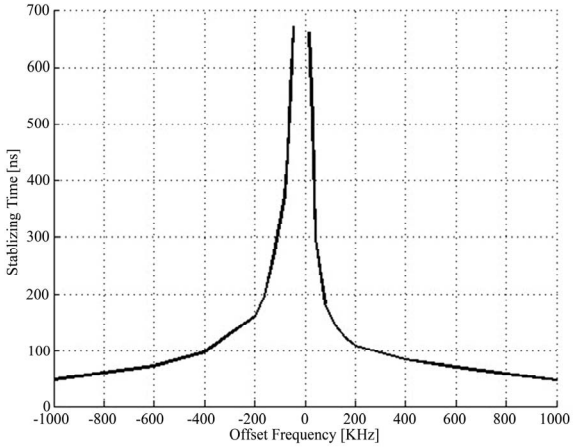

Figure 11. Frequency detector stabilizing time versus frequency.

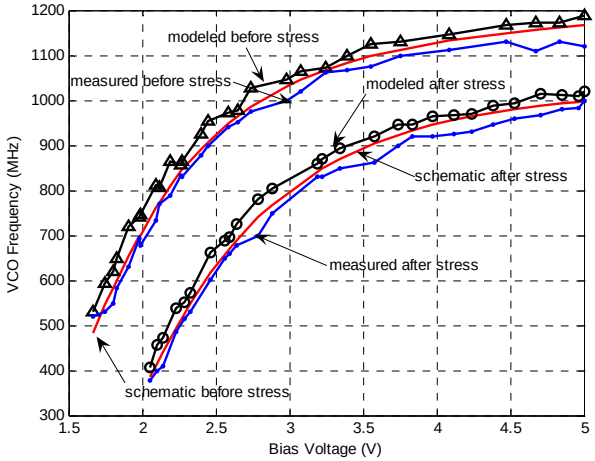

Figure 12. The degradation of VCO frequency due to hot carrier effects.

When the input frequency equals the reference frequency, the output will be oscillating and the stable time will be infinity as shown in **Figure 11**. To deal with this problem, the frequency over-lapping range of the two PLLs is expanded.

It can be noticed that the over-lapping range is at least 200 MHz in **Figure 9**. Thus, if the input frequency is close to reference frequency (80 MHz) the control voltage of the local oscillator can be adjusted to change the reference frequency higher or lower. The large over-lapping range guarantees that the difference between the input frequency and the local oscillator frequency is large enough so that the stabilizing time is smaller than 200 ns, which is the stabilizing time of the high frequency PLL. As a result, the stabilizing time of the switchable PLL is decided by the PLLs, while the operation range is much larger than that of the single PLL.

5. Simulation and Experimental Results

5.1. Simulation Results for H-PLL VCO due to Hot Carrier Effects

Figure 12 shows the simulation, modeled and measured results of the oscillation frequency of open loop VCO in H_PLL before and after hot carrier stress versus different bias voltages. The modeled results are in good agreement with the simulation and measured results. The simulation results are performed by Cadence/Spectre. It is shown that at a 4 V bias, the frequency is around 1150 MHz before stress and it is about 950 MHz after stress. This is the effect on VCO output frequency due to hot carrier injection in MOSFETs.

Figure 12 includes experimental data on tuning range of VCO whose operation frequency is slightly lower than the simulation one. Phase noise and jitter measured under hot carrier stress for both VCO and PLL are reported in subsection 5.2. Threshold voltage increases by approximate 120 mV and the electron mobility decreases by about 80 cm^2/Vsec [9] after 4 hours of stress on MOSFETs.

Figure 13 shows the decrease of H_PLL VCO frequency gain at 2.5 V bias voltage versus stress time, which agrees with the Equation (4). After 4 hours of hot carrier injection, the VCO gain decreases by about 33%, from 460 MHz to 310 MHz.

Figure 14 shows the simulation result for the variation of the jitter proportionality parameter, κ changing with the oscillation frequency before and after 4 hours of stress. κ increases by about 10%, which means the value of the jitter of 3-stage single-ended VCO increases by about $0.2\sqrt{\Delta T}ns$ due to hot carrier effects from Equation (5). ΔT is the time difference between rising edge of trigger clock and the observed clock. Thus, the jitter $\sigma_{\Delta T}$ mainly depends on κ, which varies with different tuning frequencies.

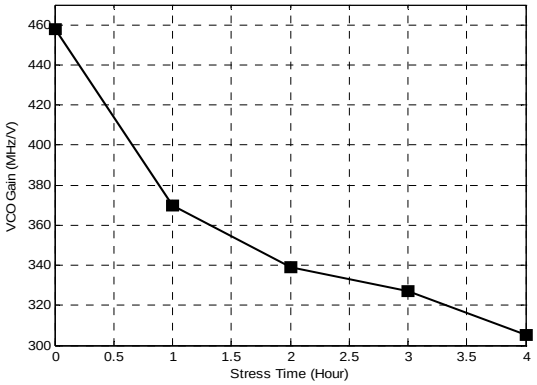

Figure 13. VCO gain versus stress time.

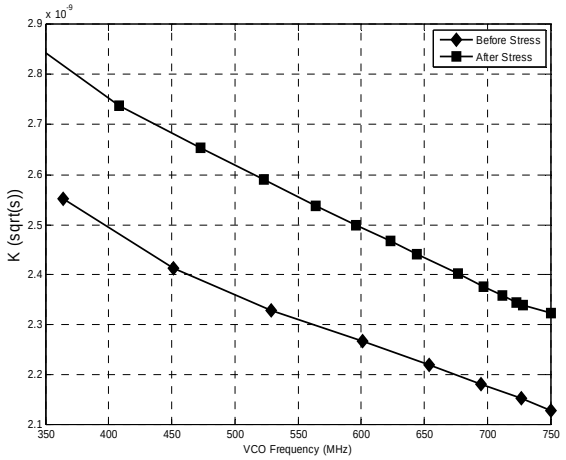

Figure 14. The dependence of K and VCO frequency due to hot carrier effects.

5.2. Experimental Results

Figure 15 shows the experimental and modeled phase noises of the open loop VCO at 1 GHz oscillation frequency before and after hot carrier stress. The experimental results which are from open loop VCO circuit in the chip are in good agreement with the modeled phase noises which are calculated from Equation (9).

Figure 16 shows the experimental results of device degradation on RMS jitter performance under different PLL output frequencies due to hot carrier effects. A 40 ps increase is observed after 4 hours of stress.

The experimental results for PLL output frequencies with and without hot carrier effects are listed in **Table 1**, measured using Tektronix 11801A Digital Sampling Oscilloscope and Agilent ESA-E4404B Spectrum Analyzer.

Figure 17 shows a photograph of the switchable PLL jitter performance measured by a digital sampling oscilloscope.

Figure 18 shows the experimental results of PLL output phase noise at 700 MHz carrier frequency by using Agilent ESA-E4404B Spectrum Analyzer, before and after stress. The offset frequency is from 10 kHz to 1 MHz. In **Figure 18**, the PLL phase noise before stress is −81 dBc/Hz at 10 kHz offset frequency and is around −104 dBc/Hz at 1 MHz offset frequency. The PLL phase noise increases by about 1-2 dB relative to carrier power per Hertz after four hours of hot carriers stress.

The switchable PLL described in the present work was fabricated in 0.5 μm n-well CMOS process. **Figures 19** and **20** show the cadence/virtuoso layout and the microphotograph of the fabricated switchable PLL chip. **Figure 21** shows the RF test board with mounted PLL chip which is specially designed for this experiment. The chip output is connected to Agilent ESA-E4404B Spectrum

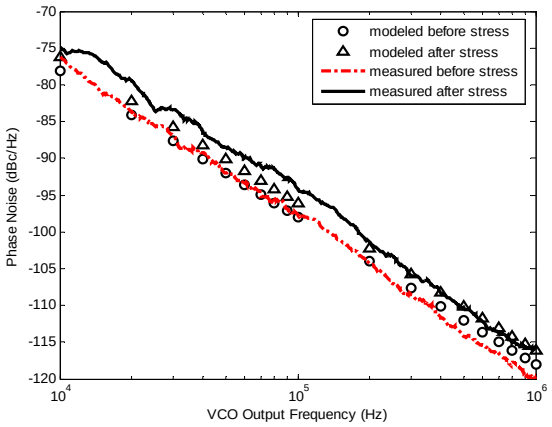

Figure 15. Degradation on phase noise performance under 1 GHz oscillation frequency.

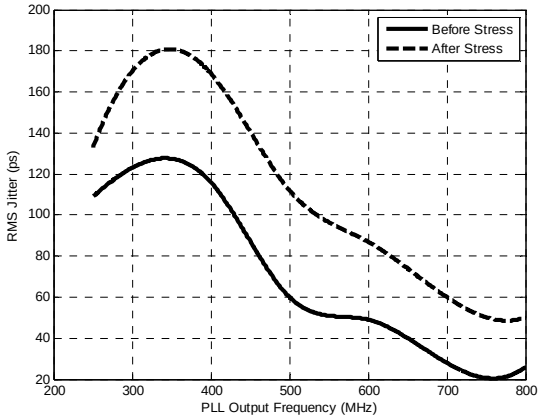

Figure 16. Experimental results of PLL jitter.

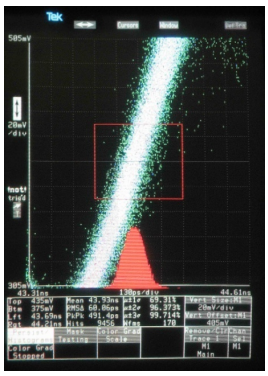

Figure 17. A photograph of PLL jitter.

Analyzer with built-in phase noise module. The RF module is powered by VDD = 5 V and VSS = 0 V.

6. Conclusions

A new design is proposed to expand PLL tuning range without sacrificing its speed and jitter and phase noise

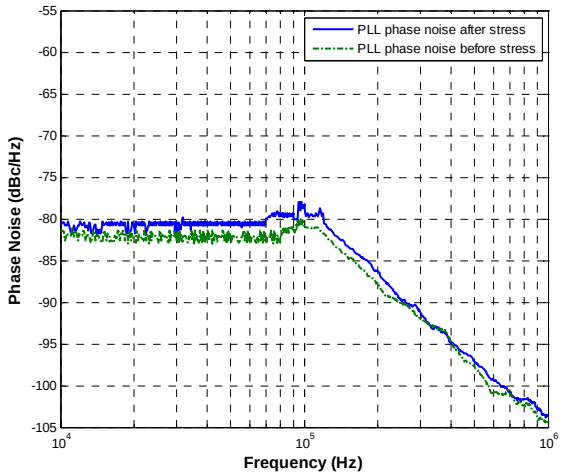

Figure 18. Experimental results of PLL phase noise at 700 MHz carrier frequency.

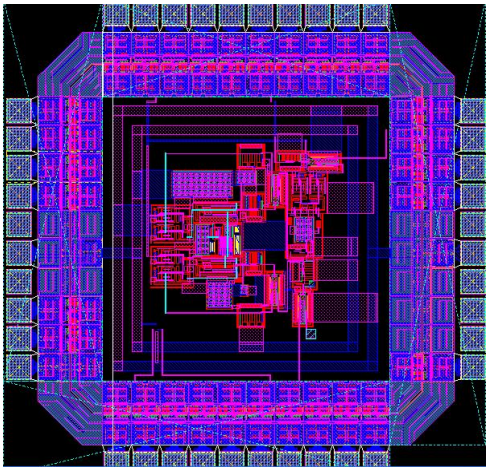

Figure 19. Layout of switchable PLL frequency synthesizer.

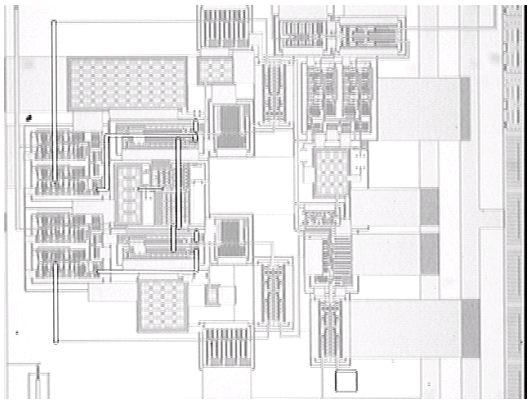

Figure 20. Microphotograph of fabricated switchable PLL.

performances. The two CMOS PLLs are integrated on a single chip. Cadence/Spectre has been used for post-layout simulations for jitter, phase noise and switchable frequency range. The chip is experimentally tested for

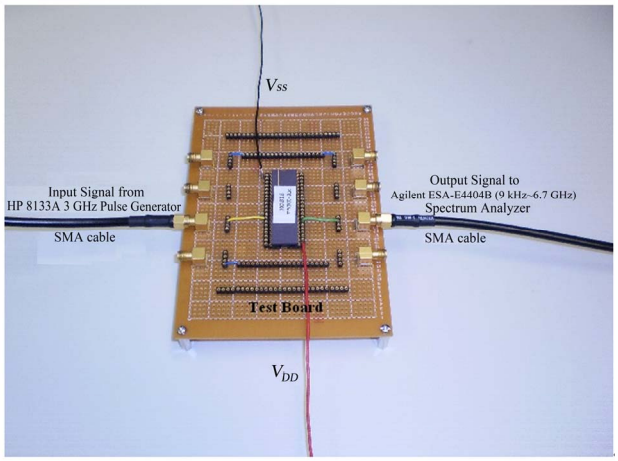

Figure 21. Photograph of RF test board with mounted PLL chip.

jitter, phase noise and switchable frequency range with and without hot carrier effects. A model is presented to address the hot carrier effects on the VCO jitter and phase noise performance. The modeled results are in good agreement with both the simulation and experimental results. It is demonstrated that the jitter can be predicted by the jitter proportionality parameter, κ. The measured jitter and phase noise ranges of the PLL are around 26 to 123 ps and around −69 to −126 dBc/Hz under the entire PLL tuning frequency, 200 MHz –700 MHz.

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