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CMOS Phase and Quadrature Pulsed Differential Oscillators Coupled through Microstrip Delay-Lines

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Abstract

An innovative solution to design phase and quadrature pulsed coupled oscillators systems through electromagnetic waveguides is described in this paper. Each oscillator is constituted by an LC differential resonator refilled through a couple of current pulse generator circuits. The phase and quadrature coupling between the two differential oscillators is achieved using delayed replicas of generated fundamentals from a resonator as driving signal of pulse generator injecting in the other resonator. The delayed replicas are obtained by microstrip-based delay-lines. A 2.4 - 2.5 GHz VCO has been implemented in a 150 nm RF CMOS process. Simulations showed at 1 MHz offset a phase noise of −139.9 dBc/Hz and a FOM of −189.1 dB.

Keywords

Voltage Controlled Oscillator, Microstrip, Delay-Line, Phase and Quadrature, Phase Noise

1. Introduction

Pushed from the ever-increasing demand in the electronic devices market for personal mobile devices and for wireless sensor networks, the research on innovative techniques for lowering energy requirements and costs of the electronic hardware is an extensively treated subject. At the core of every of above mentioned device, certainly an RF-IC resides, since it accomplish the necessary functional block for the establishment of a RF communication. In particular, the upconversion/downconversion task in RF-ICs usually represents the subsystems involving the major wafer area and power consumption. Toward the reduction of both areas occupation and power are placed CMOS Pulsed Bias Oscillators (PBOs). The PBO approach represents a technique exploiting the time-varying

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properties of electronic oscillators system. This technique can be applied to oscillators constituted of harmonic resonators refilled by active devices acting as current generators. This oscillator class aims to reach high performance in terms of phase noise with reduced energy requirements with respect to their non-pulsed counterparts. Basing on the results of Floquet Theory applied to a single oscillator [1], we extended the pulsed bias concept to a coupled phase and quadrature system in [2]. We proved that the pulsed bias approach allows to minimize noise injection onto the Floquet Eigenvector with unitary eigenvalue, leading to decrease phase noise of generated fundamental in particular at low frequency offsets [3] [4]. However, in the effective implementation of pulsed bias architectures, the introduction of a delay is necessary for proper positioning of refilling current pulses. In the most common way, a delay can be obtained with the charging of a capacitor through a dissipative media [5]. Unfortunately, using an RC-based delay is not possible to set the pulse width independently from the pulse position. This issue is explained considering that, in the cascading of lumped elements circuits, the total delay time strictly depends on the number of stages and how they are connected. In this paper we propose a circuital solution based on the joint use of decoupling stages from resonator and of microstrip delay-lines capable to break such constraint and, at the same time, to establish coupling among oscillators with a desired phase relation. The paper is organized as follows. In Section II the proposed architecture is introduced, focusing on the explanation of the concept for the coupling between two oscillators in phase and quadrature. In Section III the theoretical analysis of the delay-line is pursued and insights for proper design are derived. In Section IV the implementation on RF CMOS process is reported and simulation comparison with a non-pulsed architecture built in the same technology is discussed as well as a comparison with literature is given.

2. Proposed Architecture

The outputs of a phase and quadrature oscillator are phase shifted replicas of a fundamental frequency f_0 as drawn in **Figure 1**.

The voltage maximum of a delayed sinusoid from a resonator can be hence used to generate refilling pulses, synchronized at output voltage minimum of another resonator. Thus in this paper, we propose to couple two oscillators applying a fixed delay of $T_0/4$ where $T_0 = 1/f_0$. In particular we choose to realize the delay by a microstrip transmission-line.

In a lossless transmission-line the secondary constants Z_c, characteristic line impedance, and β_z, propagation constant, are both real number. The voltage of the transmission-line equation as a function of the z is given by $V(z) = V_0^+ \mathrm{e}^{-j\beta_z z} + V_0^- \mathrm{e}^{+j\beta_z z}$. If the load is matched to the Z_c, the contribution of the regressive term V_0^- is negligible and the transfer function between the input port, at $z = -l$, and the output port, $z = 0$, of the transmission-line results in

$$H(\omega) = \frac{V(0)}{V(-l)} = \mathrm{e}^{-j\beta_z l} \tag{1}$$

where l is the total line length.

If β_z has linear increase with frequency, the transmission-line behaves as a delay-line. The delay $T_0/4$ is related to the l, through

$$\beta_z l = \omega \frac{T_0}{4} \tag{2}$$

where ω is evaluated at the fundamental frequency $\omega_0 = 2\pi f_0$ along with β_z. Hence, the value of l is established considering the condition $l = \pi/(2\beta_z)$ holds. For the refilling of all the tanks, four transmission-lines in a phase and quadrature PBO (PQPBO) are needed.

The reference schematic of the oscillator is presented in **Figure 2**. The system is formed by four coupled LC tanks, subdivided in two blocks, I and Q, respectively. The two inductances of every single block are implemented by center tapped inductors. All the capacitances are implemented by MIM capacitors. The value of L and C were set to obtain operative center frequency of 2.45 GHz, suitable for ISM applications, according to $f_0 = 1/2\pi\sqrt{LC}$.

The losses are compensated by the introduction of the current pulse generators (PG) as showed in **Figure 2**. The PG circuit is reported in **Figure 3**.

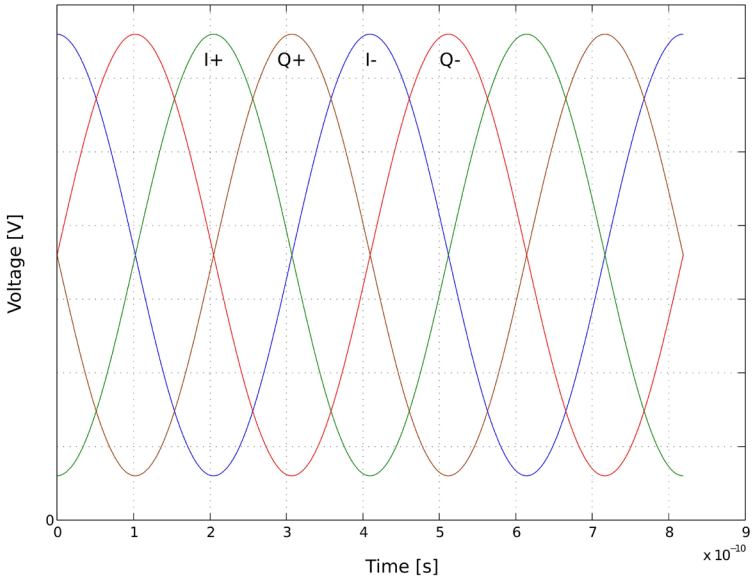

Figure 1. Typical output signals of a phase and quadrature oscillator.

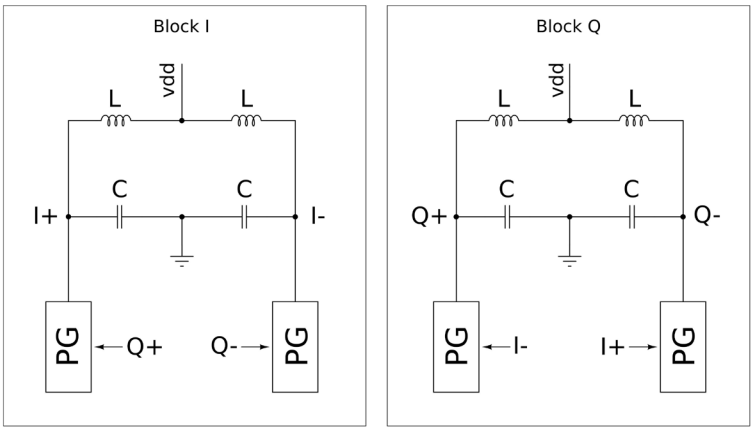

Figure 2. Oscillator schematic of the proposed PQPBO.

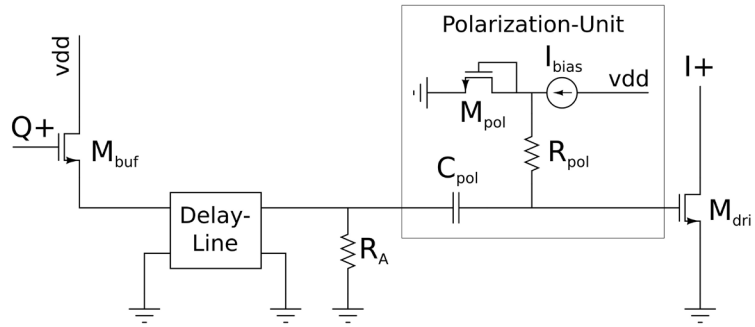

Figure 3. Pulse generator schematic.

The following description refers to the PG recharging the $I+$ tank node and driven by the signal coming from $Q+$ tank node. The buffer transistor M_{buf} provides to decouple the Delay-Line (DL) from the source tank $Q+$, in order to prevent energy absorption by the PG. The observed impedance at the DL input is Z_c once the DL load is matched. Then the decoupling stage is implemented as a source-follower with a resistive load as

reported in **Figure 3**. In order to maximize the voltage transfer between the gate and the source of M_{buf}, both the input capacitance $C_{gs,buf}$ and the body effect must be taken into account. A practical rule for initial sizing of M_{buf} is to set its length to the process minimum and to determine the upper bound for its width using

$$C_{gs,buf} \leq 0.1C \tag{3}$$

This bound grants an effective isolation of the resonator from the loading effect of PG input. Then, a triple-well is used to connect the M_{buf} bulk at its source voltage rather than to global ground. To avoid a large power consumption in the decoupling stage a sub-optimum value for the M_{buf} transconductance must be chosen. The M_{buf} transconductance, modeled in quadratic region, results in $g_{m,buf} = \left(2\mu C_{ox} W_{buf} / L_{buf} I_D\right)^{1/2}$, where μ, C_{ox} are carriers mobility and oxide capacitance per unit area of the adopted technology and M_{buf}, L_{buf} are transistor width and length, respectively. If $C_{gs,buf} = C_{ox} W_{buf} L_{buf}$ is inferred from geometrical consideration (neglecting the dependence on transistor operating region), we can derive an upper bound for M_{buf}. In fact, descending from Equation (3) it implies $W_{buf} \leq 0.1C / C_{ox} L_{buf}$ and, thus, the transconductance bound results in

$$g_{m,buf} \leq \frac{1}{L_{buf}} \sqrt{0.2\mu C I_D} \tag{4}$$

This bound must be accounted because an eventual low $g_{m,buf}$ reduces the source dynamics. It worth to notice that, since the source-follower is active only if the V_{gs} threshold is reached, in a C-class pulse generating system driven by the large oscillating signal this represents an advantage. In fact, the decoupling stage takes part in the pulse shaping even though the desired pulse width and positioning cannot be set in this stage.

To this aim, the DL is introduced to obtain the delay necessary to synchronize the refilling instant. The values of Z_c and β_z are determined through literature formulas [6] [7] for a microstrip structure, whereas the dimensions of the strip width W, height h and the interposed dielectric relative electric permittivity ε_r are consistent with the process specifications. Values of the transmission-line secondary constants represent here only a first order of approximation of the integrated waveguide, since both the dissipation effects and the presence of a dielectric over the strip are ignored. Such constants result in $Z_c = 106.6\ \Omega$ and $\beta_z = 1.72\,\omega / c_0$, where c_0 is the speed of light in vacuum once a quasi-TEM mode of propagation in the strip has been assumed. Referring again to **Figure 3**, the matching resistance R_A in introduced to add one more degree of freedom in minimization of the reverse wave contribution in the DL. The DL matching technique is discussed after the description of PG stages.

The Polarization-Unit (PU), formed by C_{pol}, R_{pol}, I_{bias} and M_{pol}, achieves the task to fix the DC value of the driver transistor gate M_{dri} in order to set its operative region in C-class region. Further, the PU grants the proper start-up of the oscillator, since the gate node voltage of M_{dri} is initially at V_{dd} and then settles to the required n-MOS sub-threshold value. The C_{pol} has obviously the role of decoupling DC voltage of M_{dri} gate and of blocking DC current flow to reverse DL path, however for its proper sizing both input capacitance $C_{gs,dri}$ of driver transistor and the time constant τ_s, involved in the operating point voltage settling, must be accounted. Again, a practical rule for C_{pol} sizing suggests to take

$$C_{pol} \geq 10C_{gs,dri} \tag{5}$$

and, descending from this choice, the derivation of the equivalent resistance, R_{eq}, and capacitance, C_{eq}, for calculating τ_s, results in

$$\tau_s = C_{eq} R_{eq} = 10C_{gs,dri} \left[\left(R_{pol} + \frac{1}{g_{m,pol}} \right) \| R_A \| R_{DL} \right] \tag{6}$$

where $g_{m,pol}$ is the M_{pol} transconductance and $R_{DL} = \left(g_{m,buf}^2 Z_c\right)^{-1}$ represents the impedance of the quarter-wave DL transformer loaded by the source follower. In R_{eq} calculation the parallel branch resistance of M_{dri} transistor has been neglected, since the gate node capacitance $C_{gs,dri}$ relates to a time constant with a more rapid exponential decay than τ_s, which does not alter the final settling voltage. If the desired time for the oscillator stabilization is identified in τ_{stab}, hence the condition for dimensioning R_{eq} is derived from $\tau_s < \tau_{stab}/5$ (exponential decay approaches the final value within $<1\%$ error).

$$R_{eq} \le \frac{t_{stab}}{50 C_{gs,dri}} \tag{7}$$

We notice in R_{eq} expression only the couple R_{pol}, $g_{m,pol}$ can be effectively adjusted to set the proper τ_s.

Finally, the M_{dri} transistor generates a current pulse that re-inject charge in the destination tank $I+$. The sizing of the driver transistor of the PG is chosen to fulfill at least two times the Barkhausen criterion, once the resonator losses, R_{loss}, related to resonator RLC parallel model, have been determined. The criterion is expressed in

$$\frac{1}{g_{m,dri}} > 2R_{loss} \tag{8}$$

It worth noticing the $g_{m,dri}$ parameter is calculated assuming the highest overdrive voltage with the gate voltage at V_{dd} as the M_{dri} transistors were arranged in a standard crossed pair architecture. This assumption leads to potentially over-estimate the necessary driver transconductance when it is operating in C-class region. In fact it is expected that C-class operation, representing a more efficient energy refilling, may allow to decrease the effective M_{dri} size in actual design of oscillator.

Follows the DL matching description. In first approximation, DL is described with its secondary constants Z_c and β_z in lossless case. The reflection coefficient at the load of the line is Γ_L. The load Z_L of the DL is formed by R_A and the input capacitance C_{gs} of the M_{dri} transistor, since the PU at f_0 is negligible because C_{pol} and R_{pol} behave as a short and an open circuit, respectively. Being reflection coefficient expressed as $\Gamma_L = (Z_L - Z_c)/(Z_L + Z_c)$ where $Z_L = (R_A / j\omega C_{gs,dri})/(R_A + 1/j\omega C_{gs,dri})$, the condition $|\Gamma_L| = 0$ cannot be imposed because of the resistive matching, but the value of $|\Gamma_L|$ can be minimized with a proper value of R_A. The values range of C_{gs} is obtained through the testing of the input capacitance of several sizing for M_{dri}.

In **Figure 4** the reflection coefficient as a function of R_A is reported for $C_{gs,dri} = 200$ fF and $Z_c = 106.6\ \Omega$. The minimum of $|\Gamma_L|$ is given by setting $R_A = 101\ \Omega$ and this optimum has been achieved through fine dimensioning of M_{dri} in simulations.

The delay-line is characterized by the transfer function on the l variable

$$H(l) = \frac{1+\Gamma_L}{e^{+j\beta_z l} + \Gamma_L e^{-j\beta_z l}} = e^{-j\beta_z l} \tag{9}$$

that takes into account $|\Gamma_L| \neq 0$. The value of l obtained with Equation (2) must be hence reduced to satisfy the condition $\angle H(l) = -90$ deg in Equation (9) at fundamental frequency, which is the dominant spectral component in the signal into the PG.

3. Delay-Line Implementation

The DL unit is implemented through a waveguide structure such a microstrip. As a first microstrip design step, literature formulas [6] [7] can be used to obtain the desired Z_c and β_z. Further, foundry process constraints have to be accounted especially in the microstrip sizing. To this aim, CST Microwave Studio™ was used to obtain a proper sizing of the microstrip. In order to reach a trade-off between the value of Z_c and minimization of resistive losses, an intermediate metallization level in chip back-end has been chosen. Below the microstrip there are an interposed dielectric and a patterned ground-plane in a lower metallization level. At sides and above, the microstrip is surrounded by a dielectric, followed by a final passivation layer on top of the die. The microstrip width W is about 500 nm and the interposed dielectric thickness h is 500 nm. In order to obtain a feasible waveguide structure in a given area, the microstrip distribution has been folded into meanders.

In **Figure 5** a detail of the microstrip layout is reported. In black the basic module of the meander is highlighted in red. In detail of layout U_m is the distance between two neighbouring strips, U_l is the length of a meander and H_{tot} is total length of the structure. In order to reduce the radiation loss of the waveguide we adopt smoothing of the corners as reported in **Figure 5**. Unfortunately, the optimum solution proposed in [8] is unrealizable since, in our case, it leads to width zone of the corners lower than that allowed by the foundry rules. We hence choose to compensate the capacitive effect of the corners with a smoothing of side equal to the microstrip width W.

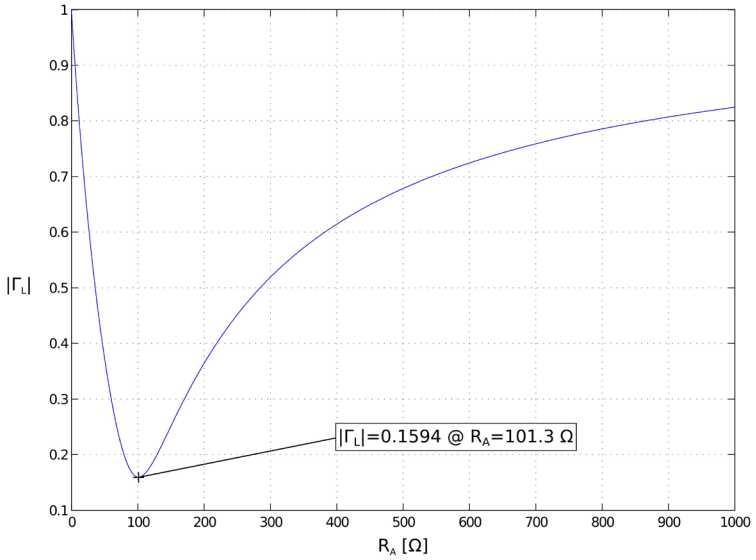

Figure 4. Reflection coefficient as a function of R_A.

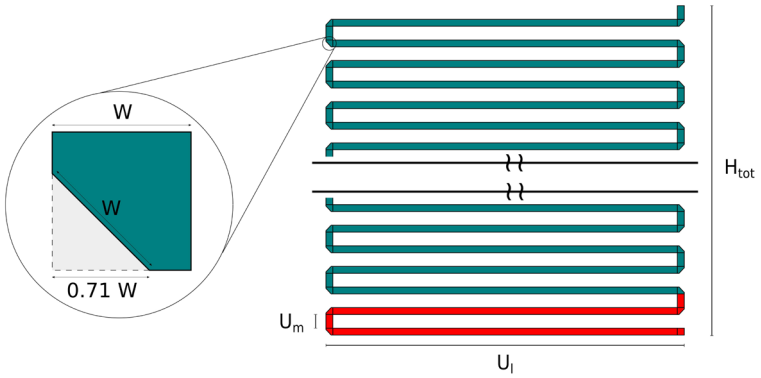

Figure 5. Detail of layout of the proposed folded microstrip delay-line.

The distance U_m had been determined through dedicated simulations in order to minimize the interaction between two neighbouring strips. In such simulations a simplified microstrip with four meanders is implemented, as shown in **Figure 6**, where the value of U_m is progressively increased until the simulated scattering parameters values achieve the desired 0.2 dB convergence level (that is the maximum expected variation due to 5% of trace length mismatch). The number of meanders was set to four in order to enhance the effect of the neighbour strips interaction on the scattering parameters. The length of each meander finger is imposed to $U_l = 150$ μm in order to make the final structure area possibly lower of that one occupied by inductors. The two termination branches are perpendicular to meander fingers in order to minimize their interaction with the meander itself. Their length L_T decrease as the U_m increases to maintain constant the total strip length according to

$$L_T = 30\ \mu\text{m} - \frac{7}{2}U_m \tag{10}$$

If the condition in Equation (10) is not respected, the scattering parameters variation also depends on the U_m increasing the total effective strip length. Simulations on the model showed that the scattering parameters convergence occurs at $U_m \geq 2W$.

The microstrip reported in **Figure 5** has been sized in order to obtain the $T_0/4$ delay between the input voltage maximum and the output current maximum of the PG. For this purpose, a circuital test-bench formed by a PG and two Thevenin equivalent generators has been simulated. These equivalents generators provide to model the tanks DC and fundamental behaviours at nodes $Q+$ and $I+$ including the observed impedance.

Figure 6. Simplified folded microstrip delay-line.

$$Q+:\begin{cases} V_{th1} = V_{dc} + \hat{V}\cos(\omega_0 t) \\ Z_{th1} = (R_{loss} + j\omega L + 1/j\omega C) \end{cases}$$
$$I+:\begin{cases} V_{th2} = V_{dc} + \hat{V}\cos(\omega_0 t + 90 \text{ deg}) \\ Z_{th2} = (R_{loss} + j\omega L + 1/j\omega C) \end{cases} \quad (11)$$

The value of $\hat{V}$ is chosen less than 80% of the $V_{dc} = 1.8$ V in order to consider the saturation effect of the drivers M_{dri} into the fundamental signal amplitude. L and C are the tank inductance and capacitance, respectively. R_{loss} is the observed parallel resistance at the resonance frequency ω_0.

The length of the microstrip is initially chosen by Equation (9). Progressive adjustments of the U_l lead to the proper positioning of the refilling current pulse on the test-bench. In this manner, a simulations loop has been created. The microstrip scattering parameters are calculated with CST Microwave Studio® and exported, through a Touchstone file, into SpectreRF® which in turn, simulating the test-bench, gives the indication to next adjustment step of the microstrip length L_{tot} into the 3D simulator. At the end of such process, to reach the desired delay a total length of the microstrip $L_{tot} = 8.47$ mm is needed. This length requires a number of $N = 32$ meanders with $U_l = 130$ µm. Furthermore, the microstrip area has been optimized to conform it in square shape by means of a dedicated routing algorithm. Finally the process variations regarding metallization levels involved in the delay-line design have been accounted with two corners, a short-line case and a long-line case with respect to the nominal length. The simulated variations on nominal scattering parameters for these two corners are evaluated in < 0.2 dB, a value close to the convergence level, thus, hereafter we consider them as negligible.

4. Simulation Results and Literature Comparison

The oscillator has been implemented in the LFoundry 150 nm RF CMOS process with a tuning frequency range spanning the $2.4 - 2.5$ GHz ISM band by a 4-bit digitally selectable capacitors bank. All the simulations were run with SpectreRF® simulator in Cadence® 6.1.5 environment. The inductance per branch of the center tapped inductor is $L = 0.33$ nH whereas the fixed capacitance used to set the upper bound of the 2.5 GHz band is $C = 11.65$ pF. The sizing of driver transistors following the Equation (4) results in a total of $W_{dri} = 35$ µm on $L_{dri} = 350$ nm, whereas the optimal sizing of the buffer transistors has been found in $W_{buf} = 15$ µm on $L_{buf} = 150$ nm. The adopted settling time is set in $\tau_s = 50$ ns obtained via $C_{pol} = 10$ pF and $R_{pol} = 5$ kΩ. The proposed architecture is first compared to a reference voltage limited phase and quadrature differential VCO implemented with a replica of the PQPBO resonator and based on the architecture proposed in [9] without the top PMOS crossed pair. Then the results of PQPBO are compared to recent literature

phase and quadrature oscillator built in state of the art CMOS technologies and running at similar frequencies.

In architecture proposed in [9] the coupling between the two oscillators is reached by the introduction of coupling transistors in parallel to the crossed pair transistors. The crossed pair transistors of reference quadrature VCO, indicated with M_{CP}, have total $W_{CP} = 30\ \mu\text{m}$ on $L_{CP} = 350\ \mu\text{m}$ sizing, whereas coupling transistors, indicated as M_{COU}, have total $W_{COU} = 8\ \mu\text{m}$ on $L_{COU} = 350\ \mu\text{m}$ sizing. The W_{COU} dimension has been chosen as the minimum width granting the effective quadrature. Process variations and mismatches of active devices dimensions of both proposed and reference oscillators play a negligible role, since all of them work in large signal condition (comprising the M_{dri} with a not so sensitive gate polarization voltage).

In the first comparison the oscillation amplitudes are kept at a fixed level of $1\ \text{V}$, whereas the maximum supply voltage for this technology $1.8\ \text{V}$.

In **Figure 7** the transient PSS node voltages of $Q+$ and $I+$ are reported for PQPBO running at $2.45\ \text{GHz}$. As can be inferred from **Figure 7** and as it was measured by the frequency domain PSS results, the signals show $1.05\ \text{V}$ oscillation amplitude level with an amplitude difference lower than $10\ \text{mV}$, whereas the quadrature phase error is lower than $0.1\ \text{deg}$.

In **Figure 8** the transient PSS results of the phase relation between the $Q+$ voltage driving the PG injecting current in tank node is reported. The phase displacement of driver current is calculated as $103.157\ \text{ps} \cdot 2.442\ \text{GHz} \cdot 360\ \text{deg} = 90.68\ \text{deg}$. The quadrature error is lower than $1\ \text{deg}$. However this phase relation is not directly related to the overall quadrature phase error between the tank node voltages signals, since the receiving resonant tank undergoes to a pulling due to the whole current pulse rather than to the position of the peak only. This phenomenon results in an attenuation of the quadrature error of about an order of magnitude in phase degree, allowing the phase error between voltage signals to be lower than $0.1\ \text{deg}$.

The phase noise results are presented in **Figure 9** for VCOs running at $2.45\ \text{GHz}$ at nominal temperature of $T = 27^{\circ}\text{C}$.

As expected from a pulsed bias architecture the phase noise improvement is consistent especially at low offsets. However, to avoid bias dependence on results, we set the comparison at $1\ \text{MHz}$ where white noise contributors dominate. The improvement is measured in $5.6\ \text{dBc/Hz}$. At lower offsets the phase noise improvement can be higher than $20\ \text{dBc/Hz}$. This can be explained considering that in the reference oscillator, in order to achieve the quadrature coupling on relative phases between resonators I and Q, the M_{COU} transistors inject a not negligible charge quantity in the oscillation portion more sensitive to phase variations. At offsets higher than $100\ \text{MHz}$ the phase noise improvement drops, however we remark such high frequency offsets are not of concern for any of actual phase noise masks in ISM modulations. For a complete comparison we need to evaluate power consumption, calculated with P_{DC} as the product of $1.8\ \text{V}$ supply voltage and the total DC current calculated by PSS analysis. Reference oscillator dissipates $48.5\ \text{mW}$ whereas the PQPBO reaches $71.5\ \text{mW}$ subdivided in $47.5\ \text{mW}$ and $24\ \text{mW}$ for driver and buffer transistors, respectively. Such high efficiency is explained by the operation in C-class of the PQPBO.

$$FOM = L(\Delta\omega) - 20\log_{10}\left(\frac{\omega_0}{\Delta\omega}\right) + 10\log_{10}\left(\frac{P_{DC}}{1\ \text{mW}}\right) \tag{12}$$

According to Figure of Merit in Equation (12), phase noise $L(\Delta\omega)$ is evaluated at $\omega_0/2\pi = 2.45\ \text{GHz}$ with $\Delta\omega/2\pi = 1\ \text{GHz}$ obtaining $FOM = -185.1\ \text{dB}$ for the reference oscillator and $FOM = -189.1\ \text{dB}$ for the PBO. We conclude that a FOM increment of $4\ \text{dB}$ is effectively observed at an offset frequency where white noise source dominate. The FOM increment increases for lower offsets. Finally, the area of every delay line is $111\ \mu\text{m} \times 131\ \mu\text{m}$ and the total area of the two inductors is $800\ \mu\text{m} \times 400\ \mu\text{m}$. Thus the four microstrips area occupation represents only the 18% of the inductors area.

In the second comparison we gather a list of recently proposed phase and quadrature VCO architectures with both coupling based on active devices and on passive components. The results are reported in **Table 1**, showing that the proposed PQPBO may reach a state-of-the-art FOM with a very reduced quadrature error.

5. Concluding Remarks

In this paper a PQPBO based on a novel coupling method has been proposed. The coupling method adopts a delay-line implementation with an extremely compact meander microstrip structure. The design equations for the PQPBO, with a dedicated section on the DL optimization, have been pursued. The PQPBO has been implemented

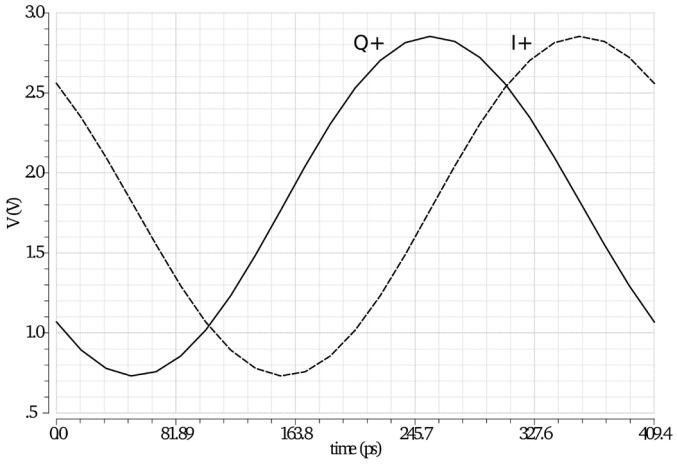

Figure 7. PSS transient result of $I+$ and $Q+$ nodes voltage.

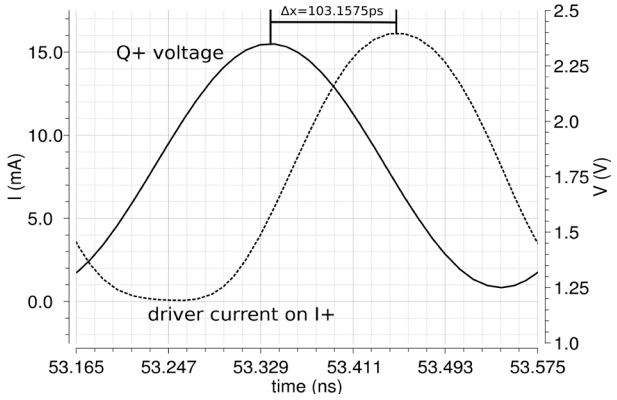

Figure 8. PSS transient result of $Q+$ voltage (continuous line) driving the PG injecting current (dotted line) in tank node $I+$.

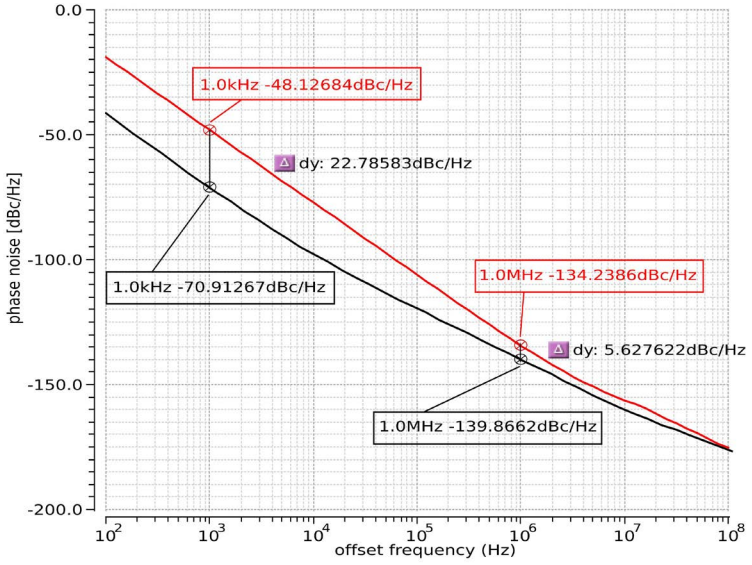

Figure 9. Phase noise results for the PQPBO (black trace) and for the reference oscillator (red trace).

Table 1. Comparison with literature phase and quadrature VCOs.

Reference	[9]	[10]	[11]	[12]	[13]	This Work
$L(\Delta\omega)$ *average* [dBc/Hz]	−115 @1MHz	−129.5 @1MHz	−125 @1MHz	−111 @1MHz	−134.8 @1MHz	−139.9 @1MHz
Freq. Range [GHz]	5.0 - 5.7	2.4 - 2.6	4.9 - 5.5	6.9 - 7.3	1.8 - 2.2	2.4 - 2.5
Process [nm]	180	180	250	180	180	150
FOM [dB]	−177.0	−189.0	−185.9	−184.6	−185.4	−189.1
Quadrature Error [deg˚]	0.36	<1	2.6	2	≥0.7	<0.1
Measured/ Simulated	M	S	M	M	S	S

at LVS level in a LFoundry 150 nm RF CMOS technology with a tuning frequency range spanning the $2.4-2.5$ GHz showing a state-of-the-art *FOM* compared to recent literature phase and quadrature VCOs with a very reduced quadrature error. These promising results encourage further optimization of the proposed architecture and an effective on-chip realization.

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