2017 Symposia on VLSI Technology and Circuits June 5th (Monday)

Time	Suzaku III	Suzaku II	Suzaku I	Shunju III	Shunju II	Shunju I
7:30-18:00	Registration (Technology and Circuits)					
8:30-10:10	Demo Setup	**2017 Symposium on VLSI Circuits Short Course 2** **Integrated Circuits for Smart Connected Cars and Automated Driving** **8:30 Brief Outline,** Short Course Chair **8:35 An Overview of Automotive Electronics,** C. Lang, Bosch USA **9:25 Intra-Vehicle Wireline Networks,** A. Klaus, Marvell Semiconductor	**2017 Symposium on VLSI Circuits Short Course 1** **Machine Learning for Circuit Designers** **8:30 Brief Outline,** Short Course Chair **8:35 Machine Learning Basics and Its Applications to Internet-of-Things,** H. Maruyama, Preferred Networks **9:25 Machine-Learning-Enabled Design Space for Energy-Efficient Mixed-Signal Inference Systems**, N. Verma, Princeton Univ.	**2017 Symposium on VLSI Technology Short Course** **Technology Enablers for 5nm and Next Wave of Integration** **8:30 Introduction** **8:35 CMOS Device Technology Enablers and Challenges for 5nm Node,** P. Hashemi and T. B. Hook, IBM Research **9:25 Heterogeneous Integration of Ge, III-V, and 2D on Si – from More Moore to Beyond CMOS –,** M. Takenaka, The Univ. of Tokyo		
10:30-12:10		**10:15 Break** **10:35 Image Sensors for Automotive Applications,** S. Kawahito, Shizuoka Univ. **11:25 LIDAR System Design for Automotive Applications,** E. Bartolome, Texas Instruments	**10:15 Break** **10:35 Designing Efficient Deep Learning Accelerators: Challenges and Opportunities,** J. Emer, Massachusetts Institute of Technology / nVidia **11:25 Advanced Techniques for High-Speed Deep Learning on Large-Scale Neural Network in the Cloud,** Y. Tomita, Fujitsu Laboratories Ltd.	**10:15 Break** **10:35 Design & Technology Co-Optimization for High Performance SoC,** P. Penzes, Qualcomm Technologies, Inc. **11:25 The Duality of Interconnect Scaling in Sub-10nm Technology Nodes: Increasingly Complex, Increasingly Important,** R. Fox, GLOBALFOUNDRIES		8:30-17:40 2017 Silicon Nanoelectronics Workshop (Day 2)
12:10-13:30		**12:15 Lunch**	**12:15 Lunch**	**12:15 Lunch**		
13:30-16:00		**13:30 Automotive Sensors and Interfaces,** B. Clark, Analog Devices, Inc. **14:20 Key Technologies That Support EV Motor Control,** S. Otani, Renesas Electronics Corp. **15:10 Break** **15:30 Autonomous Vehicles Platform: Processor/Software Architecture, Machine Learning and Security,** J. Weast, Intel Corp.	**13:30 Deep Learning for Mobile and Embedded Devices,** M. Aleksic, Qualcomm Inc. **14:20 Vision-Centric Devices at the Network Edge Using Deep-Networks and Computer Vision,** D. Moloney, Intel Corp. / Movidius **15:10 Break** **15:30 Mobile/Embedded DNN and AI SoCs,** H.-J. Yoo, KAIST	**13:30 Heterogeneous 3D/2.5D Integration toward IoT and AI Era,** M. Koyanagi, Tohoku Univ. **14:20 Device Challenges for Scaled Analog-RF,** F.-L. Hsueh, Y.-C. Peng, J.-J. Horng, W.-C. Chen, S. Yang, H. Liu, B. Yang, V. Chou, A. Kundu, C.-T. Lu, M.-C. Chuang, C.-H. Chen, H.-H. Hsieh, C.-H. Chang, Y.-W. Chen, L.-C.Cho, J. Fu and J. Tsai, TSMC **15:10 Break** **15:30 Embedded Memory Design - Memories Differentiate Microcontoller Solutions –,** T. Jew, NXP Semiconductors		
16:00-17:10	Demo Setup			**16:20 On Die Processing in Memory – PIM on DRAM –,** F. Devaux, uPmem		
17:30-22:10	17:30-19:30 Demo Session & Reception					19:00-22:10?? 2017 Spintronics Workshop on LSI

2017 Silicon Nanoelectronics Workshop (Day 1): June 4th (Sunday) 8:30-18:40 / Shunju I (for session) and Shunju II (for posters)

2017 Symposium on VLSI Techonlogy / Circuits June 9th (Friday)

Time	Suzaku I, II, III
9:00-12:00	**International Forum on Singularity: Exponential X** **(Friday Forum)** **09:00 Welcome to Exponential X,** K. Yano, Hitachi **Session 1. Exponential Technology** **09:15 Exponential Neuromorphic Systems for Singularity,** V. De, Intel **09:45 Exponential Computing for Singularity,** M. Saito, PEZY **10:15 Exponential Connectivity for Singularity,** A. Amerasekera, UCB/BWRC **10:45 Exponential Commerce for Singularity,** T. Kitagawa, Rakuten **11:15** Panel **"Where will the Next Exponential Technology Arise?"**
12:00-13:30	**12:00 Lunch Time**
13:30-16:30	**Session 2. Exponential Humans** **13:30 Exponential Intelligence for Singularity,** K. Ataka, Yahoo **14:00 Exponential Healthcare for Singularity,** Y. Ishikawa **14:30 Exponential Mind for Singularity,** J. Tani, KAIST **15:00 Exponential Robotics for Singularity,** K. Kanaoka, Ritsumeikan Univ. **15:30 Break** **15:45** Panel **"How will Human Beings Change in the Future?"**

2017 Symposia on VLSI Technology and Circuits June 6th (Tuesday)

7:00-17:00 Registration (Technology and Circuits)

8:00-10:05 / 10:30-12:30

T1 "Welcome and Plenary Session"

T1-1	8:00-8:45
	Welcome and Opening Remarks
T1-2	**8:45-9:25 (Plenary)**
SoftBank	5G and It's Surrounding Situations until 2020
T1-3	**9:25-10:05 (Plenary)**
NXP Semiconductors	Privacy and Security: Key Requirements for Sustainable IoT Growth

C1 "Welcome and Plenary Session"

C1-1	10:30-10:50
	Welcome and Opening Remarks
C1-2	**10:50-11:40 (Plenary)**
Panasonic	Innovative Solutions toward Future Society whth AI, Robotics, and IoT
C1-3	**11:40-12:30 (Plenary)**
Waymo	Inside Waymo's Self-Driving Car: My Favorite Transistors

12:30-14:00

14:00-15:40

C2: Machine / Deep Learning

C2-1	14:00-14:25	
Hokkaido Univ.	BRein Memory: A 13-Layer 4.2 K Neuron/0.8 M Synapse Binary/Ternary Reconfigurable In-Memory Deep Neural Network Accelerator in 65 nm CMOS	
C2-2	14:25-14:50	
Tsinghua Univ.	A 1.06-To-5.09 TOPS/W Reconfigurable Hybrid-Neural-Network Processor for Deep Learning Applications	
C2-3	14:50-15:15	
Princeton Univ.	A Heterogeneous Microprocessor for Energy-Scalable Sensor Inference Using Genetic Programming	
C2-4	15:15-15:40	
Univ. of Michigan	A 3.43TOPS/W 48.9pJ/Pixel 50.1nJ/Classification 512 Analog Neuron Sparse Coding Neural Network with On-Chip Learning and Classification in 40nm CMOS	

C3: Delta-Sigma Modulators

C3-1	14:00-14:25	
KAIST	A 4.2mW 10MHz BW 74.4dB SNDR Fourth-Order CT DSM with Second-Order Digital Noise Coupling Utilizing an 8b SAR ADC	
C3-2	14:25-14:50	
The Univ. of Texas at Austin	A 0.028mm^2 19.8fJ/step 2nd-Order VCO-Based CT ΔΣ Modulator Using an Inherent Passive Integrator and Capacitive Feedback in 40nm CMOS	
C3-3	14:50-15:15	
Univ. of Michigan	A 5GS/s 156MHz BW 70dB DR Continuous-Time Sigma-Delta Modulator with Time-Interleaved Reference Data-Weighted Averaging	
C3-4	15:15-15:40	
Yonsei Univ.	A 55μW 93.1dB-DR 20kHz-BW Single-Bit CT Δ Σ Modulator with Negative R-Assisted Integrator Achieving 178.7dB FoM in 65nm CMOS	

C4: Biomedical Circuits and Systems

C4-1	14:00-14:25	
National Chiao Tung Univ.	A Fully Integrated Closed-Loop Neuromodulation SoC with Wireless Power and Bi-Directional Data Telemetry for Real-Time Human Epileptic Seizure Control	
C4-2	14:25-14:50	
National Chiao Tung Univ.	A Bone-Guided Cochlear Implant CMOS Microsystem Preserving Acoustic Hearing	
C4-3	14:50-15:15	
Cortera Neurotechnologies	An Implantable 700μW 64-Channel Neuromodulation IC for Simultaneous Recording and Stimulation with Rapid Artifact Recovery	
C4-4	15:15-15:40	
imec	Intraneural Active Probe for Bidirectional Peripheral Nerve Interface	

T2: (FS) Nonvolatile & Embedded Memory

T2-1	14:00-14:25 **(Invited)**
KU Leuven and imec	Memory Technology for the Terabit Era: from 2D to 3D
T2-2	14:25-14:50 **(Invited)**
TSMC	Embedded Memories for Mobile, IoT, Automotive and High Performance Computing
T2-3	14:50-15:15
NEC	A Low-Power Cu Atom Switch Programmable Logic Fabricated in a 40nm-Node CMOS Technology
T2-4	15:15-15:40
Sony Semiconductor Solutions	A Cross Point Cu-ReRAM with a Novel OTS Selector for Storage Class Memory Applications

T3: III-V

T3-1	14:00-14:25
Lund Univ.	Record Performance for Junctionless Transistors in InGaAs MOSFETs
T3-2	14:25-14:50
Lund Univ.	Vertical Heterojunction InAs/InGaAs Nanowire MOSFETs on Si with I_{on} = 330 μA/μm at I_{off} = 100 nA/μm and V_D = 0.5V
T3-3	14:50-15:15
imec	First Demonstration of ~3500 cm^2/V-s Electron Mobility *and* Sufficient BTI Reliability (Max V_{ov} Up to 0.6V) $In_{0.53}Ga_{0.47}As$ nFET Using an IL/$LaSiO_x$/HfO_2 Gate Stack
T3-4	15:15-15:40
IBM T. J. Watson Research Center	High Performance and Low Leakage Current InGaAs-on-Silicon FinFETs with 20 nm Gate Length

16:00-18:05

C5: Application Specific I/Os

C5-1	16:00-16:25	
IBM Research	A 5Gb/s 7.1fJ/b/mm 8× Multi-Drop On-Chip 10mm Data Link in 14nm FinFET CMOS SOI at 0.5V	
C5-2	16:25-16:50	
Univ. of Minnesota	A 10Gb/s 10mm On-Chip Serial Link in 65nm CMOS Featuring a Half-Rate Time-Based Decision Feedback Equalizer	
C5-3	16:50-17:15	
POSTECH	An FFE TX with 3.8x Eye Improvement by Automatic Impedance Adaptation for Universal Compatibility with Arbitrary Channel and RX Impedances	
C5-4	17:15-17:40	
Univ. of California, Los Angeles	A Distance-Immune Low-Power 4-Mbps Inductively-Coupled Bidirectional Data Link	
C5-5	17:40-18:05	
POSTECH	A 16.6-pJ/b 150-Mb/s Body Channel Communication Transceiver with Decision Feedback Equalization Improving >200% Area Efficiency	

C6: (CFS) Ultra-Low Power Wireless Transceivers for IoT Systems

C6-1	16:00-16:25 **(Invited)**	
Texas Instruments	Reaching 10-Years of Battery Life for Industrial IoT Wireless Sensor Networks	
C6-2	16:25-16:50	
Univ. of Michigan	A 1.7nW PLL-Assisted Current Injected 32KHz Crystal Oscillator for IoT	
C6-3	16:50-17:15	
KAIST	A 2.4GHz, -102dBm-Sensitivity, 25kb/s, 0.466mW Interference Resistant BFSK Multi-Channel Sliding-IF ULP Receiver	
C6-4	17:15-17:40	
TSMC	A 16 nm FinFET 0.4 V Inductor-Less Cellular Receiver Front-End with 10 mW Ultra-Low Power and 0.31 mm^2 Ultra-Small Area for 5G System in Sub-6 GHz Band	
C6-5	17:40-18:05 **(Invited)**	
Broadcom	A Multi-Mode WPAN (Bluetooth, BLE, IEEE 802.15.4) SoC for Low-Power and IoT Applications	

C7: Sensor Readout Circuits

C7-1	16:00-16:25	
Delft Univ. of Technology	A Compact Sensor Readout Circuit with Combined Temperature, Capacitance and Voltage Sensing Functionality	
C7-2	16:25-16:50	
Delft Univ. of Technology	A 9.1 mW Inductive Displacement-to-Digital Converter with 1.85 nm Resolution	
C7-3	16:50-17:15	
Delft Univ. of Technology	A CMOS Temperature Sensor with a 49fJ·K^2 Resolution FoM	
C7-4	17:15-17:40	
National Taiwan Univ.	A 0.06mm^2 ± 50mV Range -82dB THD Chopper VCO-Based Sensor Readout Circuit in 40nm CMOS	

T4: (FS) 1D and 2D Atomic Thin Materials and Devices

T4-1	16:00-16:25 **(Invited)**
Duke Univ.	Scaling, Stacking, and Printing: How 1D and 2D Nanomaterials still Hold Promise for a New Era of Electronics
T4-2	16:25-16:50 **(Invited)**
Fujitsu Laboratories	One and Two Dimensional Nanocarbon Materials for Innovative Functional Devices
T4-3	16:50-17:15
Purdue Univ.	Experimental Demonstration of Electrically-Tunable Bandgap on 2D Black Phosphorus by Quantum Confined Stark Effect
T4-4	17:15-17:40
The Univ. of Tokyo	Statistical Analyses of Random Telegraph Noise Amplitude in Ultra-Narrow (Deep Sub-10nm) Silicon Nanowire Transistors

T5: Hetero Integration

T5-1	16:00-16:25
TSMC	Wafer Level Integration of an Advanced Logic-Memory System Through 2nd Generation CoWoS® Technology
T5-2	16:25-16:50
National Univ. of Singapore	Enabling Low Power and High Speed OEICs: First Monolithic Integration of InGaAs n-FETs and Lasers on Si Substrate
T5-3	16:50-17:15
Osaka Univ	Enhancement-Mode N-Channel TFT and Room-Temperature Near-Infrared Emission Based on n$^+$/p Junction in Single-Crystalline GeSn on Transparent Substrate
T5-4	17:15-17:40
National Chiao Tung Univ.	High V_{th} Enhancement Mode GaN Power Devices with High $I_{D,max}$ Using Hybrid Ferroelectric Charge Trap Gate Stack

18:15-19:30

IEEE SSCS Young Professional Mentoring Event

19:30-20:00

19:30-20:00
Symposium on VLSI Circuits
30th Anniversary Celebration

20:00-21:30

20:00-21:30 Circuits Evening Panel Discussion
The Most Important Circuits of 2037

20:00-21:30 Joint Evening Panel Discussion
How will We Survive the Post-Scaling Era?

20:00-21:30 Technology Evening Panel Discussion
Transistor Future; How Does It Evolve after FinFET Era?

2017 Symposia on VLSI Technology and Circuits June 7th (Wednesday)

Time	Suzaku III	Suzaku II	Suzaku I	Shunju III	Shunju II	Shunju I
7:30-17:00	**Registration (Technology and Circuits)**					
8:30-10:10		**C8: Pipelined ADCs**	**C9: Sensors for Biomedical Applications**	**T6: Highlight**		
		C8-1 8:30-8:55	C9-1 8:30-8:55	T6-1 8:30-8:55		
		imec — A 16nm 69dB SNDR 300MSps ADC with Capacitive Reference Stabilization	Arizona State Univ. — A 1.06 µW Smart ECG Processor in 65 nm CMOS for Real-Time Biometric Authentication and Personal Cardiac Monitoring	Samsung Electronics — Highly Manufacturable 7nm FinFET Technology Featuring EUV Lithography for Low Power and High Performance Applications		
		C8-2 8:55-9:20	C9-2 8:55-9:20	T6-2 8:55-9:20		
		KAIST — A 9.1 ENOB 21.7fJ/conversion-step 10b 500MS/s Single-Channel Pipelined SAR ADC with a Current-Mode Fine ADC in 28nm CMOS	Stanford Univ. — A High-Precision 36 mm^3 Programmable Implantable Pressure Sensor with Fully Ultrasonic Power-Up and Data Link	Qualcomm Technologies — 10nm High Performance Mobile SoC Design and Technology Co-Developed for Performance, Power, and Area Scaling		
		C8-3 9:20-9:45	C9-3 9:20-9:45	T6-3 9:20-9:45		
		Vrije Universitei t Brussel — A Single-Channel, 600Msps, 12bit, Ringamp-Based Pipelined ADC in 28nm CMOS	Univ. of California, Berkeley — Chip-Scale Fluorescence Imager for *In Vivo* Microscopic Cancer Detection	National Chiao Tung Univ. — First Demonstration of Flash RRAM on Pure CMOS Logic 14nm FinFET Platform Featuring Excellent Immunity to Sneak-Path and MLC Capability		
		C8-4 9:45-10:10	C9-4 9:45-10:10	T6-4 9:45-10:10		
		Univ. of Michigan — A Calibration-Free 2.3 mW 73.2 dB SNDR 15b 100 MS/s Four-Stage Fully Differential Ring Amplifier Based SAR-Assisted Pipeline ADC	California Institute of Technology — A 4µW, ADPLL-Based Implantable Amperometric Biosensor in 65nm CMOS	IBM Research — First Demonstration of 3D SRAM Through 3D Monolithic Integration of InGaAs n-FinFETs on FDSOI Si CMOS with Inter-Layer Contacts		
10:30-12:35	**JFS1: Emerging Reliability Solutions**	**C10: Frequency Generation**	**C11: Analog Techniques**	**T7: Memory 1 PCM ReRAM**		**T8: Sensing**
	JFS1-1 10:30-10:55	C10-1 10:30-10:55	C11-1 10:30-10:55	T7-1 10:30-10:55		T8-1 10:30-10:55
	Fujitsu Laboratories — An Adaptive Clocking Control Circuit with 7.5% Frequency Gain for SPARC Processors	Tokyo Institute of Technology — A Pulse-Tail-Feedback VCO Achieving FoM of 195dBc/Hz with Flicker Noise Corner of 700Hz	Broadcom — A Capacitively-Degenerated 100dB Linear 20-150MS/s Dynamic Amplifier	Univ. of Tsukuba — Reduction of Cycle-to-Cycle Variability in ReRAM by Filamentary Refresh		National Chiao Tung Univ. — Towards A Fully Integrated, Wirelessly Powered, and Ordinarily Equipped On-Lens System for Successive Dry Eye Syndrome Diagnosis
	JFS1-2 10:55-11:20	C10-2 10:55-11:20	C11-2 10:55-11:20	T7-2 10:55-11:20		T8-2 10:55-11:20
	Univ. of Minnesota — Statistical Characterization of Radiation-Induced Pulse Waveforms and Flip-Flop Soft Errors in 14nm Tri-Gate CMOS Using a Back-Sampling Chain (BSC) Technique	Renesas System Design — A 3.2ppm/°C Second-Order Temperature Compensated CMOS On-Chip Oscillator Using Voltage Ratio Adjusting Technique	KAIST — A Hybrid Power Amplifier Using 3-Phase 3-Level Class-D with 200nH Inductors and Current Balancing Technique	imec — Thermally Stable Integrated Se-Based OTS Selectors with >20 MA/cm^2 Current Drive, >3.10^3 Half-Bias Nonlinearity, Tunable Threshold Voltage and Excellent Endurance		Univ. of Minnesota — A Powerless and Non-Volatile Counterfeit IC Detection Sensor in a Standard Logic Process Based on an Exposed Floating-Gate Array
	JFS1-3 11:20-11:45	C10-3 11:20-11:45	C11-3 11:20-11:45	T7-3 11:20-11:45		T8-3 11:20-11:45
	Intel — F_{MAX} / V_{MIN} and Noise Margin Impacts of Aging on Domino Read, Static Write, and Retention of 8T 1R1W SRAM Arrays in 22nm High-k/Metal-Gate Tri-Gate CMOS	Samsung Electronics — An 8GHz, 0.005mm^2 All Digital Clock Generator Having 0.1% Frequency Accuracy by New ZTC Algorithm	The Univ. of Texas at Austin — A 1V 0.25uW Inverter-Stacking Amplifier with 1.07 Noise Efficiency Factor	CEA-LETI — Innovative PCM+OTS Device with High Sub-Threshold Non-Linearity for Non-Switching Reading Operations and Higher Endurance Performance		Samsung Electronics — An All Pixel PDAF CMOS Image Sensor with 0.64µm×1.28 µm Photodiode Separated by Self-Aligned In-Pixel Deep Trench Isolation for High AF Performance
	JFS1-4 11:45-12:10	C10-4 11:45-12:10	C11-4 11:45-12:10	T7-4 11:45-12:10		T8-4 11:45-12:10
	National Tsing Hua Univ. — Excellent Reliability of Ferroelectric $HfZrO_x$ Free from Wake-Up and Fatigue Effects by NH_3 Plasma Treatment	TSMC — A 4GHz Clock Distribution Architecture Using Subharmonically Injection-Locked Coupled Oscillators with Clock Skew Calibration in 16nm CMOS	Univ. of Toronto — A 150-µW 3rd-Order Butterworth Passive-Switched-Capacitor Filter with 92 dB SFDR	Samsung Electronics — A Novel Write Method for Improving RESET Distribution of PRAM		Hitachi — FET-Type Hydrogen Sensor with Short Response Time and High Drift Immunity
	JFS1-5 12:10-12:35	C10-5 12:10-12:35	C11-5 12:10-12:35			
	The Univ. of Texas at Dallas — A 10MHz 5-to-40V EMI-Regulated GaN Power Driver with Closed-Loop Adaptive Miller Plateau Sensing	National Taiwan Univ. — A 5.12-GHz Fractional-*N* Frequency Synthesizer with an LC-VCO-Based MDLL	KAIST — A 0.8V, 37nW, 42ppm/°C Sub-Bandgap Voltage Reference with PSRR of -81dB and Line Sensitivity of 51ppm/V in 0.18um CMOS			
12:35-14:00						
14:00-15:40	**JFS2: Advanced Assembly**	**C12: SRAM & Emerging Memory**	**C13: Biosignal Recording / Monitoring Circuits**	**T9: SiGe/Ge FET 1**		**T10: Reliability**
	JFS2-1 14:00-14:25	C12-1 14:00-14:25	C13-1 14:00-14:25	T9-1 14:00-14:25		T10-1 14:00-14:25
	Intel — A Digitally Controlled Fully Integrated Voltage Regulator with 3D-TSV Based On-Die Solenoid Inductor with Backside Planar Magnetic Core in 14nm Tri-Gate CMOS	KAIST — A 31.2pJ/disparity·pixel Stereo Matching Processor with Stereo SRAM for Mobile UI Application	Univ. of Michigan — 3.37 µW/Ch Modular Scalable Neural Recording System with Embedded Lossless Compression for Dynamic Power Reduction	IBM Research — High Performance and Record Subthreshold Swing Demonstration in Scaled RMG SiGe FinFETs with High-Ge-Content Channels Formed by 3D Condensation and a Novel Gate Stack Process		TSMC — On-Die 16nm Metal Critical Peak Current Test Methodology with 100ps Pulse Width
	JFS2-2 14:25-14:50	C12-2 14:25-14:50	C13-2 14:25-14:50	T9-2 14:25-14:50		T10-2 14:25-14:50
	Keio Univ. — A 6Gb/s Rotatable Non-Contact Connector with High-Speed/I^2C/CAN/SPI Interface Bridge IC	Univ. of Michigan — A 0.3V VDDmin 4+2T SRAM for Searching and In-Memory Computing Using 55nm DDC Technology	imec/Holst Centre — A 36µW Reconfigurable Analog Front-End IC for Multimodal Vital Signs Monitoring	IBM Research — SiGe FinFET for Practical Logic Libraries by Mitigating Local Layout Effect		KU Leuven — A Fully-Integrated Method for RTN Parameter Extraction
	JFS2-3 14:50-15:15	C12-3 14:50-15:15	C13-3 14:50-15:15	T9-3 14:50-15:15		T10-3 14:50-15:15
	TSMC — High Density 3D Fanout Package for Heterogeneous Integration	Semiconductor Energy Laboratory — A 140 MHz 1 Mbit 2T1C Gain-Cell Memory with 60-nm Indium–Gallium–Zinc Oxide Transistor Embedded Into 65-nm CMOS Logic Process Technology	Univ. of Washington — A Scalable, Highly-Multiplexed Delta-Encoded Digital Feedback ECoG Recording Amplifier with Common and Differential-Mode Artifact Suppression	The Univ. of Tokyo — High Performance 4.5-nm-Thick Compressively-Strained Ge-On-Insulator pMOSFETs Fabricated by Ge Condensation with Optimized Temperature Control		CEA-LETI — New Insight on the Geometry Dependence of BTI in 3D Technologies Based on Experiments and Modeling
	JFS2-4 15:15-15:40	C12-4 15:15-15:40	C13-4 15:15-15:40	T9-4 15:15-15:40		T10-4 15:15-15:40
	KAIST — A Shutter-Less Micro-Bolometer Thermal Imaging System Using Multiple Digital Correlated Double Sampling for Mobile Applications	National Tsing Hua Univ. — Embedded 2Mb ReRAM Macro with 2.6ns Read Access Time Using Dynamic-Trip-Point-Mismatch Sampling Current-Mode Sense Amplifier for IoE Applications	imec/Holst Centre — A Bio-Impedance Readout IC with Frequency Sweeping from 1k-to-1MHz for Electrical Impedance Tomography	IBM Research — Understanding the Interfacial Layer Formation on Strained $Si_{1-x}Ge_x$ Channels and Their Correlation to Inversion Layer Hole Mobility		Peking Univ. — Unified Self-Heating Effect Model for Advanced Digital and Analog Technology and Thermal-Aware Lifetime Prediction Methodology
16:00-18:05	**C14: Phase-Locked Loops**	**C15: Memory Interface and Flash Memory**	**C16: Power Management Circuit**	**T11: CMOS Integration I**		**T12: Ferroelectric**
	C14-1 16:00-16:25	C15-1 16:00-16:25	C16-1 16:00-16:25	T11-1 16:00-16:25		T12-1 16:00-16:25
	TSMC — A 0.5V 1.6mW 2.4GHz Fractional-N All-Digital PLL for Bluetooth LE with PVT-Insensitive TDC Using Switched-Capacitor Doubler in 28nm CMOS	SK hynix — A Floating Tap Termination Scheme with Inverted DBI AC and Floating Tap Forcing Technique for High-Speed Low-Power Signaling	KAIST — A 1452-% Power Extraction Improvement Energy Harvesting Circuit with Simultaneous Energy Extraction from a Piezoelectric Transducer and A Thermoelectric Generator	GLOBALFOUNDRIES — 14nm FinFET Technology for Analog and RF Applications		National Nano Device Laboratories — Nano-Scaled Ge FinFETs with Low Temperature Ferroelectric $HfZrO_x$ on Specific Interfacial Layers Exhibiting 65% S.S. Reduction and Improved I_{ON}
	C14-2 16:25-16:50	C15-2 16:25-16:50	C16-2 16:25-16:50	T11-2 16:25-16:50		T12-2 16:25-16:50
	KAIST — A Supply Noise Insensitive PLL with a Rail-To-Rail Swing Ring Oscillator and a Wideband Noise Suppression Loop	TSMC — A Resistor-Free 4.266 Gbps LPDDR4 I/O in 10 nm FinFET CMOS Technology	Seoul National Univ. — A 20nW-to-140mW Input Power Range, 94% Peak Efficiency Energy-Harvesting Battery Charger with Frequency-Sweeping Input Voltage Monitor and Optimal On-Time Generator	Samsung Electronics — High Performance 14nm FinFET Technology for Low Power Mobile RF Application		Univ. of Notre Dame — Impact of Total and Partial Dipole Switching on the Switching Slope of Gate-Last Negative Capacitance FETs with Ferroelectric Hafnium Zirconium Oxide Gate Stack
	C14-3 16:50-17:15	C15-3 16:50-17:15	C16-3 16:50-17:15	T11-3 16:50-17:15		T12-3 16:50-17:15
	Xilinx — A 164fs_{rms} 9-to-18GHz Sampling Phase Detector Based PLL with In-Band Noise Suppression and Robust Frequency Acquisition in 16nm FinFET	Samsung Electronics — A 1.2V 1.33Gb/s/pin 8Tb NAND Flash Memory Multi-Chip Package Employing F-Chip for Low Power and High Performance Storage Applications	Korea Univ. — A 42nJ/Conversion On-Demand State-of-Charge Indicator for Miniature IoT Li-Ion Batteries	Samsung Electronics — 10nm 2nd Generation BEOL Technology with Optimized Illumination and LELELELE		The Univ. of Tokyo — A Nonvolatile SRAM Integrated with Ferroelectric HfO_2 Capacitor for Normally-Off and Ultralow Power IoT Application
	C14-4 17:15-17:40	C15-4 17:15-17:40	C16-4 17:15-17:40	T11-4 17:15-17:40		T12-4 17:15-17:40
	Univ. of Washington — Computational Locking: Accelerating Lock-Times in All-Digital PLLs	Univ. of Michigan — An Ultra-Wide Program, 122pJ/Bit Flash Memory Using Charge Recycling	Northwestern Univ. — A 0.3-0.86V Fully Integrated Buck Regulator with 2GHz Resonant Switching for Ultra-Low Power Applications	UNIST — Trantenna: Monolithic Transistor-Antenna Device for Real-Time THz Imaging System		KU Leuven — First Demonstration of Vertically Stacked Ferroelectric Al Doped HfO_2 Devices for NAND Applications
	C14-5 17:40-18:05	C15-5 17:40-18:05	C16-5 17:40-18:05	T11-5 17:40-18:05 (Late News)		
	UNIST — A −242-dB FOM and −71-dBc Reference Spur Ring-VCO-Based Ultra-Low-Jitter Switched-Loop-Filter PLL Using a Fast Phase-Error Correction Technique	TSMC — A 40nm Split Gate Embedded Flash Macro with Flexible 2-in-1 Architecture, Code Memory with 140MHz Read Speed and Data Memory with 1M Cycles Endurance	KU Leuven — A True Two-Quadrant Fully Integrated Switched Capacitor DC-DC Converter Supporting Vertically Stacked DVS-Loads with up to 99.6% Efficiency	IBM Research — Comparison of Key Fine-Line BEOL Metallization Schemes for Beyond 7 nm Node		
19:00-21:00				**19:00-21:00 Joint Banquet**		

2017 Symposia on VLSI Technology and Circuits June 8th (Thursday)

Time	Suzaku III	Suzaku II	Suzaku I	Shunju III	Shunju II	Shunju I
8:00-17:00	**Registration (Technology and Circuits)**					
8:30-10:10	**C17: Video Processing**	**C18: SAR ADCs**	**C19: Image Sensors**	**JFS3: Ultra Low Power for IoT**		**T13: Quantum Neuromorphic Computing**
	C17-1 8:30-8:55 **(Invited)**	C18-1 8:30-8:55	C19-1 8:30-8:55	JFS3-1 8:30-8:55 **(Invited)**		T13-1 8:30-8:55
	Socionext: System Architecture with Single Chip 8K HEVC Decoder for 8K Advanced BS Receiver System	MediaTek: A 2.4-mW 25-MHz BW 300-MS/s Passive Noise Shaping SAR ADC with Noise Quantizer Technique in 14-nm CMOS	Sony Semiconductor Solutions: A 4.1Mpix 280fps Stacked CMOS Image Sensor with Array-Parallel ADC Architecture for Region Control	DENSO: Computing Platform for Automotive Electronics of Automated Driving Generation		CEA-LETI: Towards Quantum Computing in Si MOS Technology: Single-Shot Readout of Spin States in a FDSOI Split-Gate Device with Built-In Charge Detector
	C17-2 8:55-9:20	C18-2 8:55-9:20	C19-2 8:55-9:20	JFS3-2 8:55-9:20 **(Invited)**		T13-2 8:55-9:20
	Univ. of Michigan: A 127mW 1.63TOPS Sparse Spatio-Temporal Cognitive SoC for Action Classification and Motion Tracking in Videos	The Univ. of Texas at Austin: A 13b-ENOB 173dB-FoM 2nd -Order NS SAR ADC with Passive Integrators	CEA-LETI: A 256 Energy Bin Spectrum X-Ray Photon-Counting Image Sensor Providing 8Mcounts/s/pixel and On-Chip Charge Sharing, Charge Induction and Pile-Up Corrections	GLOBALFOUNDRIES: Semiconductor Platforms for Ultra Low Power IoT Solutions		Sandia National Laboratories: Achieving Ideal Accuracies in Analog Neuromorphic Computing Using Periodic Carry
	C17-3 9:20-9:45	C18-3 9:20-9:45	C19-3 9:20-9:45	JFS3-3 9:20-9:45		T13-3 9:20-9:45
	EPFL: A Single-Chip 2048×1080 Resolution 32fps 380mW Trinocular Disparity Estimation Processor in 28nm CMOS Technology	National Taiwan Univ.: A 510nW 12-bit 200kS/s SAR-Assisted SAR ADC Using a Re-Switching Technique	Shizuoka Univ.: A 0.61 E- Noise Global Shutter CMOS Image Sensor with Two-Stage Charge Transfer Pixels	United Microelectronics Corporation: Performance Boost of Crystalline In-Ga-Zn-O Material and Transistor with Extremely Low Leakage for IoT Normally-Off CPU Application		NaMLab gGmbH: Novel Ferroelectric FET Based Synapse for Neuromorphic Systems
	C17-4 9:45-10:10	C18-4 9:45-10:10	C19-4 9:45-10:10	JFS3-4 9:45-10:10		T13-4 9:45-10:10
	Massachusetts Institute of Technology: A Fully-Integrated Energy-Efficient H.265/HEVC Decoder with eDRAM for Wearable Devices	Univ. of Ulm: A 107 dB SFDR, 80 kS/s Nyquist-Rate SAR ADC Using a Hybrid Capacitive and Incremental ΣΔ DAC	Sony Semiconductor Solutions: 224-ke Saturation Signal Global Shutter CMOS Image Sensor with In-Pixel Pinned Storage and Lateral Overflow Integration Capacitor	Renesas Electronics: A 65 nm 1.0 V 1.84 ns Silicon-On-Thin-Box (SOTB) Embedded SRAM with 13.72 nW/Mbit Standby Power for Smart IoT		imec: Design-Technology Co-Optimization for OxRRAM-Based Synaptic Processing Unit
10:30-12:35	**C20: Circuits for Security and Low Power**	**C21: High Speed ADCs**		**JFS4: Computing Beyond Von Neumann**		**T14: SiGe / Ge FET 2**
	C20-1 10:30-10:55	C21-1 10:30-10:55		JFS4-1 10:30-10:55 **(Invited)**		T14-1 10:30-10:55
	Univ. of Michigan: Recryptor: A Reconfigurable In-Memory Cryptographic Cortex-M0 Processor for IoT	ETH Zurich: A 12b 61dB SNDR 300MS/s SAR ADC with Inverter-Based Preamplifier and Common-Mode-Regulation DAC in 14nm CMOS FinFET		IBM Research: Implementation Challenges for Scalable Neuromorphic Computing		AIST: First Experimental Observation of Channel Thickness Scaling (Down to 3 nm) Induced Mobility Enhancement in UTB GeOI*n* MOSFETs
	C20-2 10:55-11:20	C21-2 10:55-11:20		JFS4-2 10:55-11:20 **(Invited)**		T14-2 10:55-11:20
	Kobe Univ.: A 2.5ns-Latency 0.39pJ/b 289μm²/Gb/s Ultra-Light-Weight PRINCE Cryptographic Processor	Marvell - Shanghai: A 0.014mm² 10-Bit 2GS/s Time-Interleaved SAR ADC with Low-Complexity Background Timing Skew Calibration		Keio Univ.: Distributed Quantum Computing Systems: Technology to Quantum Circuits		imec: Strained Germanium Gate-All-Around PMOS Device Demonstration Using Selective Wire Release Etch Prior to Replacement Metal Gate Deposition
	C20-3 11:20-11:45	C21-3 11:20-11:45		JFS4-3 11:20-11:45		T14-3 11:20-11:45
	The Univ. of Texas at Austin: Strong Subthreshold Current Array PUF with 2^25 Challenge-Response Pairs Resilient to Machine Learning Attacks in 130nm CMOS	Analog Devices: An 18-Bit 2MS/s Pipelined SAR ADC Utilizing a Sampling Distortion Cancellation Circuit with -107dB THD at 100kHz		Univ. of Notre Dame: Ultra-Low Power Probabilistic IMT Neurons for Stochastic Sampling Machines		imec: Performance and Electrostatic Improvement by High-Pressure Anneal on Si-Passivated Strained Ge pFinFET and Gate All Around Devices with Superior NBTI Reliability
	C20-4 11:45-12:10	C21-4 11:45-12:10		JFS4-4 11:45-12:10		T14-4 11:45-12:10
	Univ. of Michigan: A Sequence Dependent Challenge-Response PUF Using 28nm SRAM 6T Bit Cell	Analog Devices: A 16-Bit 16MS/s SAR ADC with On-Chip Calibration in 55nm CMOS		Tsinghua Univ.: A 462GOPs/J RRAM-Based Nonvolatile Intelligent Processor for Energy Harvesting IoE System Featuring Nonvolatile Logics and Processing-In-Memory		National Univ. of Singapore: The First GeSn FinFET on a Novel GeSnOI Substrate Achieving Lowest S of 79 mV/decade and Record High $G_{m,int}$ of 807 μS/μm for GeSn P-FETs
	C20-5 12:10-12:35	C21-5 12:10-12:35				
	Columbia Univ.: A Continuous-Time Digital IIR Filter with Signal-Derived Timing, Agile Power Dissipation and Synchronous Output	The Univ. of Texas at Dallas: A 2GS/s 8b Flash ADC Based on Remainder Number System in 65nm CMOS				
12:35-14:00			**Luncheon Talk** **Approach to Develop Prosthetic Technology as a Part of Body**			
14:00-15:40	**C22: (CFS) Advanced Sensing Systems**	**C23: High-Speed and Power Efficient Wireless Transceivers**		**T15: Memory 2 Flash MRAM**		**T16: Process**
	C22-1 14:00-14:25 **(Invited)**	C23-1 14:00-14:25		T15-1 14:00-14:25		T16-1 14:00-14:25
	Sony Semiconductor Solutions: 320x240 Back-Illuminated 10μm CAPD Pixels for High Speed Modulation Time-of-Flight CMOS Image Sensor	Tokyo Institute of Technology: A 100mW 3.0 Gb/s Spectrum Efficient 60 GHz Bi-Phase OOK CMOS Transceiver		Samsung Electronics: High-Speed and Logic-Compatible Split-Gate Embedded Flash on 28-nm Low-Power HKMG Logic Process		IBM Research: Dual Beam Laser Annealing for Contact Resistance Reduction and Its Impact on VLSI Integrated Circuit Variability
	C22-2 14:25-14:50 **(Invited)**	C23-2 14:25-14:50		T15-2 14:25-14:50		T16-2 14:25-14:50
	DENSO: An Imager Using 2-D Single-Photon Avalanche Diode Array in 0.18-μm CMOS for Automotive LIDAR Application	KAIST: A 230-260GHz Wideband Amplifier in 65nm CMOS Based on Dual-Peak G_{max}-Core		Seoul National Univ.: First Demonstration of Diode-Type 3-D NAND Flash Memory String Having Super-Steep Switching Slope		imec: Sub-10^{-9} Ω.cm² Contact Resistivity on p-SiGe Achieved by Ga Doping and Nanosecond Laser Activation
	C22-3 14:50-15:15	C23-3 14:50-15:15		T15-3 14:50-15:15		T16-3 14:50-15:15
	Univ. of Edinburgh: A 16.5 Giga Events/s 1024 × 8 SPAD Line Sensor with Per-Pixel Zoomable 50ps-6.4ns/bin Histogramming TDC	Univ. of California, Berkeley: A 65nm CMOS I/Q RF Power DAC with 24 - 42dB 3rd Harmonic Cancellation and up to 18dB Mixed-Signal Filtering		Chuo Univ.: Flash Reliability Boost Huffman Coding (FRBH): Co-Optimization of Data Compression and V_{TH} Distribution Modulation to Enhance Data-Retention Time by Over 2900x		IBM Research: Highly-Selective Superconformal CVD Ti Silicide Process Enabling Area-Enhanced Contacts for Next-Generation CMOS Architectures
	C22-4 15:15-15:40	C23-4 15:15-15:40		T15-4 15:15-15:40		T16-4 15:15-15:40
	Univ. of Michigan: A 272.49 pJ/pixel CMOS Image Sensor with Embedded Object Detection and Bio-Inspired 2D Optic Flow Generation for Nano-Air-Vehicle Navigation	Renesas Electronics: A 43%-Efficiency 20dBm Sub-GHz Transmitter Employing Rise-Edge-Synchronized Harmonic Calibration with 33.3% Duty Cycle		GLOBALFOUNDRIES: CMOS-Embedded STT-MRAM Arrays in 2x nm Nodes for GP-MCU Applications		National Univ. of Singapore: Record Low Specific Contact Resistivity (1.2×10^{8} Ω-cm²) for P-Type Semiconductors: Incorporation of Sn into Ge and *In-Situ* Ga Doping
16:00-18:05	**C24: Physical Sensors**	**C25: High-Speed Wireline Circuits**	**C26: Processors and SoC**	**T17: CMOS Integration II**		
	C24-1 16:00-16:25	C25-1 16:00-16:25	C26-1 16:00-16:25	T17-1 16:00-16:25		
	KAIST: A 10.1° 56-Channel, 183 uW/electrode, 0.73 mm²/sensor High SNR 3D Hover Sensor Based on Enhanced Signal Refining and Fine Error Calibrating Techniques	IBM T. J. Watson Research Center: A 32Gb/s, 4.7pJ/bit Optical Link with −11.7dBm Sensitivity in 14nm FinFET CMOS	National Taiwan Univ.: A 501mW 7.61Gb/s Integrated Message-Passing Detector and Decoder for Polar-Coded Massive MIMO Systems	GLOBALFOUNDRIES: Low-Variation SRAM Bitcells in 22nm FDSOI Technology		
	C24-2 16:25-16:50	C25-2 16:25-16:50	C26-2 16:25-16:50	T17-2 16:25-16:50		
	CEA-LETI: A Robust and Versatile, -40°C to +180°C, 8Sps to 1kSps, Multi Power Source Wireless Sensor System for Aeronautic Applications	IBM Research: A 60 Gb/s 1.9 Pj/bit NRZ Optical-Receiver with Low Latency Digital CDR in 14nm CMOS FinFET	ARM: A 12.4pJ/cycle Sub-Threshold, 16pJ/cycle Near-Threshold ARM Cortex-M0+ MCU with Autonomous SRPG/DVFS and Temperature Tracking Clocks	CEA-LETI: Impact of Strain on Access Resistance in Planar and Nanowire CMOS Devices		
	C24-3 16:50-17:15	C25-3 16:50-17:15	C26-3 16:50-17:15	T17-3 16:50-17:15		
	Univ. of Michigan: A 6×5×4mm³ General Purpose Audio Sensor Node with a 4.7μW Audio Processing IC	NTT: A 2.25-mW/Gb/s 80-Gb/s-PAM4 Linear Driver with a Single Supply Using Stacked Current-Mode Architecture in 65-nm CMOS	Univ. of California, Los Angeles: A 2.267 Gbps, 93.7pJ/b Non-Binary LDPC Decoder for Storage Applications	CEA-LETI: Key Process Steps for High Performance and Reliable 3D Sequential Integration		
	C24-4 17:15-17:40	C25-4 17:15-17:40	C26-4 17:15-17:40	T17-4 17:15-17:40		
	Univ. of Michigan: A 4.7μW Switched-Bias MEMS Microphone Preamplifier for Ultra-Low-Power Voice Interfaces	Xilinx: A 26-Gb/s 8.1-mW Receiver with Linear Sampling Phase Detector for Data and Edge Equalization	Tsinghua Univ.: A 130nm FeRAM-Based Parallel Recovery Nonvolatile SOC for Normally-OFF Operations with 3.9× Faster Running Speed and 11× Higher Energy Efficiency Using Fast Power-On Detection and Nonvolatile Radio Controller	GLOBALFOUNDRIES: Influence of Stress Induced CT Local Layout Effect (LLE) on 14nm FinFET		
		C25-5 17:40-18:05	C26-5 17:40-18:05	T17-5 17:40-18:05 (Late News)		
		GLOBALFOUNDRIES: A 28.05Gb/s Transceiver Using Quarter-Rate Triple-Speculation Hybrid-DFE Receiver with Calibrated Sampling Phases in 32nm CMOS	Univ. of Virginia: A Battery-Less 507nW SoC with Integrated Platform Power Manager and SiP Interfaces	IBM: Stacked Nanosheet Gate-All-Around Transistor to Enable Scaling Beyond FinFET		