2023 Symposium on VLSI Technology and Circuits (Sunday, June 11)

Time	Suzaku III	Suzaku II	Suzaku I	Shunju III	Shunju II	Shunju I	Le Bois	La Cigogne	Le Cygne
8:00-20:00	Registration								
8:30-18:30					8:30-18:30 2023 Silicon Nanoelectronics Workshop (Day 1)				
17:30-19:15								Workshop 1	
20:00-21:45	Workshop 3	Workshop 2					Workshop 4	Workshop 5	Workshop 6

Workshop 1: Open Source PDKs and EDAs, Community Experiences toward Democratization of Chip Design [La Cigogne]

Design Experience: "The Journey of Two Novice LSI Enthusiasts: Tape-Out of CPU+RAM in Just One Month", K. Uchiyama* and Y. Azuma**, *Univ. of Electro-Communications and **Univ. of Tsukuba

From Zero to 1000 Open Source Custom Designs in Two Years, M. Kassem, Efabless

The SKY130 Open Source PDK: Building an Open Source Innovation Ecosystem, S. Kosier, SkyWater Technology

Open Source Chip Design on GF180MCU – A Foundry Perspective, K. Chandrasekaran, GlobalFoundries

Japan Foundries' Perspectives on Silicon Design Democratization, S. Hara, Minimal Fab & AIST

Google's Perspective on Open Source PDKs, Open Source EDA Tools, and OpenMPW Shuttle Program, J. Euphrosine and T. Ansell, Google LLC

The Nanofabrication Accelerator Project, M. Daniels, NIST

Japanese Government Perspective on Silicon Design Democratization, Y. Ogino, The Ministry of Economy, Trade and Industry (METI)

Workshop 2: EUV Lithography & Path to High NA EUV Patterning Solutions [Suzaku I+II]

Development of Current EUV Tools and Future High NA Tools, A. Yen, ASML

Novel Resists to Achieve Promised High NA EUV Resolution, R. Wise, Lam Research Corp.

EUV and High NA EUV Mask Challenges, N. Hayashi, Dai Nippon Printing Co., Ltd.

High NA EUV Exposure Tool Implications to Chip and Mask Layouts, D. Schmidt, IBM Research

Resolution Capability and Stitching of Features Across the High NA Exposure Fields, E. van Setten, ASML

Workshop 3: Towards Functional Backside : What's Next After Backside Power Delivery? [Suzaku III]

System and Physical Design: Backside PDN for Mobile Applications, S.-C. Song, Google

System and Physical Design: Design and Process Considerations for Implementing Holistic Routing : Power Delivery, Clocking, and Signaling, R. Preston, ARM Ltd.

System and Physical Design: A New VLSI R&D Frontier : Cell-Level Interconnects to Enable Back-Side Power Delivery Networks (BSPDN) and Device Stacking, M. Kobrinsky, Intel Corp.

Electronic Design Automation: Backside Clock Delivery : Opportunities and Challenges from System Design Perspectives, S. K. Lim, Georgia Institute of Technology

Electronic Design Automation: Enabling Backside Technology Benefits Using Cadence Digital Full Flow, M. Yue, Cadence

Electronic Design Automation: Realizing PPA Benefits of Backside Power and Signal Routing Using Synopsys Digital Design Flow, A. Khurana, Synopsys, Inc.

Process and Integration: 3D Integration of SoC Power Delivery : Contacting the Standard Cell Power Grid from the Wafer Backside, A. Veloso, imec

Process and Integration: Evolution of Backside PDN and Its Impact on Lithography, P. Wöltgens, ASML

Workshop 4: The Deployment of Materials to System Co-Optimization Methodology (MSCO) to Enable Rapid PPACt Assessment for Advanced Node Technology Development [Le Bois]

Materials to Systems Co-Optimization: Accelerating Technological Innovations, B. Ayyagari-Sangamalli, Applied Materials, Inc.

Transition from Gate-All-Around to Stacked Transistor Architecture for Logic and SRAM, V. Moroz, Synopsys

System to Device Co-Optimization for Efficient Development of Analog In-Memory Accelerators, G. Pedretti, Hewlett Packard Enterprise

Building a Methodology for Design- and System-Technology Co-Optimization, G. Hellings, imec

Design Technology Co-Optimization Solutions for Enhanced PPAC for CFET Device Architectures, J. Smith, Tokyo Electron's Technology Center

Application Dependent Architectural Design Technology Innovation and Co-Optimization for Feature Rich Technologies, N. Jain, GlobalFoundries

Workshop 5: Uniform and Rigorous Benchmarking of Machine Learning ICs and Systems [La Cigogne]

MLPerf Tiny : Benchmarking Ultra-Low-Power Machine Learning Systems, V. Janapa Reddi, Harvard Univ./MLCommons

Proper Benchmarking of In-Memory Computing Architectures, N. Shanbhag, Univ. of Illinois at Urbana-Champaign

Characterizing and Assessing In-Memory Computing Processors, N. Verma, Princeton Univ.

Benchmarking Novel AI Accelerators : Striving to Be Both Fair and Comprehensive, G. Burr, IBM Research

Challenges in Designing and Evaluating Neural Processing Units, J.-S. Park, Samsung Electronics Co., Ltd.

Workshop 6: 3D Image Sensor [Le Cygne]

Role and Function of LiDAR Sensor for Autonomous Driving: Beyond Autonomous Driving Level 3, K. Kweon, Hyundai Motor Company

3D Sensing Technologies for Immersive Experiences in the Metaverse, H. Finkelstein, Meta

Integrated LiDAR Sensors for L4 Autonomous Vehicles, J. Dunphy, Waymo

Indirect-ToF System for Non-Mobile Application, S.-C. Shin, Samsung Electronics Co., Ltd.

Time of Flight 3D-Sensing Architectures, B. Rae, STMicroelectronics

Silicon-Based FMCW Imaging for Human-Like Vison, M. Asghari, SiLC

2023 Symposium on VLSI Technology and Circuits (Monday, June 12)

Time	Suzaku III	Suzaku II	Suzaku I	Shunju III	Shunju II	Shunju I
7:30-18:00	Registration					
8:25-12:20		**Short Course 2** **Future Directions in Highspeed Wireline/Optical IO** **8:25** **Introduction** **8:30** **Industry Megatrends Driving Connectivity R&D,** T. C. Carusone, Univ. of Toronto / Alphawave Semi **9:20** **SerDes System Design,** T. Toifl, Cisco Systems **10:10** **Break** **10:40** **Trends in Digital Coherent Technologies with DSP ASICs for Optical Communication Systems,** F. Hamaoka, NTT Network Innovation Laboratories **11:30** **Silicon Photonics Transceiver for High-Density Optical Interconnection,** T. Nakamura, AIO Core Co., Ltd.		**Short Course 1** **Advanced CMOS Technologies for 1 nm & Beyond** **8:25** **Introduction** **8:30** **Advanced CMOS Transistor Scaling towards 1nm Node and Beyond,** C.-H. Lin, Intel Corp. **9:20** **Advances in EUV Lithography: From 0.33NA Technology towards High-NA and Beyond,** E. van Setten, ASML **10:10** **Break** **10:40** **Advanced Logic Transistor Process Technology towards 1-nm Node,** N. Yoshida, Applied Materials, Inc. **11:30** **Challenges and Innovations for Advanced BEOL Scaling at the 1nm Node and Beyond,** C. Penny, IBM Research	8:30-17:30 2023 Silicon Nanoelectronics Workshop (Day 2)
12:20-13:10		**12:20** **Lunch**			**12:20** **Lunch**	
13:10-17:00	13:30-17:00 Demo Setup	**13:10** **Beyond the Interconnect Challenges on the Way to Enabling Heterogenous Chiplets in Package,** A. Kashem, Advanced Micro Devices, Inc. (AMD) **14:00** **Architecture and Circuit Design of High-Speed Wireline Receivers,** A. Balankutty, Intel Corp. **14:50** **Break** **15:10** **Design Considerations for High-Speed Transmitters in Wireline and Optical Communications,** A. Vasani, Broadcom Ltd. **16:00** **Recent Developments and Challenges for NAND Flash Memory Interface,** T. Toi, KIOXIA Corp.			**13:10** **CMOS Scaling by Backside Power Delivery,** N. Horiguchi, imec **14:00** **Process Control Solutions for the Era of 3D Architecture Devices,** S. H. Han, Nova **14:50** **Break** **15:10** **Semiconductor Packaging Revolution in the Era of Chiplets,** Y. Orii, Rapidus Corp. **16:00** **Device Technology for 2D Layered Semiconductor FETs: Challenge & Perspective,** K. Nagashio, The Univ. of Tokyo	
17:30-21:45	**17:30-19:30 Demo Session & Reception**					19:30-21:45 2023 Spintronics Workshop

2023 Symposium on VLSI Technology and Circuits (Friday , June 16)

Time	Suzaku I+II+III
8:30-14:00	Registration
8:50-11:40	**Forum** **Compute Paradigms for Secured Microelectronics and Combinatorial Optimization** **8:50** **Opening by Forum Chair** **8:55** **Cyber-Physical Security from Chip to Cloud,** T. Perianin and V. Yli-Mäyry, Secure-IC **9:25** **In-Memory-Computing Based Accelerators for Secure Computing,** X. S. Hu, CISE CCF, National Science Foundation **9:55** **Cryptographic Circuit Technology Consisting of Photonic Logic Gates,** J. Takahashi, NTT Social Informatics Laboratories **10:25** **Looking Beyond Cryptography: Side-Channel Attacks (and more) on Machine Learning Accelerators,** S. Bhasin, Nanyang Technological Univ. **10:55** **Panel Discussion for Secured Microelectronics**
11:40-12:40	**11:40** **Lunch**
12:40-15:25	**12:40** **Quantum-Inspired Annealing Processor,** C. H. Kim, Univ. of Minnesota **13:10** **Simulated Bifurcation Machines: Combinatorial Optimization Accelerators Based on a Quantum-Inspired Parallelizable Algorithm,** K. Tatsumura, Toshiba Corp. **13:40** **Flexible Optimization Solver Using Mixed Analog-Digital In-Memory Computing,** J. P. Strachan, RWTH Aachen **14:10** **Engineering for Large-Scale Superconducting Quantum Annealers,** S. Kawabata, AIST **14:40** **Panel Discussion for Combinatorial Optimization** **15:25** **Closing by Forum Chair**

International Symposium on Integrated Circuits and Systems for Smart Society: 16:00-18:30 [La Cigogne]

2023 Symposium on VLSI Technology and Circuits (Tuesday, June 13)

Time	Suzaku III	Suzaku II	Suzaku I	Shunju III	Shunju II	Shunju I
7:00-17:00	**Registration**					
8:00-10:00				**Opening and Plenary Session 1** 8:00-8:40 ***Opening Remarks*** PL1-1 8:40-9:20 (Plenary) A*STAR Multi-Chiplet Heterogeneous Integration Packaging for Semiconductor System Scaling PL1-2 09:20-10:00 (Plenary) Google A Six-Word Story on the Future of VLSI: AI-Driven, Software-Defined, and Uncomfortably Exciting		
10:30-12:35	**C1: Neural Interfaces** C1-1 10:30-10:55 Univ. of Toronto — A Wireless Sensor-Brain Interface System for Tracking and Guiding Animal Behaviors Through Goal-Directed Closed-Loop Neuromodulation C1-2 10:55-11:20 Univ. of Michigan — A Wireless Neural Stimulator IC for Cortical Visual Prosthesis C1-3 11:20-11:45 Stanford Univ. — A 1024-Channel 268 nW/pixel 36x36 μm²/ch Data-Compressive Neural Recording IC for High-Bandwidth Brain-Computer Interfaces C1-4 11:45-12:10 ETH Zurich — A 1,024-Channel, 64-Interconnect, Capacitive Neural Interface Using a Cross-Coupled Microelectrode Array and 2-Dimensional Code-Division Multiplexing C1-5 12:10-12:35 Columbia Univ. — A Wireless, Mechanically Flexible, 25μm-Thick, 65,536-Channel Subdural Surface Recording and Stimulating Microelectrode Array with Integrated Antennas	**C2: Non-Volatile Memory and Low Power SRAM** C2-1 10:30-10:55 KIOXIA — A 1Tb 3b/Cell 3D-Flash Memory of more than 17Gb/mm² bit Density with 3.2Gbps Interface and 205MB/s Program Throughput C2-2 10:55-11:20 Samsung Electronics — A 14nm 128Mb Embedded MRAM Macro Achieved the Best Figure-Of-Merit with 80MHz Read Operation and 18.1Mb/mm² Implementation at 0.64V C2-3 11:20-11:45 Samsung Electronics — A 3.0 Gb/s/pin 4th Generation F-Chip with Toggle 5.0 Specification for 16Tb NAND Flash Memory Multi Chip Package C2-4 11:45-12:10 Sony Semiconductor Solutions — A 40 nm 2 kb MTJ-Based Non-Volatile SRAM Macro with Novel Data-Aware Store Architecture for Normally Off Computing C2-5 12:10-12:35 TSMC Design Technology — 3.7-GHz Multi-Bank High-Current Single-Port Cache SRAM with 0.5V-1.4V Wide Voltage Range Operation in 3nm FinFET for HPC Applications		**T1: Highlight 1** T1-1 10:30-10:55 Intel — E-Core Implementation in Intel 4 with PowerVia (Backside Power) Technology T1-2 10:55-11:20 Samsung Electronics — World's First GAA 3nm Foundry Platform Technology (SF3) with Novel Multi-Bridge-Channel-FET (MBCFET™) Process T1-3 11:20-11:45 imec — Nanosheet-Based Complementary Field-Effect Transistors (CFETs) at 48nm Gate Pitch, and Middle Dielectric Isolation to Enable CFET Inner Spacer Formation and Multi-Vt Patterning T1-4 11:45-12:10 TSMC — Scaled Contact Length with Low Contact Resistance in Monolayer 2D Channel Transistors T1-5 12:10-12:35 Applied Materials — Contact Cavity Shaping and Selective SiGe:B Low-Temperature Epitaxy Process Solution for Sub 10^{-9} Ω.cm² Contact Resistivity in Nonplanar FETs	
12:35-14:00						
14:00-15:40	**C3: Processors** C3-1 14:00-14:25 National Taiwan Univ. — A 26.4mW, 18.6MS/s Image Reconstruction Processor for IoT Compressive Sensing C3-2 14:25-14:50 National Taiwan Univ. — A 169mW Fully-Integrated Ultrasound Imaging Processor Supporting Advanced Modes for Hand-Held Devices C3-3 14:50-15:15 The Univ. of Tokyo — 183.4nJ/inference 152.8μW Single-Chip Fully Synthesizable Wired-Logic DNN Processor for Always-On 35 Voice Commands Recognition Application C3-4 15:15-15:40 MediaTek — A 12-nm 0.62-1.61 mW Ultra-Low Power Digital CIM-Based Deep-Learning System for End-to-End Always-On Vision	**C4: Continuous-Time A/D Converteres** C4-1 14:00-14:25 MIT — A 6.4-GS/s 1-GHz BW Continuous-Time Pipelined ADC with Time-Interleaved Sub-ADC-DAC Achieving 61.7-dB SNDR in 16-nm FinFET C4-2 14:25-14:50 Univ. of Michigan — A 0.024mm² 84.2dB-SNDR 1MHz-BW 3rd-Order VCO-Based CTDSM with NS-SAR Quantizer (NSQ VCO CTDSM) C4-3 14:50-15:15 Delft Univ. of Technology — A 6GHz Multi-Path Multi-Frequency Chopping CTΔΣ Modulator Achieving 122dBFS SFDR from 150kHz to 120MHz BW C4-4 15:15-15:40 Technical Univ. of Berlin — A 4.4 GS/s 220 MHz ΣΔ ADC with a Linearized Back-Gate Controlled GmC Filter	**C5: Wireless Transceivers** C5-1 14:00-14:25 Tokyo Institute of Technology — A Time-Mode-Modulation Digital Quadrature Power Amplifier Based on 1-bit Delta-Sigma Modulator and Transformer Combined FIR FIlter C5-2 14:25-14:50 imec — An 8.7 mW/TX, 21 mW/RX 6-to-9GHz IEEE 802.15.4a/4z Compliant IR-UWB Transceiver with Pulse Pre-Emphasis Achieving 14mm Ranging Precision C5-3 14:50-15:15 POSTECH — A 6.5nW, -73.5dBm Sensitivity, Cryptographic Wake-Up Receiver with a PUF-Based OTP and Temperature-Insensitive Code Recovery C5-4 15:15-15:40 Peking Univ. — An All-Digital Outphasing Transmitter IC for Ka-Band Bit-to-RF Concurrent Multi-Beam DBF Array	**T2: Reliability and Characterization** T2-1 14:00-14:25 National Univ. of Singapore — A Novel Bridge Transmission Line Method for Thin-Film Semiconductors: Modelling, Simulation Verification, and Experimental Demonstration T2-2 14:25-14:50 National Univ. of Singapore — First Study of the Charge Trapping Aggravation Induced by Anti-Ferroelectric Switching in the MFIS Stack T2-3 14:50-15:15 East China Normal Univ. — Catching the Missing EM Consequence in Soft Breakdown Reliability in Advanced FinFETs: Impacts of Self-Heating, On-State TDDB, and Layout Dependence T2-4 15:15-15:40 National Yang Ming Chiao Tung Univ. — FeRAM Recovery up to 200 Periods with Accumulated Endurance 10^{12} Cycles and an Applicable Array Circuit toward Unlimited eNVM Operations	**T3: NAND Flash** T3-1 14:00-14:25 Samsung Electronics — Novel Strategies for Highly Uniform and Reliable Cell Characteristics of 8th Generation 1Tb 3D-NAND Flash Memory T3-2 14:25-14:50 Tokyo Electron Miyagi — Beyond 10 μm Depth Ultra-High Speed Etch Process with 84% Lower Carbon Footprint for Memory Channel Hole of 3D NAND Flash over 400 Layers T3-3 14:50-15:15 KIOXIA — Demonstration of Recovery Annealing on 7-Bits per Cell 3D Flash Memory at Cryogenic Operation for Bit Cost Scalability and Sustainability T3-4 15:15-15:40 Samsung Electronics — High Bit Cost Scalability and Reliable Cell Characteristics for 7th Generation 1Tb 4Bit/Cell 3D-NAND Flash	**T4: DTCO** T4-1 14:00-14:25 Samsung Electronics — Breakthrough Design Technology Co-Optimization Using BSPDN and Standard Cell Variants for Maximizing Block-Level PPA T4-2 14:25-14:50 imec — PPA and Scaling Potential of Backside Power Options in N2 and A14 Nanosheet Technology T4-3 14:50-15:15 imec — Upcoming Challenges of ESD Reliability in DTCO with BS-PDN Routing via BPRs T4-4 15:15-15:40 MIT — Towards DTCO in High Temperature GaN-On-Si Technology: Arithmetic Logic Unit at 300 °C and CAD Framework Up to 500 °C
16:00-18:05	**C6: High-Speed Links** C6-1 16:00-16:25 Univ. of California, Los Angeles — A 112-Gb/s 58-mW PAM4 Transmitter in 28-nm CMOS Technology C6-2 16:25-16:50 Intel — A 256 Gbps Heterogeneously Integrated Silicon Photonic Microring-Based DWDM Receiver Suitable for In-Package Optical I/O C6-3 16:50-17:15 Univ. of Toronto — A 0.32pJ/b 90Gbps PAM4 Optical Receiver Front-End with Automatic Gain Control in 12nm CMOS FinFET C6-4 17:15-17:40 Chinese Academy of Sciences — A 64-Gb/s Reference-Less PAM4 CDR with Asymmetrical Linear Phase Detector Soring 231.5-fs_{rms} Clock Jitter and 0.21-pJ/Bit Energy Efficiency in 40-nm CMOS C6-5 17:40-18:05 Texas A&M Univ. — A 50Gb/s DAC-Based Multicarrier Polar Transmitter in 22nm FinFET	**C7: Digital Systems** C7-1 16:00-16:25 Univ. of Michigan — Arvon: A Heterogeneous SiP Integrating a 14nm FPGA and Two 22nm 1.8TFLOPS/W DSPs with 1.7Tbps/mm² AIB 2.0 Interface to Provide Versatile Workload Acceleration C7-2 16:25-16:50 National Taiwan Univ. — A 4.8mW, 800Mbps Hybrid Crypto SoC for Post-Quantum Secure Neural Interfacing C7-3 16:50-17:15 Nanyang Technological Univ. — A Bit-Serial Computing Accelerator for Solving Coupled Partial Differential Equations C7-4 17:15-17:40 POSTECH — A 2.35 Gb/s/mm² (7440, 6696) NB-LDPC Decoder Over GF(32) Using Memory-Reduced Column-Wise Trellis Min-Max Algorithm in 28nm CMOS Technology C7-5 17:40-18:05 Georgia Institute of Technology — A 65nm 60mW Dual-Loop Adaptive Digital Beamformer with Optimized Sidelobe Cancellation and On-Chip DOA Estimation for mm-Wave Applications	**C8: Biomedical Circuit and Systems** C8-1 16:00-16:25 Southern Univ. of Science and Technology — Wireless Body-Area Network Transceiver ICs with Concurrent Body-Coupled Powering and Communication Using Single Electrode C8-2 16:25-16:50 KU Leuven — A Fingertip-Mimicking 12×16 200μm-Resolution *e*-skin Taxel Readout Chip with Per-Taxel Spiking Readout and Embedded Receptive Field Processing C8-3 16:50-17:15 POSTECH — A 110dB-TCMRR TDM-based 8-Channel Noncontact ECG Recording IC with Suppression of Motion-Induced Coupling in < 0.3s and CMI Cancellation Up to $22V_{PP}$ C8-4 17:15-17:40 Delft Univ. of Technology — A Pitch-Matched Transceiver ASIC for 3D Ultrasonography with Micro-Beamforming ADCs Based on Passive Boxcar Integration and a Multi-Level Datalink C8-5 17:40-18:05 National Taiwan Univ. — A CMOS/Microfluidics Point-of-Care SoC Employing Square-Wave Voltcoulometry for Biosensing with Aptamers and CRISPR-Cas12a Enzymes	**JFS1: New Computing** JFS1-1 16:00-16:25 (Invited) Synopsys — Exploring Power Savings of Gate-All-Around Cryogenic Technology JFS1-2 16:25-16:50 (Invited) NTT — Circuit Designs for Practical-Scale Fault-Tolerant Quantum Computing JFS1-3 16:50-17:15 AIST — Long-Time-Constant Leaky-Integrating Oxygen-Vacancy Drift-Diffusion FET for Human-Interactive Spiking Reservoir Computingcomputing JFS1-4 17:15-17:40 POSTECH — Experimental Demonstration of Probabilistic-Bit (p-bit) Utilizing Stochastic Oscillation of Threshold Switch Device JFS1-5 17:40-18:05 Univ. of California, Santa Barbara — Accelerating Adaptive Parallel Tempering with FPGA-Based p-bits	**T5: Ferroelectric 1: FeFETs** T5-1 16:00-16:25 KAIST — Strategy for 3D Ferroelectric Transistor: Critical Surface Orientation Dependence of $HfZrO_x$ on Si T5-2 16:25-16:50 The Univ. of Tokyo — HZO Scaling and Fatigue Recovery in FeFET with Low Voltage Operation: Evidence of Transition from Interface Degradation to Ferroelectric Fatigue T5-3 16:50-17:15 National Taiwan Univ. — First Stacked Nanosheet FeFET Featuring Memory Window of 1.8V at Record Low Write Voltage of 2V and Endurance >1E11 Cycles T5-4 17:15-17:40 National Univ. of Singapore — First Demonstration of BEOL-Compatible MFMIS Fe-FETs with 3D Multi-Fin Floating Gate: In-Situ ALD-Deposited MFM, L_{CH} of 50 nm, > 2×10^9 Endurance, and 58.3% Area Saving T5-5 17:40-18:05 Georgia Institute of Technology — Cold-FeFET as Embedded Non-Volatile Memory with Unlimited Cycling Endurance	**T6: Logic Technology 1: Advanced Platforms and Device Structures** T6-1 16:00-16:25 Intel — Intel PowerVia Technology: Backside Power Delivery for High Density and High-Performance Computing T6-2 16:25-16:50 Qualcomm Technologies — High Performance 5G Mobile SOC Productization with 4nm EUV Fin-FET Technology T6-3 16:50-17:15 imec — Molybdenum Nitride as a Scalable and Thermally Stable pWFM for CFET T6-4 17:15-17:40 imec — Integration of a Stacked Contact MOL for Monolithic CFET T6-5 17:40-18:05 POSTECH — Front-Side and Back-Side Power Delivery Network Guidelines for 2nm Node High Perf Computing and Mobile SoC Applications
20:00-21:30		**Evening Panel Discussion 2** **Can Universities Help to Revitalize the IC Design Industry? If So, How?**			**Evening Panel Discussion 1** **What is Scalable & Sustainable in the Next 25 Years?**	

Diversity Meeting - Hosted by SSCS Women in Circuits: 12:45-13:55 [Le Bois]

SSCS/EDS Young Professionals and Women in Circuits Mentoring Event: 18:00-19:30 [La Cigogne]

2023 Symposium on VLSI Technology and Circuits (Wednesday, June 14)

Time	Suzaku III	Suzaku II	Suzaku I	Shunju III	Shunju II	Shunju I
7:00-17:00	Registration					
8:00-10:00				**Award and Plenary Session 2**		
				8:00-8:40		
				Award Ceremony		
				PL2-1 8:40-9:20 (Plenary)		
				Hitachi — Quantum Computing from Hype to Game Changer		
				PL2-2 09:20-10:00 (Plenary)		
				Western Digital — Searching for Nonlinearity: Scaling Limits in NAND Flash		
10:30-12:35	**C9: Advanced SRAM Design**	**C10: Advanced Memories for AI**		**T7: Highlight 2**		
	C9-1 10:30-10:55	C10-1 10:30-10:55		T7-1 10:30-10:55		
	TSMC Design Technology — A 3nm 256Mb SRAM in FinFET Technology with New Array Banking Architecture and Write-Assist Circuitry Scheme for High-Density and Low-V_{MIN} Applications	Georgia Institute of Technology — A 2.38 MCells/mm^2 9.81 - 350 TOPS/W RRAM Compute-in-Memory Macro in 40nm CMOS with Hybrid Offset/I_{OFF} Cancellation and $I_{CELL}R_{BLSL}$ Drop Mitigation		KIOXIA — Highly Scalable Metal Induced Lateral Crystallization (MILC) Techniques for Vertical Si Channel in Ultra-High (> 300 Layers) 3D Flash Memory		
	C9-2 10:55-11:20	C10-2 10:55-11:20		T7-2 10:55-11:20		
	IBM Systems and Technology — A 1.9GHz 0.57V Vmin 576Kb Embedded Product-Ready L2 Cache in 5nm FinFET Technology	National Tsing Hua Univ. — A 28nm Nonvolatile AI Edge Processor using 4Mb Analog-Based Near-Memory- Compute ReRAM with 27.2 TOPS/W for Tiny AI Edge Devices		SK hynix — QLC Programmable 3D Ferroelectric NAND Flash Memory by Memory Window Expansion Using Cell Stack Engineering		
	C9-3 11:20-11:45	C10-3 11:20-11:45		T7-3 11:20-11:45		
	Samsung Electronics — A 4.0GHz UHS Pseudo Two-Port SRAM with BL Charge Time Reduction and Flying Word-Line for HPC Applications in 4nm FinFET Technology	KAIST — Scaling-CIM: An eDRAM-Based In-Memory-Computing Accelerator with Dynamic-Scaling ADC for SQNR-Boosting and Layer-Wise Adaptive Bit-Truncation		Stanford Univ. — First Observation of Ultra-high Polarization (~ 108 μC/cm^2) in Nanometer Scaled High Performance Ferroelectric HZO Capacitors with Mo Electrodes		
	C9-4 11:45-12:10	C10-4 11:45-12:10		T7-4 11:45-12:10		
	TSMC — A 4.24GHz 128X256 SRAM Operating Double Pump Read Write Same Cycle in 5nm Technology	MediaTek — A 12nm 137 TOPS/W Digital Compute-In-Memory Using Foundry 8T SRAM Bitcell Supporting 16 Kernel Weight Sets for AI Edge Applications		Sony Semiconductor Solutions — Noise Performance Improvements of 2-Layer Transistor Pixel Stacked CMOS Image Sensor with Non-Doped Pixel-FinFETs		
	C9-5 12:10-12:35	C10-5 12:10-12:35		T7-5 12:10-12:35		
	TSMC Design Technology Japan — A 3-nm 27.6-Mbit/mm^2 Self-Timed SRAM Enabling 0.48 - 1.2 V Wide Operating Range with Far-End Pre-Charge and Weak-Bit Tracking	KAIST — SP-PIM: A 22.41TFLOPS/W, 8.81Epochs/Sec Super-Pipelined Processing-In-Memory Accelerator with Local Error Prediction for On-Device Learning		KAIST — Cryogenic RF Transistors and Routing Circuits Based on 3D Stackable InGaAs HEMTs with Nb Superconductors for Large-Scale Quantum Signal Processing		
12:35-14:00						
14:00-15:40	**C11: DC-DC Converter**	**C12: Digital Building Blocks**	**C13: Millimeter-Wave Transceivers and Synthesizers**	**JFS2: AR/VR/MR Metaverse 1**	**TFS1: Future Memory Directions**	**T8: Logic Technology 2: Advanced Processes**
	C11-1 14:00-14:25	C12-1 14:00-14:25	C13-1 14:00-14:25	JFS2-1 14:00-14:25 (Invited)	TFS1-1 14:00-14:25 (Invited)	T8-1 14:00-14:25
	Univ. of Macau — A 0.05-to-3.1A 585mA/mm^3 97.3%-Efficiency Outphase Switched-Capacitor Hybrid Buck Converter with Relieved Capacitor Inrush Current and C_{OUT}-Free Operation	Rice Univ. — A Fully Synthesizable 100Mbps Edge-Chasing True Random Number Generator	Tokyo Institute of Technology — A Sub-THz Full-Duplex Phased-Array Transceiver with Self-Interference Cancellation and LO Feedthrough Suppression	Meta — A Prototype 5nm Custom Sensor SoC for Augmented Reality/Virtual Reality Targeting Smartglasses with Embedded Computer Vision, Audio, Security and ML	Samsung R&D Center — Ongoing Evolution of DRAM Scaling via Third Dimension - Vertically Stacked DRAM -	TSMC — Building High Performance Transistors on Carbon Nanotube Channel
	C11-2 14:25-14:50	C12-2 14:25-14:50	C13-2 14:25-14:50	JFS2-2 14:25-14:50	TFS1-2 14:25-14:50 (Invited)	T8-2 14:25-14:50
	Sogang Univ. — 96.48% Peak-Efficiency Continuous-Current Step-Up Battery Charger (CC-SUBC) with Dual Energy-Harvesting Sources for Automotive Application	Intel — 218Kauth/S, 3nJ/Auth SCA/ML-Resistant Privacy-Preserving Mutual Authentication Accelerator with a Crypto-Double-Coupled PUF in 4nm Class CMOS	Tsinghua Univ. — An 11.4-to-16.4GHz FMCW Digital PLL with Cycle-Slipping Compensation and Back-Tracking DPD Achieving 0.034% RMS Frequency Error under 3.4-GHz Chirp Bandwidth and 960-MHz/μs Chirp Slope	Sony Semiconductor Solutions — A Back-Illuminated 6 μm SPAD Depth Sensor with PDE 36.5% at 940 nm via Combination of Dual Diffraction Structure and 2×2 On-Chip Lens	IBM — Phase Change Memory-Based Hardware Accelerators for Deep Neural Networks	National Univ. of Singapore — Record High Active Boron Doping Using Low Temperature *In-situ* CVD: Enabling Sub-5×10^{-10} Ω-cm^2 ρ_c from Cryogenic (5 K) to Room Temperature
	C11-3 14:50-15:15	C12-3 14:50-15:15	C13-3 14:50-15:15	JFS2-3 14:50-15:15	TFS1-3 14:50-15:15	T8-3 14:50-15:15
	Kyungpook National Univ. — A 19.8W/29.6W Hybrid Step-Up/Down DC-DC Converter with 97.2% Peak Efficiency for 1-Cell/2-Cell Battery Charger Applications	National Univ. of Singapore — ECC-Less Multi-Level SRAM Physically Unclonable Function and 127% PUF-to- Memory Capacity Ratio with No Bitcell Modification in 28nm	Univ. of Science and Technology of China — An 18.8-to-23.3 GHz ADPLL Based on Charge-Steering-Sampling Technique Achieving 75.9 fs RMS Jitter and −252 dB FoM	Northwestern Univ. — Human Activity Recognition SoC for AR/VR with Integrated Neural Sensing, AI Classifier and Chained Infrared Communication for Multi-Chip Collaboration	National Univ. of Singapore — Non-Destructive-Read 1T1C Ferroelectric Capacitive Memory Cell with BEOL 3D Monolithically Integrated IGZO Access Transistor for 4F^2 High-Density Integration	Kyungpook National Univ. — L_g = 60 nm $In_{0.53}Ga_{0.47}As$ MBCFETs: From g_{m_max} = 13.7 mS/μm and Q = 180 to Virtual-Source Modeling
	C11-4 15:15-15:40	C12-4 15:15-15:40	C13-4 15:15-15:40		TFS1-4 15:15-15:40	T8-4 15:15-15:40
	ETH Zurich — A 4.1W/mm^2 Peak Power Density and 77% Peak Efficiency Fully Integrated DC-DC Converter Based on Electromagnetically Coupled Class-D LC Oscillators and a Resonant LC Flying Impedance in 22nm FDSOI CMOS	Yonsei Univ. — A Static Contention-Free Dual-Edge-Triggered Flip-Flop with Redundant Internal Node Transition Elimination for Ultra-Low-Power Applications	Hong Kong Univ. of Science and Technology — A 24-30 GHz Cascaded QPLL Achieving 56.8-fs RMS Jitter and −248.6-dB FoM_{jitter}		MIT — Foundry Monolithic 3D BEOL Transistor + Memory Stack: Iso-Performance and Iso-Footprint BEOL Carbon Nanotube FET+RRAM vs. FEOL Silicon FET+RRAM	Forschungszentrum Jülich — High Performance 5 nm Si Nanowire FETs with a Record Small SS = 2.3 mV/dec and High Transconductance at 5.5 K Enabled by Dopant Segregated Silicide Source/Drain
16:00-18:05	**C14: Nyquist-Rate ADCs**	**C15: Images for Emerging Applications**	**C16: Advanced NNs**	**T9: PCM, ReRAM and Threshold Switch**	**T10: Ferroelectric 2: FeRAM, FTJ and FMD**	**T11: New Channel Material 1: InOx and ITO**
	C14-1 16:00-16:25	C15-1 16:00-16:25	C16-1 16:00-16:25	T9-1 16:00-16:25	T10-1 16:00-16:25	T11-1 16:00-16:25
	Politecnico di Mllano — A 2GS/s 11b 8x Interleaved ADC with 9.2 ENOB and 69.9dB SFDR in 28nm CMOS	Samsung Electronics — An Indirect Time-of-Flight CMOS Image Sensor Achieving Sub-ms Motion Lagging and 60fps Depth Image from On-Chip ISP	POSTECH — A 28 nm 66.8 TOPS/W Sparsity-Aware Dynamic-Precision Deep-Learning Processor	SK hynix — The Chalcogenide-Based Memory Technology Continues : Beyond 20nm 4-Deck 256Gb Cross-Point Memory	Chinese Academy of Sciences — First Demonstration of a Design Methodology for Highly Reliable Operation at High Temperature on 128kb 1T1C FeRAM Chip	Purdue Univ. — Ultrathin Atomic-Layer-Deposited In_2O_3 Radio-Frequency Transistors with Record High f_T of 36 GHz and BEOL Compatibility
	C14-2 16:25-16:50	C15-2 16:25-16:50	C16-2 16:25-16:50	T9-2 16:25-16:50	T10-2 16:25-16:50	T11-2 16:25-16:50
	Univ. of Macau — A 79.5dB-SNDR Pipelined-SAR ADC with a Linearity-Shifting 32× Dynamic Amplifier and Mounted-Over-Die Bypass Capacitors	Sony Semiconductor Solutions — A 3.36 μm-Pitch SPAD Photon-Counting Image Sensor Using Clustered Multi-Cycle Clocked Recharging Technique with Intermediate Most-Significant-Bit Readout	Tsinghua Univ. — ANP-G: A 28nm 1.04pJ/SOP Sub-mm^2 Spiking and Back-Propagation Hybrid Neural Network Asynchronous Olfactory Processor Enabling Few-Shot Class-Incremental On-Chip Learning	POSTECH — Simple Binary In-Te OTS with Sub-nm HfO_x Buffer Layer for 3D Vertical X-point Memory Applications	National Taiwan Univ. — 3D Stackable Vertical Ferroelectric Tunneling Junction (V-FTJ) with On/Off Ratio 1500x, Applicable Cell Current, Self-Rectifying Ratio 1000x, Robust Endurance of 10^7 Cycles, Multilevel and Demonstrated Macro Operation Toward High-Density BEOL NVMs	National Univ. of Singapore — Thickness-Engineered Extremely-Thin Channel High Performance ITO TFTs with Raised S/D Architecture: Record-Low R_{SD}, Highest Mobility (Sub-4 nm T_{ch} Regime), and High V_{TH} Tunability
	C14-3 16:50-17:15	C15-3 16:50-17:15	C16-3 16:50-17:15	T9-3 16:50-17:15	T10-3 16:50-17:15	T11-3 16:50-17:15
	Univ. of Michigan — A 150-MS/s Fully Dynamic SAR-Assisted Pipeline ADC Using a Floating Ring Amplifier and Gain-Enhancing Miller Negative-C	Univ. of Waterloo — A Monolithic Amorphous-Selenium/CMOS Small-Pixel-Effect-Enhanced X-Ray-Energy-Discriminating Quantum-Counting Pixel for Biomedical Imaging	IBM T. J. Watson Research Center — A Switched-Capacitor Integer Compute Unit with Decoupled Storage and Arithmetic for Cloud AI Inference in 5nm CMOS	Chinese Academy of Sciences — 16-Layer 3D Vertical RRAM with Low Read Latency (18ns), High Nonlinearity (>5000) and Ultra-Low Leakage Current (~pA) Self-Selective Cells	KAIST — Ultra-high Tunneling Electroresistance Ratio (2×10^4) & Endurance (10^8) in Oxide Semiconductor-Hafnia Self-Rectifying (1.5×10^3) Ferroelectric Tunnel Junction	Purdue Univ. — Ultrahigh Bias Stability of ALD In_2O_3 FETs Enabled by High Temperature O_2 Annealing
	C14-4 17:15-17:40	C15-4 17:15-17:40	C16-4 17:15-17:40	T9-4 17:15-17:40	T10-4 17:15-17:40	T11-4 17:15-17:40
	Hitachi — A 0.75V 0.016mm^2 12ENOB 7nm CMOS Cyclic ADC with 1.5bit Passive Amplification Stage and Dynamic Capacitance Scaling	National Tsing Hua Univ. — A -20°C~+107°C 52mk-NETD Reference-Cell-Free 15-bits ROIC for 80x60 Microbolometer Thermal Imager	Tokyo Institute of Technology — *Pianissimo:* A Sub-mW Class DNN Accelerator with Progressive Bit-by-Bit Datapath Architecture for Adaptive Inference at Edge	National Tsing Hua Univ. — High Density Embedded 3D Stackable Via RRAM in Advanced MCU Applications	National Univ. of Singapore — First Demonstration of BEOL-Compatible Write-Enhanced Ferroelectric-Modulated Diode (FMD): New Possibility for Oxide Semiconductor Memory Devices	Stanford Univ. — Co-Designed Capacitive Coupling-Immune Sensing Scheme for Indium-Tin-Oxide (ITO) 2T Gain Cell Operating at Positive Voltage Below 2 V
			C16-5 17:40-18:05			
			Tsinghua Univ. — A 28nm 77.35TOPS/W Similar Vectors Traceable Transformer Processor with Principal-Component-Prior Speculating and Dynamic Bit-Wise Stationary Computing			
17:00-19:00						
19:15-21:15	**Banquet**					
20:00-21:30						

Code-a-Chip Travel Award Meeting: 17:00-19:00 [Salon de Charme]

2023 Symposium on VLSI Technology and Circuits (Thursday, June 15)

Time	Suzaku III	Suzaku II	Suzaku I	Shunju III	Shunju II	Shunju I
8:00-17:00	Registration					
8:30-10:10		**C17: Power Management Circuit**	**C18: Data Conversion Techniques**	**JFS3: AR/VR/MR Metaverse 2**	**T12: Ferroelectric 3: Advanced Structures and Processes**	**T13: Quantum Computing and Cryo-CMOS**
		C17-1 8:30-8:55	C18-1 8:30-8:55	JFS3-1 8:30-8:55 (Invited)	T12-1 8:30-8:55	T13-1 8:30-8:55
		KU Leuven: A Fully Integrated 230 V_{RMS}-to-12 V_{DC} AC-DC Converter Achieving 9 mW/mm^2	Eindhoven Univ. of Technology: A 3-320 fJ/Conv.step Continuous Time Level Crossing ADC with Dynamic Self-Biasing Comparators Achieving 61.4 dB-SNDR	Sony: 216 fps 672 × 512 pixel 3 µm Indirect Time-of-Flight Image Sensor with 1-Frame Depth Acquisition for Motion Artifact Suppression	National Univ. of Singapore: Grain Size Reduction of Ferroelectric HZO Enabled by a Novel Solid Phase Epitaxy (SPE) Approach: Working Principle, Experimental Demonstration, and Theoretical Understanding	imec: Comprehensive 300 mm Process for Silicon Spin Qubits with Modular Integration
		C17-2 8:55-9:20	C18-2 8:55-9:20	JFS3-2 8:55-9:20	T12-2 8:55-9:20	T13-2 8:55-9:20
		Samsung Electronics: 5G NR RF PA Supply Modulator Supporting 179ns 0.5-to-5.5V Symbol Power Tracking and Envelope Tracking	Renesas Electronics: A 24-OSR to Simplify Anti-Aliasing Filter 2MHz-BW 83dB-DR 3rd-Order DT-DSM Using FIA-Based Integrator and Noise-Shaping SAR Combined Digital Noise-Coupling Quantizer	Meta: A 3.96µm, 124dB Dynamic Range, 6.2mW Stacked Digital Pixel Sensor with Monochrome and Near-Infrared Dual-Channel Global Shutter Capture	National Univ. of Singapore: First Demonstration of Work Function-Engineered BEOL-Compatible IGZO Non-Volatile MFMIS AFeFETs and Their Co-Integration with Volatile-AFeFETs	EPFL: Quantum Dots Array on Ultra-Thin SOI Nanowires with Ferromagnetic Cobalt Barrier Gates for Enhanced Spin Qubit Control
		C17-3 9:20-9:45	C18-3 9:20-9:45	JFS3-3 9:20-9:45	T12-3 9:20-9:45	T13-3 9:20-9:45
		Korea Univ.: A 93.5%-Efficiency 13.56-MHz-Bandwidth Optimal On/Off Tracking Active Rectifier with Fully Digital Feedback-Based Delay Control for Adaptive Efficiency Compensation	KAIST: A 2.5mW 12MHz-BW 69dB SNDR Passive Bandpass ΔΣ ADC with Highpass Noise-Shaping SAR Quantizers	KIST: Doping-Optimized Back-Illuminated Single-Photon Avalanche Diode in Stacked 40 nm CIS Technology Achieving 60% PDP at 905 nm	Univ. of California, Berkeley: Record Transconductance in L_{eff}~30 nm Self-Aligned Replacement Gate ETSOI nFETs Using Low EOT Negative Capacitance HfO_2-ZrO_2 Superlattice Gate Stack	TSMC: How Fault-Tolerant Quantum Computing Benefits from Cryo-CMOS Technology
		C17-4 9:45-10:10	C18-4 9:45-10:10		T12-4 9:45-10:10	T13-4 9:45-10:10
		Analog Devices: A 0.22mm^2 per Channel Data Link for Reinforced Isolation with >25kVpk Surge Tolerance and >295kV/µs Common Mode Transient Immunity	KAIST: A 187dB FoM_S 46fJ/Conv. 2nd-order Highpass ΔΣ Capacitance-to-Digital Converter		National Taiwan Univ.: Towards Epitaxial Ferroelectric HZO on n$^+$-Si/Ge Substrates Achieving Record $2P_r$ = 84 µC/cm^2 and Endurance > 1E11	Advanced Industrial Science and Technology: Determining the Low-Frequency Noise Source in Cryogenic Operation of Short-Channel Bulk MOSFETs
10:30-12:35	**C19: Analog Circuit Techniques**	**C20: Circuit Designs for Optical Systems**	**C21: PIM/CIM Systems**		**JFS4: 3D System Integration**	**T14: New Channel Material 2: InOx and 2D Material**
	C19-1 10:30-10:55	C20-1 10:30-10:55	C21-1 10:30-10:55		JFS4-1 10:30-10:55 (Invited)	T14-1 10:30-10:55
	Univ. of Michigan: A Reconfigurable Analog FIR Filter Achieving -70dB Rejection with Sharp Transition for Narrowband Receivers	KAIST: A Mobile OLED Source-Driver IC Featuring Ultra-Compact 3-Stage-Cascaded 10-Bit DAC and 42V/µs-Slew-Rate True-DC-Interpolative Super-OTA Buffer	Northwestern Univ.: A General-Purpose Compute-in-Memory Processor Combining CPU and Deep Learning with Elevated CPU Efficiency and Enhanced Data Locality		Advanced Micro Devices: AMD Instinct™ MI250X Accelerator Enabled by Elevated Fanout Bridge Advanced Packaging Architecture	The Univ. of Tokyo: A Nanosheet Oxide Semiconductor FET Using ALD InGaOx Channel and InSnOx Electrode with Normally-Off Operation, High Mobility and Reliability for 3D Integrated Devices
	C19-2 10:55-11:20	C20-2 10:55-11:20	C21-2 10:55-11:20		JFS4-2 10:55-11:20 (Invited)	T14-2 10:55-11:20
	ETH Zurich: An Energy-Efficient Impedance-Boosted Discrete-Time Amplifier Achieving 0.34 Noise Efficiency Factor and 389 MΩ Input Impedance	Samsung Electronics: A 16-Channel Active-Matrix Mini-LED Driver with an USI-B for EMI Noise Reduction	KAIST: A 709.3 TOPS/W Event-Driven Smart Vision SoC with High-Linearity and Reconfigurable MRAM PIM		TSMC: An Integrated System Scaling Solution for Future High Performance Computing	National Yang Ming Chiao Tung Univ.: Aggressively Scaled Atomic Layer Deposited Amorphous $InZnO_x$ Thin Film Transistor Exhibiting Prominent Short Channel Characteristics (SS= 69 mV/dec.; DIBL = 27.8 mV/V) and High G_m (802 µS/µm at V_{DS} = 2V)
	C19-3 11:20-11:45	C20-3 11:20-11:45	C21-3 11:20-11:45		JFS4-3 11:20-11:45	T14-3 11:20-11:45
	Sogang Univ.: A 1V 20.7µW Four-Stage Amplifier Capable of Driving a 4-to-12nF Capacitive Load with >1.07MHz GBW with an Improved Active Zero	Semiconductor Energy Laboratory: Two-Dimensionally Arranged Display Drivers Achieved by OS/Si Structure	Tsinghua Univ.: A 5.6-89.9TOPS/W Heterogeneous Computing-in-Memory SoC with High-Utilization Producer-Consumer Architecture and High-Frequency Read-Free CIM Macro		Powerchip Semiconductor Manufacturing: 4-Layer Wafer on Wafer Stacking Demonstration with Face to Face/Face to Back Stacked Flexibility Using Hybrid Bond/TSV-Middle for Various 3D Integration	Intel: 2D Materials in The BEOL
	C19-4 11:45-12:10	C20-4 11:45-12:10	C21-4 11:45-12:10		JFS4-4 11:45-12:10	T14-4 11:45-12:10
	Delft Univ. of Technology: A Class-D Piezoelectric Speaker Driver Using A Quadrature Feedback Chopping Scheme Achieving 29dB Large-Signal THD+N Improvement	Analog Photonics: A 2048-Channel, 125µW/ch DAC Controlling a 9,216-Element Optical Phased Array Coherent Solid-State LiDAR	KAIST: GPPU: A 330.4-µJ/task Neural Path Planning Processor with Hybrid GNN Acceleration for Autonomous 3D Navigation		Hitachi: Bumpless Build Cube (BBCube) 3D: Heterogeneous 3D Integration Using WoW and CoW to Provide TB/s Bandwidth with Lowest Bit Access Energy	imec: Integration of Epitaxial Monolayer MX_2 Channels on 300mm Wafers via Collective-Die-To-Wafer (CoD2W) Transfer
	C19-5 12:10-12:35	C20-5 12:10-12:35	C21-5 12:10-12:35		JFS4-5 12:10-12:35	T14-5 12:10-12:35
	Tokyo Institute of Technology: A Compact 0.9uW Direct-Conversion Frequency Analyzer for Speech Recognition with Wide-Range Q-Controlable Bandpass Rectifier	National Univ. of Singapore: Super-Cutoff Analog Building Blocks for pW/Stage Operation and Demonstration of 78-pW Battery-Less Light-Harvested Wake-Up Receiver down to Moonlight	KAIST: NeRPIM: A 4.2 mJ/frame Neural Rendering Processing-in-Memory Processor with Space Encoding Block-Wise Mapping for Mobile Devices		Semiconductor Energy Laboratory: 1Mbit 1T1C 3D DRAM with Monolithically Stacked One Planar FET and Two Vertical FET Heterogeneous Oxide Semiconductor Layers over Si CMOS	imec: Towards Low Damage and fab-Compatible Top-Contacts in MX_2 Transistors Using a Combined Synchronous Pulse Atomic Layer Etch and Wet-Chemical Etch Approach
12:35-14:00						
14:00-15:40	**JFS5: Automotive and Aerospace**	**C22: Advanced Imagers**	**C23: Short-Reach Links**		**T15: In-Memory Computing**	**T16: Logic Technology 3: Advanced Platforms and Processes**
	JFS5-1 14:00-14:25 (Invited)	C22-1 14:00-14:25	C23-1 14:00-14:25		T15-1 14:00-14:25	T16-1 14:00-14:25
	JAXA: How Harsh is Space?—Equations That Connect Space and Ground VLSI	CSEM: A 90 µW at 1 fps and 1.33 mW at 30 fps 120 dB Intra-Scene Dynamic Range 640 x 480 Stacked Image Sensor for Autonomous Vision Systems	Yonsei Univ.: A Low-Voltage Area-Efficient TSV I/O for HBM with Data Rate up to 15Gb/s Featuring Overlapped Multiplexing Driver, ISI Compensators and QEC		Macronix International: Chip Demonstration of a High-Density (43Gb) and High-Search-Bandwidth (300Gb/s) 3D NAND Based In-Memory Search Accelerator for Ternary Content Addressable Memory (TCAM) and Proximity Search of Hamming Distance	TSMC: Characterizing and Reducing the Layout Dependent Effect and Gate Resistance to Enable Multiple-Vt Scaling for a 3nm CMOS Technology
	JFS5-2 14:25-14:50 (Invited)	C22-2 14:25-14:50	C23-2 14:25-14:50		T15-2 14:25-14:50	T16-2 14:25-14:50
	Sandia: Enabling High-Speed, High-Resolution Space-Based Focal Plane Arrays with Analog In-Memory Computing	Prophesee: A 320 x 320 1/5" BSI-CMOS Stacked Event Sensor for Low-Power Vision Applications	NVIDIA: A 0.190-pJ/bit 25.2-Gb/s/wire Inverter-Based AC-Coupled Transceiver for Short-Reach Die-to-Die Interfaces in 5-nm CMOS		National Central Univ.: 3-Bits-Per-Cell $2T32C_{FE}$ nvTCAM by Angstrom-laminated Ferroelectric Layers with 10^{11} Cycles of Endurance and 4.92V of Ultra-Wide Memory-Windows for In-Memory-Searching	imec: Novel Low Thermal Budget CMOS RMG: Performance and Reliability Benchmark Against Conventional High Thermal Budget Gate Stack Solutions
	JFS5-3 14:50-15:15	C22-3 14:50-15:15	C23-3 14:50-15:15		T15-3 14:50-15:15	T16-3 14:50-15:15
	STMicroelectronics: ASIL-D Automotive-Grade Microcontroller in 28nm FD-SOI with Full-OTA Capable 21MB Embedded PCM Memory and Highly Scalable Power Management	Sony Semiconductor Solutions: An 0.08e$^-$-pJ/Step 14-bit Gain-Adaptive Single-Slope Column ADC with Enhanced HDR Function for High-Quality Imagers	Univ. of Illinois at Urbana-Champaign: A 5.2 Gb/s 3 mm Air-Gap 4.7 pJ/bit Capacitively-Coupled Transceiver for Giant Video Walls Enabled by a Dual-Edge Tracking Clock and Data Recovery Loop		TSMC: Write-Enhanced Single-Ended 11T SRAM Enabling Single Bitcell Reconfigurable Compute-In-Memory Employing Complementary FETs	Samsung Electronics: Highly Reliable/Manufacturable 4nm FinFET Platform Technology (SF4X) for HPC Application with Dual-CPP/HP-HD Standard Cells
		C22-4 15:15-15:40	C23-4 15:15-15:40		T15-4 15:15-15:40	T16-4 15:15-15:40
		vivo Mobile Communication: A 60fps 9.9nJ/frame·pixel CMOS Image Sensor with On-Chip Pixel-Wise Conversion Gain Modulation for Per-Frame Adaptive DCG-HDR Imaging	Texas A&M Univ.: A Sub-500fJ/bit 3D Direct Bond Silicon Photonic Transceiver in 12nm FinFET		Tsinghua Univ.: Monolithic 3D Integration of FeFET, Hybrid CMOS Logic and Analog RRAM Array for Energy-Efficient Reconfigurable Computing-In-Memory Architecture	National Taiwan Univ.: Extremely High-κ $Hf_{0.2}Zr_{0.8}O_2$ Gate Stacks Integrated into $Ge_{0.95}Si_{0.05}$ Nanowire and Nanosheet nFETs Featuring Respective Record I_{ON} per Footprint of 9200µA/µm and Record I_{ON} per Stack of 360µA at V_{OV}=V_{DS}=0.5V
16:00-18:05	**C24: Sensor Circuits and Systems**	**C25: Power and Security Control Systems**	**C26: Frequency Generation**	**T17: New Channel Material 3: IGZO**	**T18: DRAM/MRAM**	**TFS2: BEOL/BSPDN**
	C24-1 16:00-16:25	C25-1 16:00-16:25	C26-1 16:00-16:25	T17-1 16:00-16:25	T18-1 16:00-16:25	TFS2-1 16:00-16:25 (Invited)
	Harvard Univ.: A Wideband CMOS NMR Spectrometer for Multinuclear Molecular Fingerprinting	Northwestern Univ.: Proactive Power Regulation with Real-Time Prediction and Fast Response Guardband for Fine-Grained Dynamic Voltage Droop Mitigation on Digital SoCs	The Univ. of Tokyo: A Reference-Sampling PLL with Low-Ripple Double-Sampling PD Achieving −80-dBc Reference Spur and −259-dB FoM with 12-pF Input Load	National Univ. of Singapore: Overcoming Negative nFET V_{TH} by Defect-Compensated Low-Thermal Budget ITO-IGZO Hetero-Oxide Channel to Achieve Record Mobility and Enhancement-Mode Operation	Samsung Electronics: 14nm DRAM Development and Manufacturing	Intel: Novel Cell Architectures with Back-side Transistor Contacts for Scaling and Performance
	C24-2 16:25-16:50	C25-2 16:25-16:50	C26-2 16:25-16:50	T17-2 16:25-16:50	T18-2 16:25-16:50	TFS2-2 16:25-16:50 (Invited)
	Yonsei Univ.: A Highly-Digital PWM-Based Impedance Monitoring IC with 143.2dB DR and 17.7fF_{rms} Resolution	Intel: A 2.6 mV/b Resolution, 1.2 GHz Throughput, All-Digital Voltage Droop Monitor Using Coupled Ring Oscillators in Intel 4 CMOS	Samsung Electronics: A 2.4-to-4.2GHz 440.2fs_{rms}-Integrated-Jitter 4.3mW Ring-Oscillator-Based PLL Using a Switched-Capacitor-Bias-Based Sampling PD in 4nm FinFET CMOS	Purdue Univ.: First Demonstration of BEOL-Compatible Atomic-Layer-Deposited InGaZnO TFTs with 1.5 nm Channel Thickness and 60 nm Channel Length Achieving ON/OFF Ratio Exceeding 10^{11}, SS of 68 mV/dec, Normal-Off Operation and High Positive Gate Bias Stability	Xi'an UniIC Semiconductors: A 135 GBps/Gbit 0.66 pJ/bit Stacked Embedded DRAM with Multilayer Arrays by Fine Pitch Hybrid Bonding and Mini-TSV	imec: Nano-Through Silicon Vias (nTSV) for Backside Power Delivery Networks (BSPDN)
	C24-3 16:50-17:15	C25-3 16:50-17:15	C26-3 16:50-17:15	T17-3 16:50-17:15	T18-3 16:50-17:15	TFS2-3 16:50-17:15
	Rice Univ.: A 36nW CMOS Temperature Sensor with <0.1K Inaccuracy and Uniform Resolution	National Univ. of Singapore: Self-Referenced Design-Agnostic Laser Voltage Probing Attack Detection with 100% Protection Coverage, 58% Area Overhead for Automated Design	MediaTek: A 6nW 30.8kHz Relaxation Oscillator with Sampling Bias-Free RC Circuit and Dynamic Power Scaling in a 12nm FinFET	National Taiwan Univ.: First Demonstration of a-IGZO GAA Nanosheet FETs Featuring Achievable SS=61 mV/dec, I_{off}<10^{-2}µA/µm, DIBL=44 mV/V, Positive V_t, and Process Temp. of 300°C	KAIST: Epitaxial Strain Control of $Hf_xZr_{1-x}O_2$ with Sub-nm IGZO Seed Layer Achieving EOT=0.44 nm for DRAM Cell Capacitor	Applied Materials: BEOL Interconnect Innovation: Materials, Process and Systems Co-Optimization for 3nm Node and Beyond
	C24-4 17:15-17:40	C25-4 17:15-17:40	C26-4 17:15-17:40	T17-4 17:15-17:40	T18-4 17:15-17:40	TFS2-4 17:15-17:40
	National Univ. of Singapore: 38.4-pW, 0.14-mm^2 Body-Driven Temperature-to-Digital Converter and Voltage Reference with 0.6-1.6-V Unregulated Supply for Battery-Less Systems	National Univ. of Singapore: Visual Content-Agnostic Novelty Detection Engine with 2.4 pJ/pixel Energy and Two-Order of Magnitude DNN Activity Reduction in 40 nm	Fudan Univ.: A 50µW Ring-Type Complementary Inverse-Class-D Oscillator with 191.4dBc/Hz FoM and 205.6dBc/Hz FoM_A	SK hynix: Demonstration of Crystalline IGZO Transistor with High Thermal Stability for Memory Applications	Samsung Electronics: Highly Reliable and Manufacturable MRAM Embedded in 14nm FinFET Node	imec: Block-Level Evaluation and Optimization of Backside PDN for High-Performance Computing at the A14 Node
	C24-5 17:40-18:05	C25-5 17:40-18:05	C26-5 17:40-18:05	T17-5 17:40-18:05	T18-5 17:40-18:05	TFS2-5 17:40-18:05
	Delft Univ. of Technology: A 720 nW Current Sensor with 0-to-15V Input Common-Mode Range and ±0.5% Gain Error from -40 to 85 °C	National Univ. of Singapore: Voltage Scaling-Agnostic Counteraction of Side-Channel Neural Net Reverse Engineering via Machine Learning Compensation and Multi-Level Shuffling	KAIST: A 122fs_{rms}-Jitter and −60dBc-Reference-Spur 12.24GHz MDLL with a 102-Multiplication Factor Using a Power-Gating Technique	imec: Lowest I_{OFF} < 3×10^{-21} A/µm in Capacitorless DRAM Achieved by Reactive Ion Etch of IGZO-TFT	National Yang Ming Chiao Tung Univ.: U-MRAM: Transistor-Less, High-Speed (10 ns), Low-Voltage (0.6 V), Field-Free Unipolar MRAM for High-Density Data Memory	Samsung Electronics: Structural Reliability and Performance Analysis of Backside PDN