Simplified Four-Level Inverter based Single-Phase DSTATCOM Using Model Predictive Control

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***Abstract*— The conventional two-level inverter based distribution static compensator (DSTATCOM) requires high switching frequency and fast digital signal processors (DSPs) to obtain smaller voltage/current ripples and low total harmonic distortion (THD). This increases the switching loss and computational burden. To solve such problems, this paper proposes a simplified four-level (S4L) inverter based DSTATCOM. The proposed inverter has a two-stage structure. The first stage produces three different voltage levels of full, two thirds, and one third of DC link voltage. These voltage levels are supplied to the second stage two-level inverter. Together with the zero voltage produced by the two-level inverter, the output of the proposed inverter can be four levels. With the same switching frequency and computational time, the S4L inverter based DSTATCOM achieves much better performance than the conventional ones. Moreover, compared with the existing multilevel inverter based DSTATCOMs, it is more cost-effective. To further enhance its performance, model predictive control (MPC) is employed. Experimental results are presented to verify the validity of the proposed system.**

***Index Terms*— Single-phase distribution static compensator (DSTATCOM), simplified four-level (S4L) inverter, total harmonic distortion (THD), model predictive control (MPC).**

I. INTRODUCTION

IN the modern power system, more and more nonlinear loads are integrated [1]. These types of loads will degrade the power factor at the source. The power factor plays a crucial role in the power transmission system [2]-[5]. To transfer a certain amount of electrical power, the current magnitude on the transmission line is higher under a lower power factor [2], [4]. The size of the transmission line conductor has to be increased accordingly in order to handle the higher current magnitude. It will increase the manufactural cost of the transmission system. Therefore, it is important to maintain a unity power factor at the source side.

Among all the power factor correction devices, the distribution static compensator (DSTATCOM) is one of the most comprehensive devices to solve this problem [6]. A typical DSTATCOM consists of a two-level voltage source inverter (VSI), a DC link capacitor and an inductor. The working principle of the DSTATCOM is to inject a current of specific phase angle and magnitude into the distribution line, so that the source current is regulated at the rated sinusoidal waveform and in phase with the source voltage [6].

In [6], the authors apply the H-bridge cascaded multilevel inverter to achieve four-level voltage output of the DSTATCOM. Each phase requires three cascaded H-bridge modules. The DC voltage magnitude of each module is identical. In [7], the photovoltaic array is used to support the DC link of the DSTATCOM. In addition to the power quality compensation ability, the PV-DSTATCOM can also supply power to the grid and the connected load. The inverter applied in the PV- DSTATCOM is the conventional two-level inverter. In [8], the DSTATCOM is operated in the voltage control mode. A detailed design procedure for selecting the external inductor is also carried out. In [9], the DSTATCOM is used to compensate the reactive power and harmonics in a constant speed turbine based induction generator. In [10], an *LCL* filter is utilized at the front end of the two-level converter. The inductance value of the *LCL* filter is smaller than that of the *L* filter. In [11], the JAYA optimization algorithm is adopted to calculate the gains of the PI controller and filter parameters in the PV-DSTATCOM. In [12], the leaky least mean fourth algorithm is used to extract the fundamental component from the load current in the controller of PV- DSTATCOM. In [13], the combined least mean square–least mean fourth algorithm is applied to generate the reference source current. In [14], the frequency-adaptive disturbance observer is used to eliminate the harmonic components in the load current. In [15], the authors discuss the current control mode and voltage control mode of the DSTATCOM. In [16], an immune feedback control method is developed to increase the convergence speed and reduce the computational complexity in the controller of the DSTATCOM. In [17], a second-order Volterra-filter-based control algorithm is utilized in the PV-DSTATCOM. By applying this algorithm, the error of the system can exponentially converge to zero asymptotically. In [18], the i-PNLMS algorithm is adopted in the DSTATCOM. Compared with the conventional normalized least mean square algorithm, the i-PNLMS algorithm can provide faster convergence and less steady-state error. In [19], a reduced switch count multilevel converter is used in the DSTATCOM to gradually adjust the DC link voltage according to the different load conditions. In [20], the Chebyshev functional expansion based artificial neural network algorithm is applied in the DSTATCOM to increase the convergence speed and reduce the computational effort in the controller. In [21], an adaptive neurofuzzy inference system least mean square-based control algorithm is developed for the DSTATCOM. This algorithm is used to extract the sinusoidal reference current from the distorted load current. In [22], the neural network is applied in the DSTATCOM to generate the reference source voltage based on load conductance estimation.

It is reported in literatures that high switching frequency is generally needed to maintain low harmonics in the source current, implying high switching loss. Accordingly, the sample time of the digital signal processor (DSP) must be made small enough to cope with the high switching frequency. This unavoidably increases the computational burden of DSP. Therefore, in practical applications, a lower switching frequency of the power converter is preferred.

In the conventional two-level inverter based DSTATCOM topology, the DC side can only provide a full DC link voltage. When the magnitude of the required output voltage of the full-bridge inverter is small, the full DC link voltage will introduce undesired harmonics into the source current. One solution to the problem is employing multilevel inverter, which is capable of producing improved power quality and low total harmonic distortion (THD). The multilevel inverter can provide good harmonic mitigation performance with a low operating switching frequency. For example, in [6], the H-bridge cascaded multilevel inverter is applied to achieve four-level voltage output of the DSTATCOM. The sampling time is 100 μs and the switching frequency is 5 kHz in [6]. In [23] and [24], the flying capacitor multilevel inverter (FCMLI) and the diode-clamped multilevel inverter (DCMLI) are applied in DSTATCOM to provide three-level voltage for the inverter output. The three-level neutral point clamped (3L-NPC) inverter is also a commonly utilized topology in the DSTATCOM [25]-[27]. The 3L-NPC inverter can also output three-level voltage. The T-type converter is also a popular multilevel converter to provide three voltage levels [28]. The T-type converter does not need additional diodes compared to the NPC converter. The required components of the aforementioned two-level, three-level and four-level inverters are summarized in Table I. It is noted that the H-bridge cascaded four-level inverter can provide the lowest THD. However, it requires more components compared with other topologies, which makes it not a cost-effective solution. The three-level inverters cannot provide the same performance as the H-bridge cascaded four-level inverter. Hence, both the three-level inverters and the H-bridge cascaded four-level inverter are not the best solution for the DSTATCOM in terms of cost and performance.

In this paper, we attempt to use a new simplified four-level (S4L) inverter in the DSTATCOM. This new S4L inverter does not require additional components compared with the three-level inverters. Meanwhile, it can output four-level voltage. The proposed S4L inverter is based on a three-level simplified NPC inverter [29]-[31], which comprises a dual buck converter and a conventional two-level inverter as presented in Fig. 1. In the three-level simplified NPC inverter, the dual buck converter only generates two voltage levels ($+V_{dc}$, $+V_{dc}/2$) from the full DC link voltage V_{dc}. It is still a three-level inverter. In the proposed S4L inverter, the dual buck converter can generate three voltage levels ($+V_{dc}$, $+2V_{dc}/3$, $+V_{dc}/3$). Including the zero voltage generated by the two-level inverter, the output voltages of the proposed inverter are four levels ($+V_{dc}$, $+2V_{dc}/3$, $+V_{dc}/3$, 0). Thus, more options of the output voltage can be provided, when the magnitude of the required voltage is relatively small. In this way, the problem can be significantly alleviated and the generated current harmonics can be effectively suppressed. Furthermore, the four-level inverter based DSTATCOM is more cost-effective, as it requires less components compared with other multilevel topologies. The voltage rating and switching losses of the switches in the proposed S4L inverter are compared with the commonly used T-type inverter in Appendix A and Appendix B, respectively.

To optimize the control of the S4L inverter based DSTATCOM, model predictive control (MPC) technique is adopted in this paper. The MPC is able to offer smooth transient performance and fast dynamics response [32]-[37].

The contribution of this paper is summarized as follows:

1) The S4L inverter based DSTATCOM requires less

TABLE I
COMPARISON OF PERFORMANCE AND REQUIRED COMPONENTS OF THE TWO-LEVEL, THREE-LEVEL AND FOUR-LEVEL INVERTERS IN SINGLE-PHASE DSTATCOMS

	Topology	THD	Switching frequency	Number of active switches	Number of diodes	Number of DC link capacitors
Two-level	H-bridge [7]	High	High	4	4	1
Three-level	FCMLI [23]	medium	medium	8	8	5
	DCMLI [24]	medium	medium	8	14	4
	NPC [26]	medium	medium	8	12	2
	SNPC [29]	medium	medium	8	8	2
	T-type [28]	medium	medium	8	8	2
Four-level	H-bridge cascaded [6]	Low	Low	12	12	3
	Proposed S4L	Low	Low	8	8	2

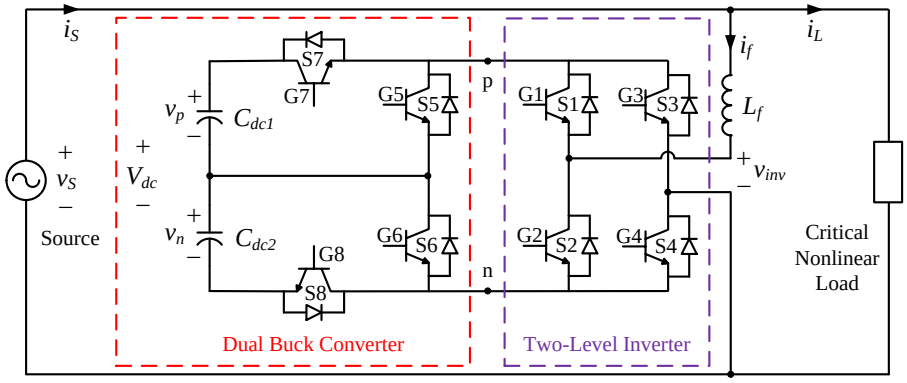


Fig. 1. Topology of S4L inverter based single-phase DSTATCOM.

components compared with the commonly used multilevel inverter based DSTATCOMs. It is a more cost-effective solution for source current compensation.

2) Compared with the commonly used three-level inverter, the S4L inverter can output four-level voltages without adding additional components. The harmonics in the source current can be mitigated.

The rest of this paper is arranged as follows. The detailed topology and the discrete-time model of the S4L inverter based DSTATCOM are presented in Section II. Using the derived discrete-time model, the MPC based controller is designed in Section III. Section IV shows the experimental results of the laboratorial prototype. Section V concludes this paper.

II. Topology of S4L Inverter Based DSTATCOM

A. System Topology

Fig. 1 shows the topology of the S4L inverter based single-phase DSTATCOM. i_S, i_L and i_f are the source current, load current and inductor current, respectively. v_S is the source voltage. V_{dc} is the total DC link voltage. v_p and v_n represent the upper and lower arm voltages. It can be observed from the topology illustrated in Fig. 1, the S4L inverter based single-phase DSTATCOM consists of a two-level inverter (S1, S2, S3 and S4), a dual buck converter (S5, S6, S7 and S8), two DC capacitors (C_{dc1} and C_{dc2}) and an inductor (L_f).

As mentioned previously, the dual buck converter is responsible for generating the three voltage levels ($+V_{dc}$, $+2V_{dc}/3$, $+V_{dc}/3$) from the full DC link voltage V_{dc}. These voltage levels are obtained from the switching combinations of S5, S6, S7 and S8 tabulated in Table II. It is obvious that if the voltages across the two capacitors C_{dc1} and C_{dc2} can be maintained at $+2V_{dc}/3$ and $+V_{dc}/3$, the terminal voltage v_{pn} of the dual buck converter is $+V_{dc}$, $+2V_{dc}/3$, $+V_{dc}/3$). Including the zero voltage generated by the two-level inverter, the output voltages v_{inv} of the proposed inverter are four levels ($+V_{dc}$, $+2V_{dc}/3$, $+V_{dc}/3$, 0). Symmetrically, the negative part of v_{inv} is also four-level ($-V_{dc}$, $-2V_{dc}/3$, $-V_{dc}/3$, 0).

TABLE II
Switching Combinations and Terminal Voltage of Dual Buck Converter

Switching Combinations				Terminal Voltage
S5	S6	S7	S8	v_{pn}
0	0	1	1	$+V_{dc}$
0	1	1	0	$+v_p = +2V_{dc}/3$
1	0	0	1	$+v_n = +V_{dc}/3$

B. Discrete-Time Model

Fig. 2 illustrates the equivalent circuit of the S4L inverter based single-phase DSTATCOM. The output voltage of the four-level inverter is derived as

$$v_{inv} = uV_{dc} \tag{1}$$

where u is the switching variable. Based on the output voltage of the two-level inverter, it can be obtained that $u \in \{1, 2/3, 1/3, 0, -1/3, -2/3, -1\}$.

In Fig. 2, the following equations describe the dynamics of the S4L inverter based single-phase DSTATCOM.

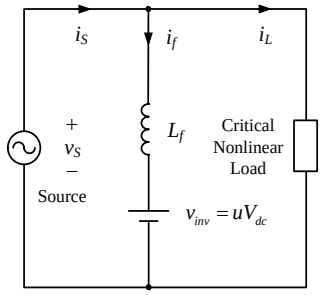


Fig. 2. Equivalent circuit of S4L inverter based single-phase DSTATCOM.

$$v_{inv} + L_f \frac{di_f}{dt} - v_S = 0 \tag{2}$$

$$i_L + i_f - i_S = 0 \tag{3}$$

When $t = k + 1$, the discretization of (2) is realized by utilizing the forward-Euler method as

$$i_f(k+1) = i_f(k) + \frac{T_S}{L_f} v_S(k) - \frac{T_S}{L_f} v_{inv}(k) \tag{4}$$

where T_S is the sampling time. Due to a small value of T_S, the values of the sensed signals i_L and v_S are treated as constant in two subsequent sampling instants. Then we obtain the equations as follows:

$$i_L(k+1) = i_L(k) \tag{5}$$

$$v_S(k+1) = v_S(k) \tag{6}$$

From (3), we can obtain that

$$i_S(k+1) = i_f(k+1) + i_L(k+1) \tag{7}$$

Substitute (4) and (5) into (7), Equation (7) is rewritten as

$$i_S(k+1) = i_f(k) + \frac{T_S}{L_f} v_S(k) - \frac{T_S}{L_f} v_{inv}(k) + i_L(k) \tag{8}$$

Using (4), (5), (6) and (8), the state-space model of the S4L inverter based single-phase DSTATCOM is derived as

$$x(k+1) = Ax(k) + Bu(k) \tag{9}$$

$$y(k) = Cx(k) \tag{10}$$

where

$$A = \begin{bmatrix} 1 & \frac{T_S}{L_f} & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 1 & \frac{T_S}{L_f} & 0 & 1 \\ 0 & 0 & 0 & 1 \end{bmatrix};\ B = \begin{bmatrix} -\frac{T_S V_{dc}}{L_f} \\ 0 \\ -\frac{T_S V_{dc}}{L_f} \\ 0 \end{bmatrix};\ C = \begin{bmatrix} 0 & 0 & 1 & 0 \end{bmatrix};$$

$x(k) = [i_f(k)\ v_S(k)\ i_S(k)\ i_L(k)]^T$ represents the vector of the state variables; $u(k)$ represents the switching variables, i.e., the control input in MPC; $y(k) = i_S(k)$ is the system output. Then the system output can be regulated to track the reference signal. In this work, it is the source current reference.

III. MPC Based Controller Design

Due to the superior performance in power electronic devices [31]-[36], the MPC method is utilized to control the S4L in-

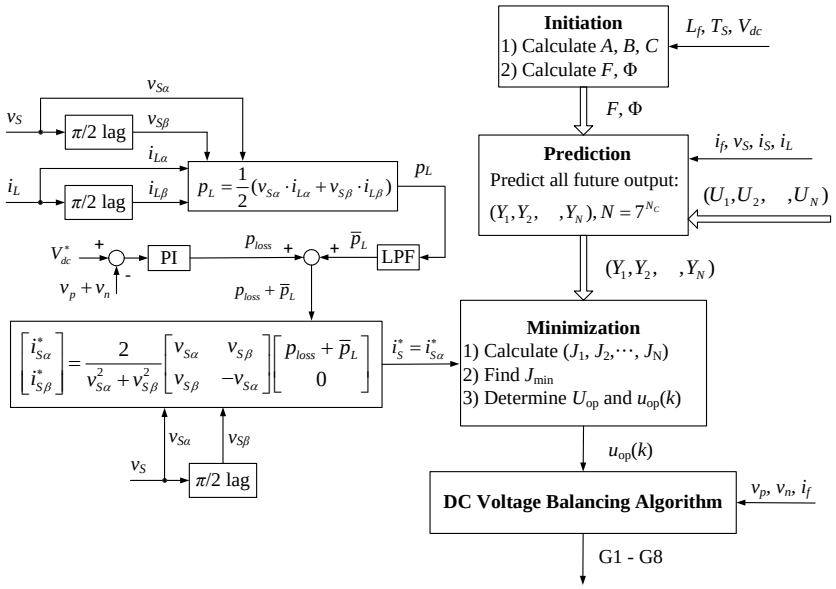


Fig. 3. Block diagram of control for S4L inverter based single-phase DSTATCOM.

verter based single-phase DSTATCOM. Using the discrete-time model derived in Section II.B, the controller is designed in this section.

A. Reference Generation for Source Current

At the left-hand side of Fig. 3, the reference generation for the source current is illustrated. By using the p-q theory [38], v_S is selected as the α-axis quantity $v_{S\alpha}$. Then a $\pi/2$ lag of v_S is conducted to obtain the β-axis quantity $v_{S\beta}$. Similarly, the $\alpha\beta$-axis quantities $i_{L\alpha}$ and $i_{L\beta}$ are obtained from i_L. Applying Akagi's p-q theory [34], the load active power is computed as

$$p_L = \frac{1}{2}(v_{S\alpha} \cdot i_{L\alpha} + v_{S\beta} \cdot i_{L\beta}) \tag{11}$$

The fundamental load active power $\bar{p}_L$ can be tracked by applying a low pass filter (LPF). The error between the reference and actual total DC link voltages is processed by a proportional integral (PI) controller to obtain the power loss p_{loss}, which is associated with maintaining the DC-link voltage. As the source only supports the fundamental load active power and the power loss, $p_{loss} + \bar{p}_L$ is used to calculate the $\alpha\beta$-axis quantities of i_S as

$$\begin{bmatrix} i_{S\alpha}^* \\ i_{S\beta}^* \end{bmatrix} = \frac{2}{v_{S\alpha}^2 + v_{S\beta}^2} \begin{bmatrix} v_{S\alpha} & v_{S\beta} \\ v_{S\beta} & -v_{S\alpha} \end{bmatrix} \begin{bmatrix} p_{loss} + \bar{p}_L \\ 0 \end{bmatrix} \tag{12}$$

where $i_{S\alpha}^*$ is the desired reference signal for the source current, i.e., $i_S^* = i_{S\alpha}^*$.

B. Minimize Cost Function of MPC

The predictive current control algorithm can maintain the source current at the desired value in the condition of the distorted load current. Thus, the error between the reference and predicted source currents should be minimized in the MPC scheme. In order to obtain the minimum error, we apply a cost function, in which N_p and N_c are the predict horizon and control horizon, respectively. The MPC will apply N_c number of control variables ($u(k)$, $u(k + 1)$, ⋯, $u(k + N_c - 1)$) to predict N_p number of future output variables ($y(k + 1)$, $y(k + 2)$, ⋯, $y(k + N_p)$). We define the cost function J as

$$J = (Y - R)^T (Y - R) \tag{13}$$

where $Y = [i_S(k + 1)\ i_S(k + 2) \ldots i_S(k + N_p)]^T$; $R = [\underbrace{1\ 1 \ldots 1}_{N_P}]^T\ i_S^*(k)$;

and $i_S^*(k)$ represents the reference of source current. Y is computed as [36]

$$Y = Fx(k) + \Phi U \tag{14}$$

where $U = [u(k)\ u(k + 1) \cdots u(k + N_c - 1)]^T$;

$$F = \begin{bmatrix} CA \\ CA^2 \\ CA^3 \\ \mathrm{M} \\ CA^{N_P} \end{bmatrix};$$

$$\Phi = \begin{bmatrix} CB & 0 & 0 & \mathrm{L} & 0 \\ CAB & CB & 0 & \mathrm{L} & 0 \\ CA^2B & CAB & CB & \mathrm{L} & 0 \\ \mathrm{M} & \mathrm{M} & \mathrm{M} & \mathrm{O} & \mathrm{M} \\ CA^{N_P-1}B & CA^{N_P-2}B & CA^{N_P-3}B & \mathrm{L} & CA^{N_P-N_C}B \end{bmatrix}$$

As u has seven possible control actions (1, 2/3, 1/3, 0, -1/3, -2/3, -1), all possible control actions of U are $(U_1, U_2, \mathrm{L}\ , U_N)$, where $N = 7^{N_C}$. The future output $(Y_1, Y_2, \mathrm{L}\ , Y_N)$ are computed utilizing (14) and the possible control actions of U. Then, $(Y_1, Y_2, \mathrm{L}\ , Y_N)$ and R are substituted into (13) to obtain the values of objective function $(J_1, J_2, \mathrm{L}\ , J_N)$. The minimal value $J_{\min}$ can be found. Then, $J_{\min}$ corresponds to the optimal control action U_{op}, which obtains the minimum error. The present control action is the first control action of U_{op}, i.e.,

TABLE IV
SWITCHING COMBINATIONS OF S4L INVERTER BASED SINGLE-PHASE DSTATCOM

Error of DC Voltages	Present Control Action	Inductor Current	Dual Buck Converter Terminal Voltage	Full-bridge Inverter Output Voltage	Switching Combinations							
Δ	$u_{op}(k)$	i_f	v_{pn}	v_{inv}	S1	S2	S3	S4	S5	S6	S7	S8
$\Delta > V_{dc}/3+\delta$	$u_{op}(k) > 0$	$i_f \geq 0$	$+v_n$	$+v_n$	1	0	0	1	1	0	0	1
$\Delta > V_{dc}/3+\delta$	$u_{op}(k) > 0$	$i_f < 0$	$+v_p$	$+v_p$	1	0	0	1	0	1	1	0
$\Delta > V_{dc}/3+\delta$	$u_{op}(k) < 0$	$i_f \geq 0$	$+v_p$	$-v_p$	0	1	1	0	0	1	1	0
$\Delta > V_{dc}/3+\delta$	$u_{op}(k) < 0$	$i_f < 0$	$+v_n$	$-v_n$	0	1	1	0	1	0	0	1
$\Delta < V_{dc}/3-\delta$	$u_{op}(k) > 0$	$i_f \geq 0$	$+v_p$	$+v_p$	1	0	0	1	0	1	1	0
$\Delta < V_{dc}/3-\delta$	$u_{op}(k) > 0$	$i_f < 0$	$+v_n$	$+v_n$	1	0	0	1	1	0	0	1
$\Delta < V_{dc}/3-\delta$	$u_{op}(k) < 0$	$i_f \geq 0$	$+v_n$	$-v_n$	0	1	1	0	1	0	0	1
$\Delta < V_{dc}/3-\delta$	$u_{op}(k) < 0$	$i_f < 0$	$+v_p$	$-v_p$	0	1	1	0	0	1	1	0
$V_{dc}/3-\delta \leq \Delta \leq V_{dc}/3+\delta$	$u_{op}(k) = 1$		$+V_{dc}$	$+V_{dc}$	1	0	0	1	0	0	1	1
$V_{dc}/3-\delta \leq \Delta \leq V_{dc}/3+\delta$	$u_{op}(k) = -1$		$+V_{dc}$	$-V_{dc}$	0	1	1	0	0	0	1	1
$V_{dc}/3-\delta \leq \Delta \leq V_{dc}/3+\delta$	$u_{op}(k) = 2/3$		$+v_p$	$+v_p$	1	0	0	1	0	1	1	0
$V_{dc}/3-\delta \leq \Delta \leq V_{dc}/3+\delta$	$u_{op}(k) = -2/3$		$+v_p$	$-v_p$	0	1	1	0	0	1	1	0
$V_{dc}/3-\delta \leq \Delta \leq V_{dc}/3+\delta$	$u_{op}(k) = 1/3$		$+v_n$	$+v_n$	1	0	0	1	1	0	0	1
$V_{dc}/3-\delta \leq \Delta \leq V_{dc}/3+\delta$	$u_{op}(k) = -1/3$		$+v_n$	$-v_n$	0	1	1	0	1	0	0	1
	$u_{op}(k) = 0$		$+V_{dc}$	0	1	0	1	0	0	0	1	1

$u_{op}(k)$. The aforementioned procedure has been summarized in Fig. 3.

C. DC Voltage Balancing

In order to maintain v_p and v_n at $2V_{dc}/3$ and $V_{dc}/3$, respectively, a DC voltage Balancing algorithm is applied in the controller. The error between the upper arm and lower arm voltages can be defined as follows:

$$\Delta = v_p - v_n \tag{15}$$

A threshold δ is utilized to guarantee the voltage balance. Thus, Δ should be within the range of $[V_{dc}/3-\delta,\ V_{dc}/3+\delta]$. It is noted that the sum of v_p and v_n is maintained at the reference value by the PI controller. If $\Delta > V_{dc}/3+\delta$, it means v_p is higher than its upper boundary and v_n is lower than its lower boundary. The voltages can be balanced by charging v_n or discharging v_p. If $\Delta < V_{dc}/3-\delta$, it means v_p is lower than its lower boundary and v_n is higher than its higher boundary. The voltages can be balanced by charging v_p or discharging v_n. If $\Delta \in [V_{dc}/3-\delta,\ V_{dc}/3+\delta]$, the switching combinations just follow the calculated $u_{op}(k)$. When $u_{op}(k) = 0$, the output voltage of the S4L inverter should be zero. The detailed DC voltage balancing algorithm is presented in Table III. Based on the DC voltage balancing algorithm, the corresponding switching combinations are listed in Table IV.

TABLE III
DC VOLTAGE BALANCING ALGORITHM

Input $u_{op}(k)$, v_p, v_n and i_f
If $\Delta > V_{dc}/3+\delta$, $u_{op}(k) > 0$ and $i_f \geq 0$
Lower arm is charged; v_{inv} is positive.
If $\Delta > V_{dc}/3+\delta$, $u_{op}(k) > 0$ and $i_f < 0$
Upper arm is discharged; v_{inv} is positive.
If $\Delta > V_{dc}/3+\delta$, $u_{op}(k) < 0$ and $i_f \geq 0$
Upper arm is discharged; v_{inv} is negative.
If $\Delta > V_{dc}/3+\delta$, $u_{op}(k) < 0$ and $i_f < 0$
Lower arm is charged; v_{inv} is negative.
If $\Delta < V_{dc}/3-\delta$, $u_{op}(k) > 0$ and $i_f \geq 0$
Upper arm is charged; v_{inv} is positive.
If $\Delta < V_{dc}/3-\delta$, $u_{op}(k) > 0$ and $i_f < 0$
Lower arm is discharged; v_{inv} is positive.
If $\Delta < V_{dc}/3-\delta$, $u_{op}(k) < 0$ and $i_f \geq 0$
Lower arm is discharged; v_{inv} is negative.
If $\Delta < V_{dc}/3-\delta$, $u_{op}(k) < 0$ and $i_f < 0$
Upper arm is charged; v_{inv} is negative.
If $V_{dc}/3-\delta \leq \Delta \leq V_{dc}/3+\delta$ and $u_{op}(k) = 1$
Full DC link is connected; v_{inv} is positive.
If $V_{dc}/3-\delta \leq \Delta \leq V_{dc}/3+\delta$ and $u_{op}(k) = -1$
Full DC link is connected; v_{inv} is negative.
If $V_{dc}/3-\delta \leq \Delta \leq V_{dc}/3+\delta$ and $u_{op}(k) = 2/3$
Upper arm is connected; v_{inv} is positive.
If $V_{dc}/3-\delta \leq \Delta \leq V_{dc}/3+\delta$ and $u_{op}(k) = -2/3$
Upper arm is connected; v_{inv} is negative.
If $V_{dc}/3-\delta \leq \Delta \leq V_{dc}/3+\delta$ and $u_{op}(k) = 1/3$
Lower arm is connected; v_{inv} is positive.
If $V_{dc}/3-\delta \leq \Delta \leq V_{dc}/3+\delta$ and $u_{op}(k) = -1/3$
Lower arm is connected; v_{inv} is negative.
If $u_{op}(k) = 0$
$v_{inv} = 0$.
Output gate signals G1-G8

D. Design of System Parameters

Based on the equivalent circuit of the S4L inverter based single-phase DSTATCOM as presented in Fig. 2, the required full DC link voltage should be higher than the maximum source voltage to obtain the compensation current. Thus, the minimum full DC link voltage is calculated as

$$V_{dc(\min)} > \sqrt{2} v_{S(\mathrm{rms})} \tag{16}$$

where $v_{S(\mathrm{rms})}$ is the source nominal voltage.

The design of the DC link capacitor is based on the capability of regulating its voltage under the transient states. We assume the DSTSTCOM is connected to an S VA system. The variation of the energy during the transient is λS VA, where λ is the variation ratio. If the capacitor voltage changes from the reference value V_{dc} to V_{dck} during the transient, using the principle of energy conservation, the equation governing C_{dc} is written as

$$\frac{1}{2} C_{dc} \left(V_{dc}^2 - V_{dck}^2 \right) = \lambda S t_s \tag{17}$$

where t_s is the time for the capacitor voltage to be restored. As

the upper and lower arm capacitors are series connected, C_{dc1} and C_{dc2} can be calculated as

$$C_{dc1} = C_{dc2} = 2C_{dc} \tag{18}$$

As given in [39], the upper and lower limits of switching frequencies f_{upp} and f_{low} satisfy the following equations

$$f_{upp} = \frac{V_{dc}}{15.6hL_f} \tag{19}$$

$$f_{low} = \frac{V_{dc}}{32.1hL_f} \tag{20}$$

where h is the magnitude of the ripple current. The selection of the inductance L_f depends on V_{dc}, h, f_{upp} and f_{low}. According to IEEE recommended limits on harmonic current injected into the grid at the point of common coupling [5], the ripple current injection has to be lower than 0.3% of rated current of the system. h can be expressed as

$$h = \frac{S}{v_{S(rms)}} \cdot 0.3\% \tag{21}$$

Then L_f can be calculated as

$$L_f = \frac{V_{dc}}{K_{sw} h f_{sw}} \tag{22}$$

where $15.6 \le K_{sw} \le 32.1$ and $f_{low} \le f_{sw} \le f_{upp}$.

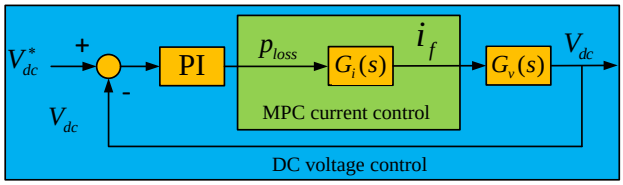


Fig. 4. Block diagram of control loop.

E. Design of PI Controller Gains

The block diagram of the control loop is shown in Fig. 4. It consists of the inner MPC based current control loop and the outer PI controller based DC voltage control loop. It has to be mentioned that the dynamics of the MPC based current control is much faster than that of the PI controller based DC voltage control. The transfer function of the PI controller is given by

$$H(s) = K_p + \frac{K_i}{s} \tag{23}$$

As the MPC based current control has much faster dynamics compare with the PI controller based DC voltage control, the transfer function $G_i(s)$ can be considered as one when we design the outer PI controller. Hence, we can have

$$G_i(s) = 1 \tag{24}$$

The dynamics of the DC link capacitor can be described by the following equation.

$$V_{dc} = \frac{1}{C_{dc}} \int \left(i_f \, dt \right) \tag{25}$$

Based on (25), the transfer function of the outer DC voltage control loop is given as follows:

$$G_v(s) = \frac{\hat{V}_{dc}(s)}{\hat{i}_f(s)} = \frac{1}{sC_{dc}} \tag{26}$$

Using (23), (24) and (26), the system closed loop transfer function is calculated as follows:

$$\phi(s) = \frac{H(s)G_i(s)G_v(s)}{1 + H(s)G_i(s)G_v(s)} = \frac{K_p s + K_i}{C_{dc}s^2 + K_p s + K_i} \tag{27}$$

From (27), the system characteristic equation can be obtained as

$$C_{dc}s^2 + K_p s + K_i = 0 \tag{28}$$

In order to ensure the system is stable, the closed-loop poles should lie in the left half of s-plane. Thus, $K_p > 0$ and $K_i > 0$. However, the closed-loop poles in the left half of s-plane does not guarantee satisfactory transient response characteristics of the system. The values of K_p and K_i have to be designed considering the transient response characteristic of the system. The system characteristic equation can be rewritten as

$$s^2 + 2\xi\omega_n s + \omega_n^2 = 0 \tag{29}$$

Based on (28), the natural frequency ω_n and damping ratio ξ can be computed as

$$\omega_n = \sqrt{\frac{K_i}{C_{dc}}} \tag{30}$$

$$\xi = \frac{K_p}{2\sqrt{K_i C_{dc}}} \tag{31}$$

In order to avoid the overdamping, ξ should satisfy

$$0 < \xi \le 1 \tag{32}$$

Substitute (31) into (32), the relation between K_p and K_i can be described as

$$0 < \frac{K_p^2}{4C_{dc}} \le K_i \tag{33}$$

IV. Experimental Results

The experimental study is carried out to verify the performance of the S4L inverter based DSTATCOM. A downscaled laboratorial prototype has been built as illustrated in Fig. 5. The CREE MOSFETs based half-bridge modules are applied for the dual-buck converter and full-bridge inverter. Two DC capacitors are connected at the DC link of the dual buck converter. The dSPACE 1202 is applied as the DSP. A Lecroy oscilloscope is used to capture the waveforms. A *RLC* circuit is connected through a diode bridge rectifier as a nonlinear load. The nonlinear load configuration is shown in Fig. 6. A *RL* circuit is series connected as a linear load. The system is originally operated under the linear load condition. Then the load side is switched from the linear load to the nonlinear load. The solid state relays are used for the load step change.

A. Calculation of System Parameters

The supply voltage is at the rated frequency and magnitude (50 Hz and 110 V) for the downscaled system. Using (16), $V_{dc(min)}$ should be high than $110 \times \sqrt{2} = 115.5$ V. Thus, the full DC link voltage is chosen as 160 V. Considering a 550 VA system, i.e., S = 550, variation ratio λ is 0.3, the capacitor voltage changes from 160 V to 140 V during the transient, and t_s = 0.02 s, using (17) C_{dc} is calculated as 1100 μF. Then using

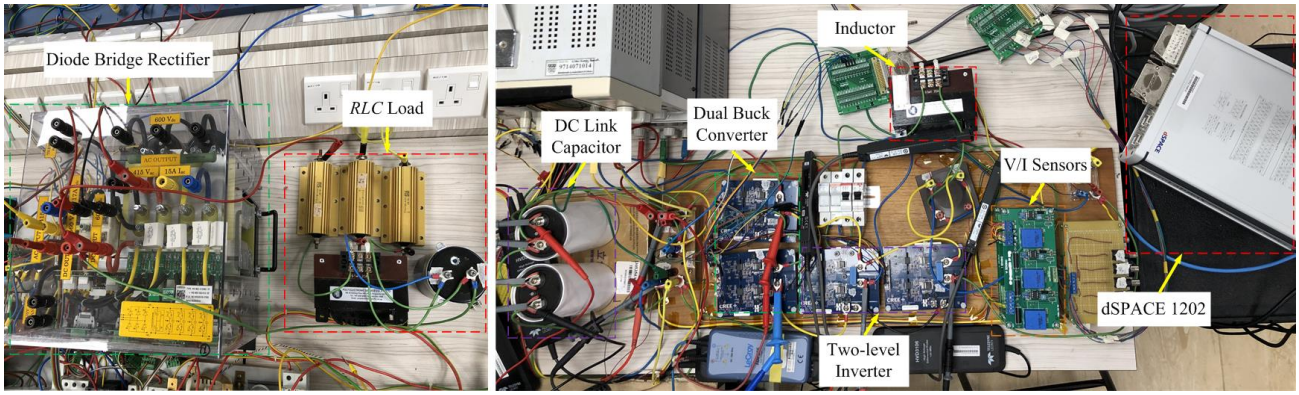


Fig. 5. Laboratorial prototype of S4L inverter based DSTATCOM.

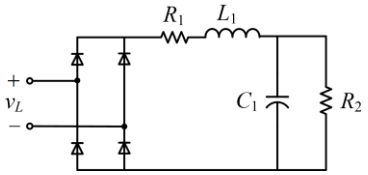


Fig. 6. Nonlinear load configuration.

TABLE V
SYSTEM PARAMETERS

Source nominal frequency and voltage	$v_{S(\text{rms})} = 110$ V $f_S = 50$ Hz
DC-link voltage	$V_{dc} = 160$ V
Nonlinear load	$R_1 = 20\ \Omega$ $L_1 = 6.5$ mH $R_2 = 20\ \Omega$ $C_1 = 3900\ \mu$F
Linear load	$R_3 = 20\ \Omega$ $L_2 = 18$ mH
Inductor	$L_f = 6.5$ mH
DC-link capacitor	$C_{dc1} = 2200\ \mu$F $C_{dc2} = 2200\ \mu$F
Sampling time	$T_s = 40\ \mu s; 100 \mu s$
Switching frequency	$f_{\text{upp}} = 25$ kHz $f_{\text{low}} = 10$ kHz
Dead time	$t_d = 2\ \mu s$
Predict horizon and control horizon	$N_p = 2$ $N_c = 2$
Threshold	$\delta = 15$ V
LPF cut-off frequency	$f_c = 30$ Hz

TABLE VI
PI CONTROLLER GAINS AND STEP RESPONSE DYNAMIC PERFORMANCE INDEX

K_p	0.38
K_i	88.10
Damping ratio	$\xi = 0.61$
Response time	$t_r = 2.5$ ms
Overshoot percentage	$\sigma\% = 22\%$
Settling time	$t_s = 20$ ms

(18), $C_{dc1} = C_{dc2} = 2200\ \mu$F. In this experiment, we manage to operate the inverter of the system at two different switching frequencies 25 kHz and 10 kHz to validate the feasibility of the proposed S4L inverter based DSTATCOM. Thus, $f_{\text{upp}} = 25$ kHz and $f_{\text{low}} = 10$ kHz. Using (21) and (22), L_f is calculated as 33.2 mH and 27.4 mH under $f_{\text{sw}} = f_{\text{low}}$ and $f_{\text{sw}} = f_{\text{upp}}$, respectively. Then L_f can be chosen as 30 mH. It has to be mentioned that 30 mH is for convention two-level inverter based DSTATCOM.

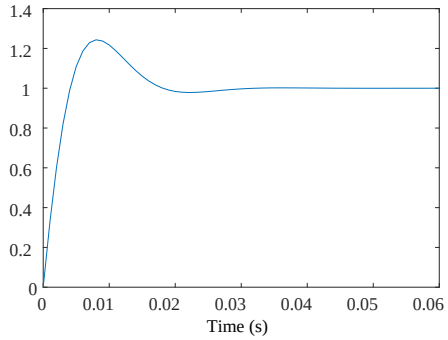


Fig. 7. Step response of DC link control

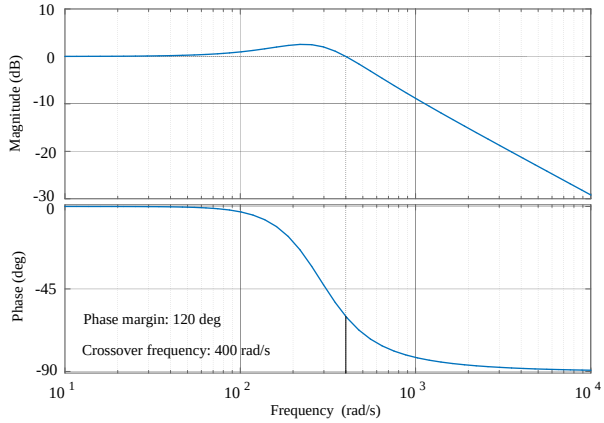
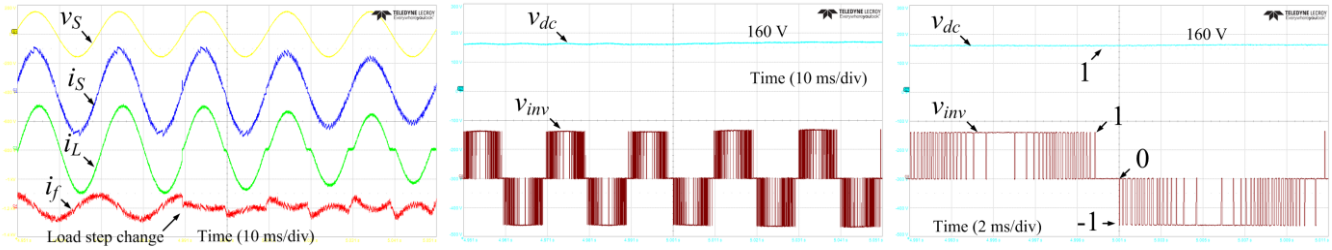


Fig. 8. Bode plot of closed loop transfer function ϕ(s) for DC link voltage control.

The reason is that the two-level inverter can only output zero and full DC link voltage. A large inductance is needed for mitigating the harmonics in the injecting compensation current. However, the large inductance leads to large volume and heavy weight of the filter inductor, which should be avoided in the practical application. In this work, a smaller filter inductor, i.e., 6.5 mH, is used to replace the large inductor. By using the smaller filter inductor, it can also show the superior performance of the multilevel inverters based DSTATCOMs in mitigating the harmonics. The parameters of the system are summarized in Table V.

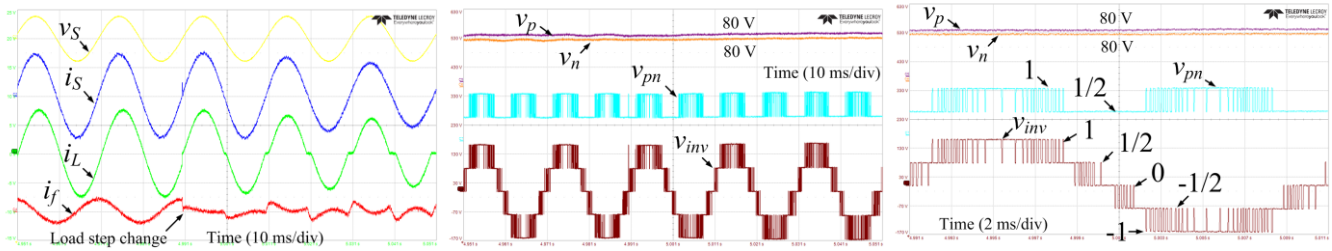
B. Calculation of PI Gains

In Section IV.A, the settling time is chosen as $t_s = 20$ ms. To achieve the settling time, the response time t_r is chosen as 2.5 ms. The crossover frequency ω_c roughly sets the control bandwidth. The closed-loop response time t_r is approximately



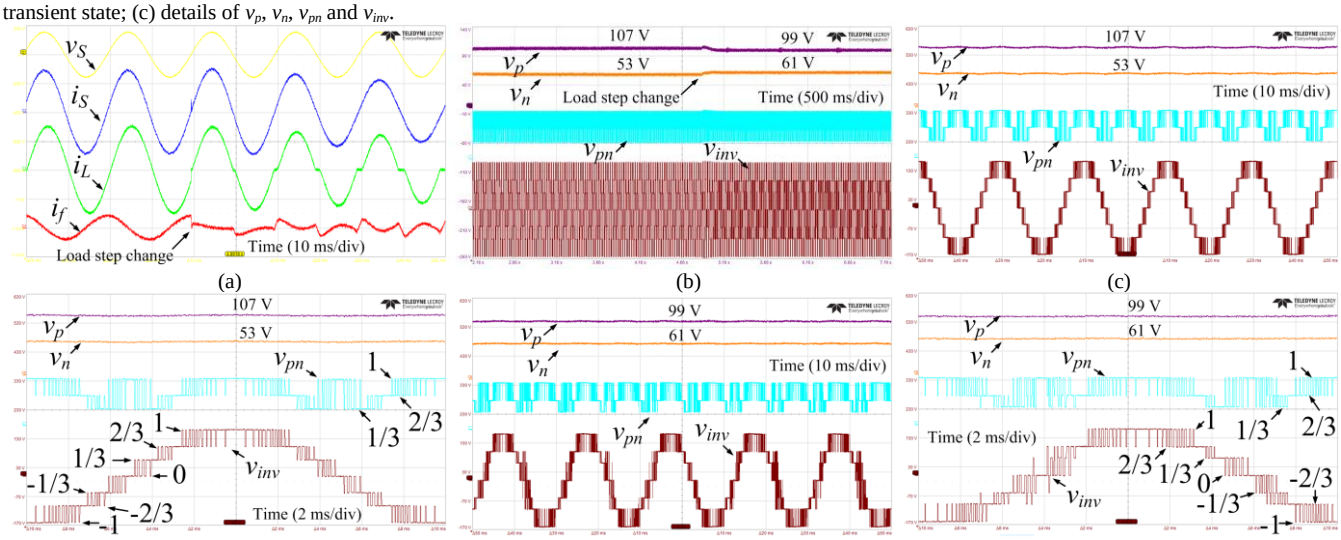
(a) (b) (c)

Fig. 9. Load step change experimental results of conventional two-level inverter based DSTATCOM under f_{upp} = 25 kHz: v_S (200 V/div), i_S (5 A/div), i_L (5 A/div), i_f (5 A/div), v_{dc} (100 V/div) and v_{inv} (100 V/div); (a) v_S, i_S, i_L and i_f under transient state; (b) v_{dc} and v_{inv} under transient state; (c) details of v_{dc} and v_{inv}.



(a) (b) (c)

Fig. 10. Load step change experimental results of three-level simplified NPC inverter based DSTATCOM under f_{upp} = 25 kHz: v_S (200 V/div), i_S (5 A/div), i_L (5 A/div), i_f (5 A/div), v_p (50 V/div), v_n (50 V/div), v_{pn} (100 V/div) and v_{inv} (100 V/div); (a) v_S, i_S, i_L and i_f under transient state; (b) v_p, v_n, v_{pn} and v_{inv} under transient state; (c) details of v_p, v_n, v_{pn} and v_{inv}.



(a) (b) (c)

(d) (e) (f)

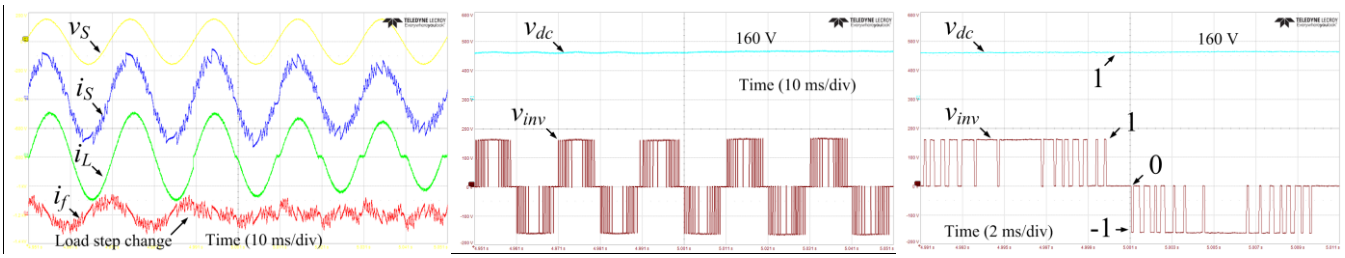
Fig. 11. Load step change experimental results of proposed S4L inverter based DSTATCOM under f_{upp} = 25 kHz: v_S (200 V/div), i_S (5 A/div), i_L (5 A/div), i_f (5 A/div) v_p (50 V/div), v_n (50 V/div), v_{pn} (100 V/div) and v_{inv} (100 V/div); (a) v_S, i_S, i_L and i_f under transient state; (b) v_p, v_n, v_{pn} and v_{inv} when the load is switched from the linear load to the nonlinear load; (c) v_p, v_n, v_{pn} and v_{inv} under the linear load condition; (d) details of v_p, v_n, v_{pn} and v_{inv} under the linear load condition; (e) v_p, v_n, v_{pn} and v_{inv} under the nonlinear load condition; (f) details of v_p, v_n, v_{pn} and v_{inv} under the nonlinear load condition.

$1/\omega_c$. Hence, ω_c is computed as 400 rad/s. Based on (27) and ω_c, the PI controller gains K_p and K_i are designed using MATLAB PID tuner toolbox, i.e., K_p = 0.38 and K_i = 88.10. The PI controller gains are listed in Table VI. The step response of the DC link control is shown in Fig. 7. The performance index of the step response is summarized in Table VI. Based on K_p, K_i and (27), the bode plot of the closed loop transfer function ϕ(s) for DC link voltage control is illustrated in Fig. 8. It is noted the phase margin is 120°, which ensures the stability of the DC link voltage control.

C. *Experimental Results*

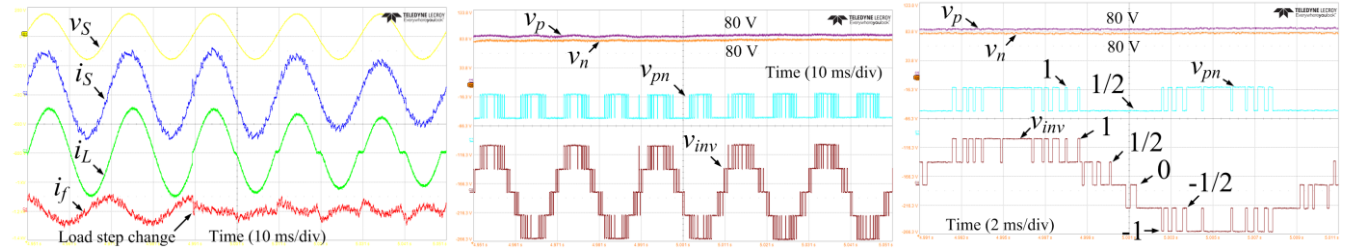
The experimental results are presented in Figs. 9-14. The THDs of i_S and i_L under the linear load and nonlinear load conditions are given in Table VI and Table VII, respectively.

The experimental results of the two-level inverter based DSTATCOM under f_{upp} = 25 kHz are shown in Fig. 9. In Fig. 9(a), it can be observed that by injecting the compensating current i_f, the source current i_S can be restored to the sinusoidal waveform and in phase with source voltage v_S. It is noted that the waveform of i_f is sinusoidal before the load step change, as the DSTATCOM only has to inject the reactive power during the linear load condition. The waveform of i_f is distorted after the load step change, as the DSTATCOM will compensate both the reactive power and the distorted load current during the nonlinear load condition. In Fig. 9(b), the output voltages v_{inv} of the conventional two-level inverter are V_{dc}, 0 and -V_{dc}. The DC link voltage v_{dc} can be maintained at 160 V. The details of the



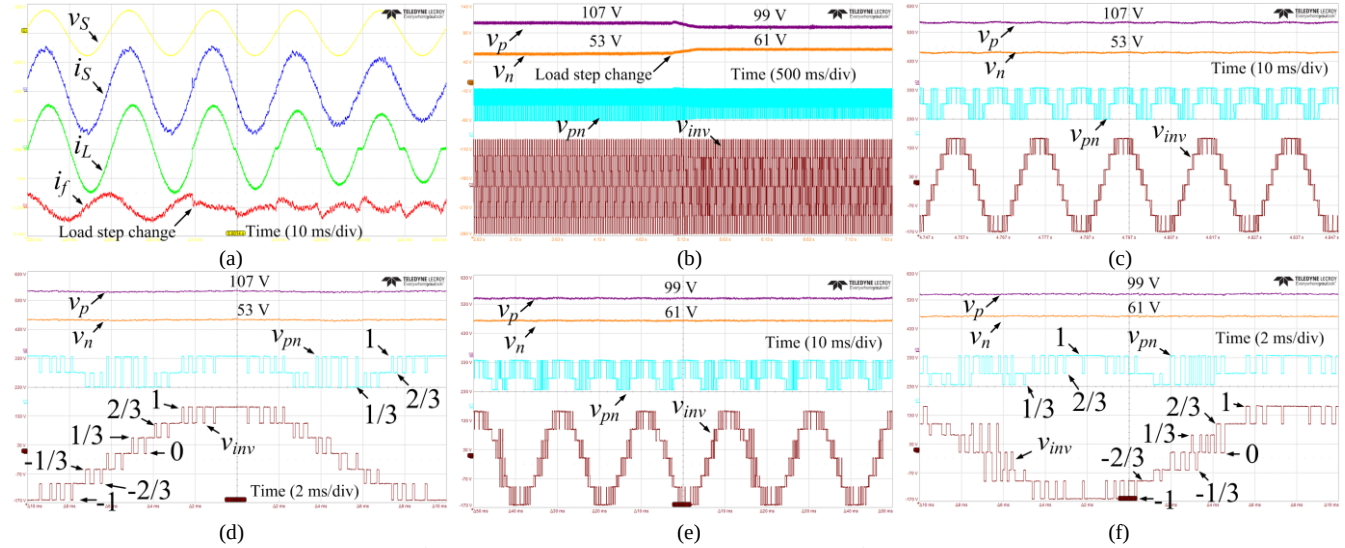
(a) (b) (c)

Fig. 12. Load step change experimental results of conventional two-level inverter based DSTATCOM under f_{low} = 10 kHz: v_S (200 V/div), i_S (5 A/div), i_L (5 A/div), i_f (5 A/div), v_{dc} (100 V/div) and v_{inv} (100 V/div); (a) v_S, i_S, i_L and i_f under transient state; (b) v_{dc} and v_{inv} under transient state; (c) details of v_{dc} and v_{inv}.



(a) (b) (c)

Fig. 13. Load step change experimental results of three-level simplified NPC inverter based DSTATCOM under f_{low} = 10 kHz: v_S (200 V/div), i_S (5 A/div), i_L (5 A/div), i_f (5 A/div), v_p (50 V/div), v_n (50 V/div), v_{pn} (100 V/div) and v_{inv} (100 V/div); (a) v_S, i_S, i_L and i_f under transient state; (b) v_p, v_n, v_{pn} and v_{inv} under transient state; (c) details of v_p, v_n, v_{pn} and v_{inv}.



(a) (b) (c)

(d) (e) (f)

Fig. 14. Load step change experimental results of proposed S4L inverter based DSTATCOM under f_{low} = 10 kHz: v_S (200 V/div), i_S (5 A/div), i_L (5 A/div), i_f (5 A/div) v_p (50 V/div), v_n (50 V/div), v_{pn} (100 V/div) and v_{inv} (100 V/div); (a) v_S, i_S, i_L and i_f under transient state; (b) v_p, v_n, v_{pn} and v_{inv} when the load is switched from the linear load to the nonlinear load; (c) v_p, v_n, v_{pn} and v_{inv} under the linear load condition; (d) details of v_p, v_n, v_{pn} and v_{inv} under the linear load condition; (e) v_p, v_n, v_{pn} and v_{inv} under the nonlinear load condition; (f) details of v_p, v_n, v_{pn} and v_{inv} under the nonlinear load condition.

voltage levels are illustrated in Fig. 9(c).

The experimental results of the three-level inverter based DSTATCOM under f_{upp} = 25 kHz are shown in Fig. 10. As shown in Fig. 10(a), the three-level inverter based DSTATCOM can provide a smoother compensating current i_f compared with the two-level inverter based topology. Thus, the THD of i_S is reduced. As presented in Tables VII and VIII, the THD reduction of i_S is 45.1% and 44.2%, respectively, under the linear and nonlinear load conditions. In Fig. 10(b), the output voltages v_{inv} of the three-level inverter are V_{dc}, V_{dc}/2, 0, -V_{dc}/2 and -V_{dc}. The DC link voltages v_p and v_n can be maintained at 80 V. The details of the voltage levels are shown in Fig. 10(c).

Fig. 11 shows the load step change experimental results of the proposed S4L inverter based DSTATCOM under f_{upp} = 25 kHz. In Fig. 11(a), it can be observed that i_f has less harmonics than that in Fig. 10(a). Hence, the THD of i_S can be further reduced. As summarized in Tables VII and VIII, the THD reduction of i_S is 64.7% and 54.7%, respectively, under the linear and nonlinear load conditions. Compared with the three-level inverter, the S4L inverter significantly improves the performance of the DSTATCOM (64.7% > 45.1% and 54.7% > 44.2%). It has to be mentioned that the performance of the three-level inverter based DSTATCOM under the linear load and nonlinear load conditions is nearly the same (45.1% ≈ 44.2%). However, the S4L inverter based DSTATCOM has better performance under the linear load condition than the nonlinear load condition (64.7% > 54.7%). The reason is that

TABLE VII
THD OF CURRENT UNDER LINEAR LOAD

Different inverters based DSTATCOM		THD (%)		THD reduction of
		i_S	i_L	i_S
Two-level inverter	40 μs	5.1	0.3	0
	100 μs	11.2	0.3	0
Three-level inverter	40 μs	2.8	0.3	45.1%
	100 μs	6.5	0.3	42.0%
S4L inverter	40 μs	1.8	0.3	64.7%
	100 μs	3.8	0.3	66.1%

*The THD of i_S in two-level inverter based DSTATCOM is chosen as the benchmark for the THD reduction calculation.

TABLE VIII
THD OF CURRENT UNDER NONLINEAR LOAD

Different inverters based DSTATCOM		THD (%)		THD reduction of
		i_S	i_L	i_S
Two-level inverter	40 μs	8.6	23.4	0
	100 μs	22.1	23.4	0
Three-level inverter	40 μs	4.8	23.4	44.2%
	100 μs	12.7	23.4	42.5%
S4L inverter	40 μs	3.9	23.4	54.7%
	100 μs	9.5	23.4	57.0%

*The THD of i_S in two-level inverter based DSTATCOM is chosen as the benchmark for the THD reduction calculation.

both the upper and lower arm DC link capacitors of the three-level inverter share half of the full DC link voltage (V_{dc}/2). There is no difference between outputting the upper and lower arm voltages, as they are both V_{dc}/2. Thus, the DC voltage balancing issue has no impact on the performance of the three-level inverter. For the S4L inverter, the upper and lower arm capacitors share two thirds and one third of the full DC link voltage ($2V_{dc}$/3 and V_{dc}/3), respectively. In Fig 11(a), the waveform of the compensation current i_f is sinusoidal under the linear load condition. Thus, the utilization rates of the upper and lower arm capacitors are the same. In Fig. 11(b), it can be observed that v_p and v_n can be well maintained at $2V_{dc}$/3 and V_{dc}/3 (107 V and 53 V) before the load step change. It means there is no DC voltage balancing issue under the linear load condition. In Fig. 11(c), v_{inv} only jumps to the adjacent levels, when there is no DC voltage balancing issue. Fig. 11(d) shows the details of v_p, v_n, v_{pn} and v_{inv} under the linear load condition. It can be observed that v_{inv} can provide four voltage levels (V_{dc}, $2V_{dc}$/3, V_{dc}/3, 0) and the symmetrical part (-V_{dc}, -$2V_{dc}$/3, -V_{dc}/3, 0). v_{inv} only jumps to the adjacent levels under the linear load condition. In Fig. 11(a), after the load step change the required waveform of i_f is distorted under the nonlinear load condition. Thus, the utilization rates of the upper and lower arm capacitors are not the same. The upper arm capacitor is required to be discharged more frequently than the lower arm capacitor. In Fig. 11(b), it is noted that after the load step change, v_p decreases until it reaches its lower boundary (99 V); v_n increases until it reaches its upper boundary (61 V). Unlike the three-level inverter, the DC voltage balancing issue has an adverse impact on the performance of the S4L inverter. We assume the lower arm capacitor should be charged according to the calculated optimal control action $u_{op}(k)$. If v_p is lower than its lower boundary, we have to charge the upper arm capacitor instead of charging the lower arm capacitor. Hence, in Figs. 11(e) and (f), it can be observed that v_{inv} can jump from 0 to $2V_{dc}$/3 or -$2V_{dc}$/3. It introduces more harmonics in i_f compared with the linear load condition. This is the reason that the S4L inverter based DSTATCOM has better performance under the linear load condition than the nonlinear load condition (64.7% >54.7%). Even though the S4L inverter has the aforementioned drawback, the performance of the S4L inverter based DSTATCOM is still better than that of the three-level inverter based DSTATCOM under the nonlinear load condition (54.7% >44.2%).

The experimental results of the two-level inverter, three-level inverter and proposed S4L inverter based DSTATCOMs under f_{low} = 10 kHz are shown in Figs. 12-14, respectively. As presented in Tables VI and VII, the S4L inverter still improves the performance of the DSTATCOM (66.1% > 42.0% and 57.0% > 42.5%) compared with the three-level inverter. Furthermore, the S4L inverter based DSTATCOM still has better performance under the linear load condition than the nonlinear load condition (66.1% >57.0%).

V. DISCUSSION

The feasibility of applying the proposed S4L inverter in the single-phase DSTATCOM system has been validated in this paper. Furthermore, by connecting the dual buck converter to a three-phase two-level inverter, the S4L inverter can be easily adopted in the three-phase DSTATCOM system. The topology of the three-phase S4L inverter is presented in Fig. 15. The number of the required switches and capacitors is 10 and 2, respectively. The feasibility validation of the S4L inverter based three-phase DSTATCOM will be presented in the future work.

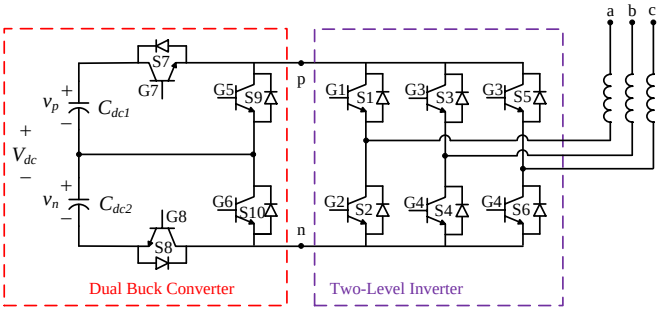


Fig. 15. Topology of the three-phase S4L inverter.

On the other hand, Y. Liu and F. L. Luo also adopt the trinary hybrid multilevel inverter in three-phase DSTATCOM [40]. The trinary hybrid multilevel inverter is one type of H-bridge cascaded inverters, which can offer five levels for DSTATCOM. However, it suffers from an inevitable disadvantage, i.e., each phase has to be formed from a single-phase H-bridge cascaded inverter for the three-phase system. Thus, the number of the required switches and capacitors are 24 and 6, respectively. The increased semiconductor count brings up the cost of the system. Compared with the hybrid multilevel inverter, the S4L inverter is a more cost-effective solution for the three-phase DSTATCOM system.

VI. Conclusion

This paper proposes a S4L inverter based single-phase DSTATCOM that obtains superior performances compared to the two-level inverter and three-level inverter based DSTATCOMs under both the linear and nonlinear load conditions. The S4L inverter based DSTATCOM can mitigate the harmonics of the source current by providing four levels for the required output voltage of the inverter in the DSTATCOM. Specifically, the dual buck converter can output full, two thirds, and one third of DC link voltages. Including the zero voltage provided by the two-level inverter, the output voltage of the proposed S4L inverter can be four levels. The proposed S4L inverter based DSTATCOM shows superior performance over the conventional three-level inverter based DSTATCOM with the same component count.

Appendix

A. Comparison of Switches Voltage Rating

The topology of the T-type converter based single-phase DSTATCOM is presented in Fig. 16 [28]. In the T-type converter, the voltage stress on S1, S2, S3 and S4 is full DC link voltage V_{dc}. The voltage stress on S5, S6, S7 and S8 is half DC link voltage $V_{dc}/2$.

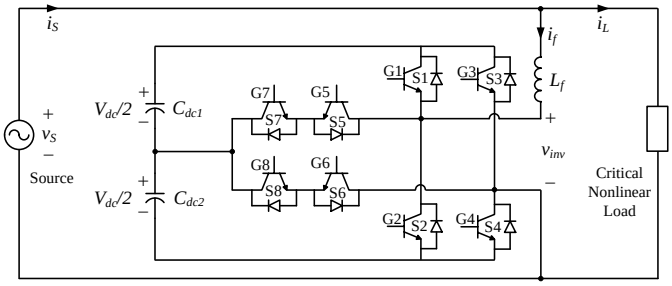


Fig. 16. Topology of the T-type converter based single-phase DSTATCOM.

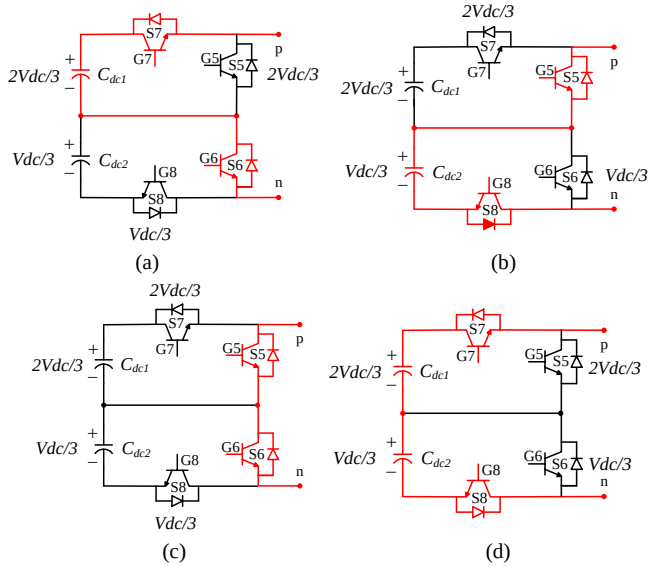


Fig. 17. Voltage stress on S5, S6, S7 and S8 in the S4L inverter (a) S6 and S7 are on, S5 and S8 are off; (b) S5 and S8 are on, S6 and S7 are off; (c) S5 and S6 are on, S7 and S8 are off; (d) S7 and S8 are on, S5 and S6 are off.

In Fig. 1, it can be observed that the voltage stress on S1, S2, S3 and S4 is also full DC link voltage V_{dc}. The voltage stress on S5, S6, S7 and S8 in the S4L inverter is illustrated in Fig. 17.

Based on the voltage stress on the switches, the voltage rating of the switches in the T-type converter and the S4L inverter is compared in Table IX.

TABLE IX
Comparison of Voltage Rating of Switches in T-type and S4L Inverters

	Topology	Number of switches with different voltage rating			
		$V_{dc}/3$	$2V_{dc}/3$	$V_{dc}/2$	V_{dc}
Three-level	T-type [28]	0	0	4 (S5,S6,S7,S8)	4
Four-level	S4L	2 (S6,S8)	2 (S5, S7)	0	4

S5 and S7 of the S4L inverter has higher voltage rating than those of the T-type converter. S6 and S8 of the S4L inverter has lower voltage rating than those of the T-type converter. Thus, the cost of the T-type converter and the S4L inverter can be considered nearly the same. However, as the S4L inverter can output four voltage levels, it can provide better performance than the T-type converter.

B. Comparison of Switching Losses

In order to compare the switching losses between the T-type converter and the proposed S4L inverter, the DC link voltage is chosen as 1200 V, the nominal system power rating is 10 kVA. Infineon IGBT 1200 V, 40 A IKW40T120 is used to handle the full and two thirds of the DC link voltage (1200 V and 800 V). Infineon IGBT 600 V, 50 A IKW50N60T is applied to handle the half and one third of the DC link voltage (600 V and 400 V). According to the datasheet provided by Infineon, the total switching losses of switches with different collector-emitter voltage are listed in Table X.

TABLE X
Comparison of Total Switching Losses of Switches with Different Collector-emitter Voltage

	Switches with different collector-emitter voltage			
	50 A IKW50N60T		40 A IKW40T120	
	400 V	600 V	800 V	1200 V
Total switching losses* (mJ)	2.6	3.4	8.8	13.4

*The total switching losses include the losses due to diode recovery and the operating junction temperature is 25° C.

Based on the total switching losses provided by Infineon, the efficiency of the S4L inverter and the T-type converter under f_{upp} = 25 kHz and f_{low} = 10 kHz can be calculated and summarized in Table XI.

TABLE XI
Comparison of Efficiency of T-type Converter and S4L Inverter under Different Operating Frequency

	T-type [28]		S4L	
	25 kHz	10 kHz	25 kHz	10 kHz
Efficiency (%)	98.8	99.1	98.7	99.0

It is noted the efficiency of the S4L inverter is only slightly lower than the T-type converter. Considering the superior THD

performance of the S4L inverter, it is still a promising solution for the DSTATCOM system.

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