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CRN - CNPA 76-8 Energie
FR7602514

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to be published in
Journal of
Applied Physics

Institut National
de Physique Nucléaire
et de Physique
des Particules

Université
Louis Pasteur
de Strasbourg

67037 STRASBOURG-CEDEX FRANCE

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ABSTRACT

The open circuit voltage of MIS solar cells realized on N-type silicon has been investigated. Chemically formed and evaporated SiO_x layers have been used for the insulating film. The latter has given the best results on polished samples, since V_{oc} reached 0.55 V. The influence of different parameters, like n or Φ_{Bn} are discussed.

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I. INTRODUCTION

Great interest in the field of Schottky silicon solar cells is rising since the advantages of these structures over the P-N junctions have been recognized. These advantages summarize as follows :

- a thin entrance window, which allows the carriers to be generated in the sensitive region even by the short wavelengths and a better collection efficiency ;

- fabrication of the devices at room temperature, so that no degradation of diffusion lengths and lifetimes occur ;

- ability to be used on polycristalline substrates.

However, due to a larger saturation current, the open circuit voltage V_{oc} of a Schottky diode is lower than that of a P-N junction. In the latter, V_{oc} ranges about 0.6 V, close to the built-in potential V_{Bi}. In the case of a Schottky cell, the open circuit voltage is expressed by

$$V_{oc} = n\left[\Phi_B + (kT/q)\ln\left(I_p/A^{++}T^2\right)\right] , \qquad (1)$$

where all the terms have their usual meaning. For example, an ideal gold-N-type silicon diode ($n = 1$, $\Phi_{Bn} = 0.8$ eV) gives $V_{oc} = 0.3$ V under AMO illumination if one assumes ideal conditions i.e. quantum and charge collection efficiencies are unity, no losses by reflection. Therefore, to become compe-

titive with P-N junctions, the open circuit voltage of Schottky solar cells has to be improved.

From equation (1) it appears that V_{oc} can be increased either by using a higher barrier Φ_B at the metal-semiconductor contact, or by increasing the diode quality factor n. On fig. 1 V_{oc} is plotted as a function of these two parameters Φ_B and n for the ideal conditions already described. However, it has to be mentioned that we have observed that this law generally does not apply on diodes with $n > 1.5$; furthermore, for larger values of n, a degradation in the fill factor occurs, as predicted by FONASHI's [1] calculations. Consequently, the most efficient way to improve V_{oc} is to increase Φ_B. As the highest Φ_B on silicon barriers is only about 0.8 eV, MIS or MOS structures are requested. Following CARD and RHODERICK [2], using their definitions, in such a structure, the open circuit voltage will be given by

$$V_{oc} = n[\Phi_B + (kT/q)\chi^{1/2}\delta + (kT/q)\ln I_p/A^{++}T^2)] \quad . \qquad (2)$$

It is clear that V_{oc} rises with the thickness of the interfacial layer δ. However, the quality factor is also related to δ. Three cases can be considered:

* if the interface states density is very small : $n = 1 + \delta\varepsilon_s/w\varepsilon_i$ (3)

where ε_s and ε_i are the dielectric constants of the semiconductor and the interfacial layer, w the thickness of the depletion layer ;

* if all the interface states are in equilibrium with the metal :

$$n = 1 + \delta\varepsilon_s/w(\varepsilon_i + \delta q D_{Sa}) \qquad (4)$$

where D_{Sa} denotes the interface state density.

* if all the interface states equilibrate with the semiconductor :

$$n = 1 + (\delta/\varepsilon_i)(\varepsilon_s/w + q D_{Sb}) \qquad (5)$$

In the two first cases, the effect of an interfacial layer and of interface states on n is small. The device behaves, therefore, like an "ideal" Schottky diode but with a higher V_{oc}. As the interfacial layer becomes thicker, the number of states that are in equilibrium with the semiconductor increases and then n has a larger value. In 10 Ω.cm silicon, for example, common values such as $\delta = 30$ Å and $D_{Sb} = 10^{12}$ cm^{-2} eV^{-1} lead to $n \approx 1.65$.

Following a more general analysis by FONASH [1, 3] the behaviour of a MIS device may be summarized as follows : as long as the interfacial layer just hinders the flow of majority carriers from the semiconductor to the metal, the diode behaves like a minority carrier device, the saturation current is reduced and consequently V_{oc} increases ; nevertheless its value is limited by the built-in potential. When the effect of the interfacial layer is to trap charges on interface states close to the semiconductor surface, the total voltage V developped by the MIS structure is such that :

$$V = V_S + V_I \ , \qquad (6)$$

where V_S and V_I are, respectively, the voltage developped in the semiconductor and in the interfacial layer. If the interface states are in equilibrium with the metal :

$$V_I = (2\varepsilon N_D \varepsilon_s)^{1/2} (\delta/\varepsilon_i)/(1 + e D_{ss}\ \delta/\varepsilon_i) \times [(V_{Bi})^{1/2} - (V_{Bi} - V_s)^{1/2}] \qquad (7)$$

The effect of the interfacial layer and of the interface states are the same as in eq. (4). When the interface states are in equilibrium with the semiconductor eq. (7) is replaced by :

$$V_I = e\, D_{ss}\, V_s\, \delta/\varepsilon_i + (2eN_D \varepsilon_s)^{1/2} (\delta/\varepsilon_i) \left[(V_{Bi})^{1/2} - (V_{Bi} - V_s)^{1/2}\right] \qquad (8)$$

Here, V_I increases with δ and D_{ss}, so that V becomes larger than V_s. Furthermore, n remains close to unity and the fill factor is improved. It can be noticed at this time that the fill factor F of an ideal Schottky solar cell would be F = 0.72.

This paper is an attempt to show that it is possible to improve the open circuit voltage of gold-Schottky barriers on N-type silicon by about 70 %, by a proper choice of surface preparation and interfacial oxide layer. Further, it will be demonstrated that V_{oc} can be larger than predicted by eqs. (1) or (2), due to the presence of slow interface states.

II. EXPERIMENTAL

N-type silicon, 1to 10 Ω.cm in resistivity, oriented along the < 111 > axis has been used. The samples were first rinsed in hydrofluoric acid and then in deionized water, but not etched. The interfacial layer was realized immediately after this cleaning procedure. For the latter, two techniques were used on these optically polished surfaces. In the first one, the samples were dropped in boiling nitric acid during times ranging from 0 to 8 minutes and a chemical oxide was grown. In the second process, silicon monoxide was evaporated at a pressure of about $5 . 10^{-6}$ torr up to a thickness of 40 Å. Backscattering measurements performed by means of a 2 MeV $^4He^+$ beam have shown that the stoichiometry of the deposited SiO_x layer strongly depends upon

the evaporation rate of silicon monoxide. When a slow rate (less than 1 Å/sec) is used x = 1.8 and for a fast one (10 Å/sec) x = 1.2.

In order to realize insulating layers with a structure as close as possible to that of silicon dioxide a 0.5 to 1 Å deposition rate was used. Gold contacts 100 Å thick were then evaporated on the interfacial layers. Ohmic contacts were obtained by evaporation of a 1 000 Å layer of magnesium on the lapped back side of the samples.

Determination of the effective barrier height $\bar{\varphi}'_{Bn}$ (defined as $\bar{\varphi}'_{Bn} = \bar{\varphi}_{Bn} + (kT/q)\,\chi^{1/2}\,\delta$) and of the diode quality factor n was performed by means of photometric and forward current measurements. The open circuit voltage V_{oc} was measured under 100 mW/cm^2 tungsten lamp illumination (T = 2900°K) filtered by 4 cm of deionized water. Under these conditions, we obtained for a conventional diffused cell I_{SC} = 30 mA/cm^2 and V_{oc} = 0.57 V. The theoretical value of V_{oc} for Schottky diodes under these experimental conditions has been computed by using eq. 1 and taking into account a transmission factor of 0.5 for the gold film, so that :

$$V_{oc}\,(c) = n\,(\bar{\varphi}_{Bn} - 0.52) \qquad (9)$$

III. RESULTS

Table I summarizes the results obtained for a number of samples oxidized during various times in boiling nitric acid.

TABLE I

Φ'_{Bn} (eV)	n	V_{oc} (mV)	V_{oc} (c) mV
0.79	1.34	325	362
0.80	1.11	300	311
0.80	1.13	310	316
0.81	1.04	312	302
0.815	1.22	356	360
0.825	1.15	358	351
0.83	1.22	398	37
0.84	1.19	405	380
0.85	1.39	420	450

The highest barrier height (Φ'_{Bn} = 0.85 eV) is obtained for a 2 minutes process and the resulting V_{oc} is 0.42 V. Under the same experimental conditions an ideal gold-Schottky diode (Φ_{Bn} = 0.80 eV, n = 1) would give V_{oc} = 0.28 V. The agreement between experimental and calculated values of V_{oc} is satisfactory, due to the rather low n values ; it is more easily seen on fig. 2 where V_{oc}/n has been plotted as a function of Φ'_{Bn}.

B. Diodes with an evaporated oxide layer

The main characteristics of the samples covered with a SiO_x interfacial layer of 20-30 Å thickness are reported on table II.

TABLE II

ϕ'_{Bn} (eV)	n	V_{oc} (mV)	V_{oc} (C) (mV)
0.83	1.59	490	493
0.88	1.34	550	494
0.88	1.25	517	450
0.89	1.19	536	440
0.92	1.21	505	463

Generally, the barrier height of these samples reaches about 0.90 eV and the n factor remains less than 1.4. Only in the case of the first sample the increase of V_{oc} results from a higher n value and it can be noticed that for this sample the agreement between experimental and calculated V_{oc} is very good. For the other samples, the measured values of V_{oc} are greater than expected from eq. 9 and reach sometimes values as high as 0.55 V. However, for this last kind of samples, we have noticed a small reduction in V_{oc} with time during a few hours after manufacturing. This final value is very close to that expected (see fig. 2). Thus, the influence of slow interface states is clear.

C. Application to solar cells

The devices, whose sensitive surface is 0.18 cm^2 were studied without grids and antireflective coating under tungsten lamp illumination (100 mW/cm^2). The samples with a chemically formed oxide layer show the same short circuit current as a reference Schottky diode ($I_{sc} \approx 16$ mA/cm^2). As the fill factor

ranges between 0.65 and 0.75, this corresponds to a maximum efficiency of about 5-6 %.

Diodes with an evaporated interface layer have a higher short circuit current ($I_{sc} \approx 22$ mA/cm^2) and the fill factor lies between 0.67 and 0.75. As an example, a particular device had the following characteristics $V_{oc} \approx 0.55$ V, $I_{sc} = 4.2$ mA, $F = 0.72$. This corresponds to a 9 % efficiency for a device entirely manufactured at room temperature.

III. DISCUSSION

Fig. 3 shows a plot of forward I-V characteristics of a reference Schottky diode without interfacial layer (curve 1) and of two MIS structures respectively with a chemical oxide layer (curve 2) and an evaporated SiO_x layer (curves 3a and 3b). In the case of a chemical oxide, the improvement in V_{oc} mainly results from a decrease in the saturation current. The barrier height, as deduced from the I-V plot is $\phi^{I}_{Bn} = 0.86$ eV and $n = 1.19$. The open circuit voltage (0.40 V) is the same as that predicted. It appears also that the current plot remains very close to that of the reference diode. Therefore, we may conclude that the effect of the interfacial layer is to reduce the flow of the majority carriers, but the influence of the interface states is negligeable. The case of an evaporated oxide is quite different. Curve 3a has been measured immediately after the device manufacturing. At low voltages, the behaviour is that of a Schottky barrier, very close to curve 2, in particular, the saturation current is the same, but at higher voltages (0.3 - 0.4 V) the current is much more lower and the characteristic

shifts towards the diffusion limit. This behaviour might be explained by the presence at the surface of the semiconductor of a low density of localized states causing charges to be trapped, their population being dictated by the Fermi level position in the semiconductor. This characteristic has been measured again after the aging occured (curve 3b), so that the interface states have stabilized. The current increases so that the initial characteristic shifts towards the thermoionic limit, however, the saturation current remains the same, i.e. $\phi'_{Bn} = 0.86$ eV. Taking into account the n value of 1.34, we obtained V_{oc} (c) = 0.46 V and $V_{oc} = 0.48$ V. The measured V_{oc} corresponding to the conditions of fig. 3a was $V_{oc} = 0.55$ V. Assuming that n remains essentially constant and that eq. 6 may be used $V_i = 0.07$ V. By using eq. 8 and assuming $\delta = 30$ Å, $N_D = 10^{16}$ cm^{-3}, $\varepsilon_i = 4\,\varepsilon_o$, the density of interface states may be determined $D_{ss} \approx 8 \cdot 10^{11}$ cm^{-2} eV^{-1}.

IV. CONCLUSION

In order to make a general comparison of the results already obtained on Schotky silicon solar cells by different authors, we have reported on table III the main characteristics of their MIS structures. It appears that polished silicon with about a 20 Å oxide layer would lead to the best results. < 111 > is known to give more surface states, but on an other hand it has been shown recently [9] that < 100 > oriented silicon would produce a higher current and a better fill factor than < 111 >. Thermal oxide and chemical oxide seem to give practically the same results on P-type material, provided they are annealed before depositing the rectifying metal contact. Further, it has been demonstrated by backscattering measurements [10 - 11] that the thermal oxide has an excess silicon concentration at the SiO_2-Si interface and that it contains some amount of carbon and carbides which should influence the surface states.

On N-type silicon it seems, both from our own experience and from table III, that a thermal or chemical oxide interface does not result in a V_{oc} higher than 0.42 V, contrarily to evaporated layers which give up to V_{oc}=0.55 V. The reasons of this different behaviour is not clear at present time and a study of these interfaces is under way in the laboratory. Without antireflective coating the short circuit current under 100 mW/cm^2 illumination is about 20 mA/cm^2. Table III shows that by using a proper antireflective coating or a multi-layer structure this current may be improved by about 50 %, thus leading to I_{sc} = 30 mA/cm^2. Last, the fill factor reported by different authors is generally less than 0.70, however, here we have shown that it may be, at least, as high as the theoretical value of 0.72 of an ideal diode. Then, it may be concluded that Schottky silicon solar cells are already able to give efficiencies higher than 13 %, value which compares with the 15 % efficiency reached for gallium arsenide Schottky solar cells (12).

TABLE III

Characteristics of the main results obtained at this time on MIS silicon solar cells

Type	Orientation	Resistivity Ω.cm	Surface Preparation	Oxide	Oxide Thickness (Å)	Contact	V_{oc} (mV)	I_{sc} (mA/cm^2)	Fill Factor	Efficiency (%)	Ref.
P	< 100 >	2	polished	600°C in Air + N_2	5-10	50 Å Cr + 50 Å Cu + 10 Å Cr	520	29*	65	9.5	4
P		3.5 - 15		dry O_2 700°C + annealing	20-40	Al 80-100 Å	470	26.5**		8	5
P	< 111 >	5-10		boiling H_2O + annealing	40-80	Ti	520	18.5			6
N	< 111 >	4.9.	formic acid + perhydrol	400°C in air	10-23 optimum 13	Au 100 Å	410	(25)	66	6.5	7
N	< 111 >	epitaxial $N_D = 5.10^{14}$ cm^{-3}	standard			Au	410	40 21	48	9	8
N	< 111 >	1 - 10	optically polished	SiO_x evaporated	10-40	Au 100Å	550	22	up to 75	9	this work

*multi layer structure

**coated

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FIGURE CAPTIONS

Fig. 1 Plot of the open circuit voltage expected under AMO conditions in Schottky silicon solar cells as a function of the barrier height and diode quality factor.

Fig. 2 Plot of experimental and calculated values of V_{oc}/n in MIS silicon solar cell versus the barrier height

Fig. 3 Forward I-V characteristics of 1) a conventional Schottky barrier 2) a MIS diode with a chemical interface and 3) a MIS diode with an evaporated oxide : curve 3a) measured immediately after manufacturing curve 3b) measured after stabilization of interface states.

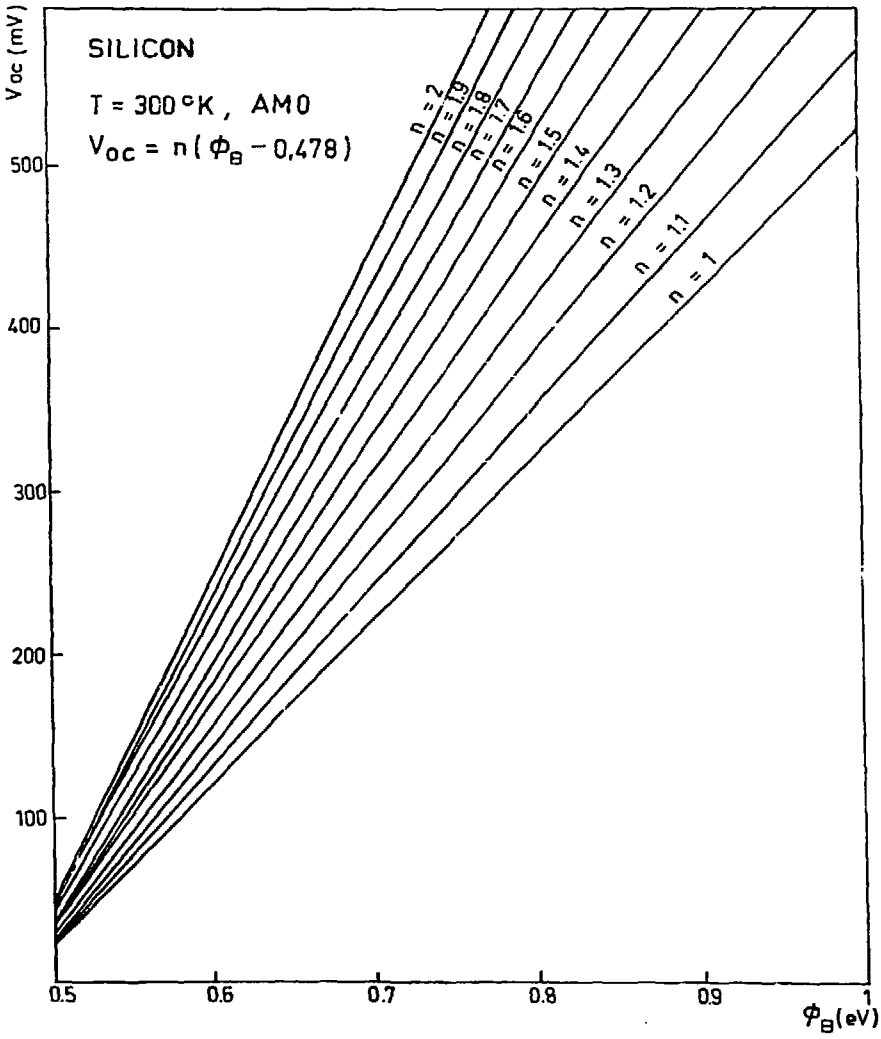
SILICON
T = 300 °K , AM0
Voc = n (φB − 0,478)
Voc (mV)
500
400
300
200
100
0.5
0.6
0.7
0.8
0.9
1
φB(eV)
n = 2
n = 1.9
n = 1.8
n = 1.7
n = 1.6
n = 1.5
n = 1.4
n = 1.3
n = 1.2
n = 1.1
n = 1

Fig. 1

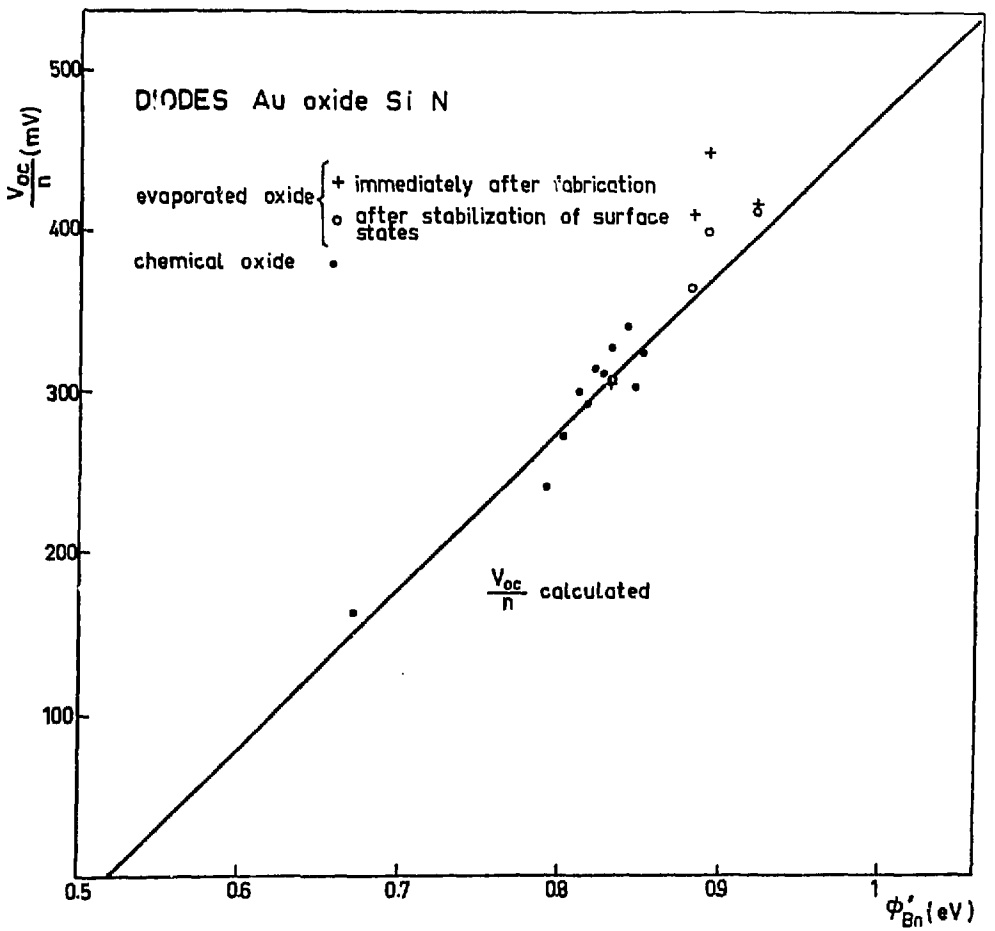
DIODES Au oxide Si N
evaporated oxide
+ immediately after fabrication
o after stabilization of surface states
chemical oxide
$\frac{V_{oc}}{n}$ calculated
$\frac{V_{oc}}{n}$ (mV)
500
400
300
200
100
0.5
0.6
0.7
0.8
0.9
1
Φ'_{Bn} (eV)

Fig. 2

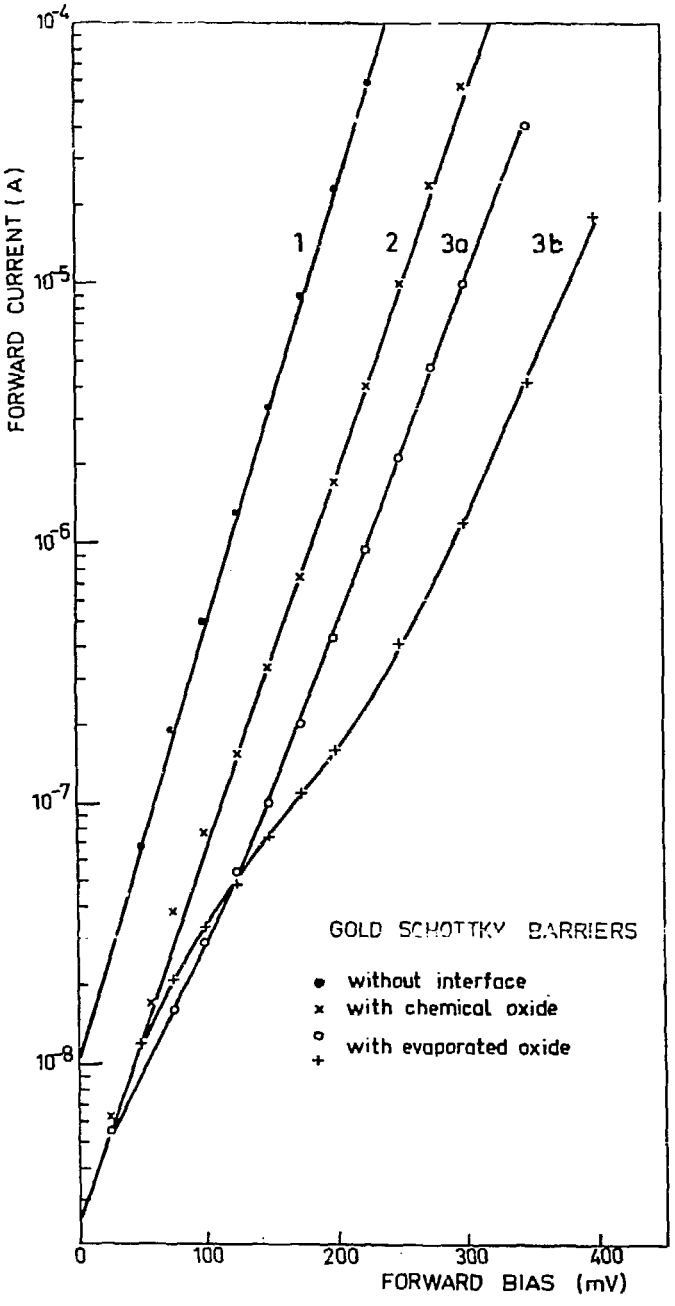
FORWARD CURRENT (A)
10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
1
2
3a
3b
GOLD SCHOTTKY BARRIERS
without interface
with chemical oxide
with evaporated oxide
0
100
200
300
400
FORWARD BIAS (mV)

Fig. 3