ELECTRICAL AND ELECTRON MICROSCOPY OBSERVATIONS ON DEFECTS IN ION IMPLANTED SILICON

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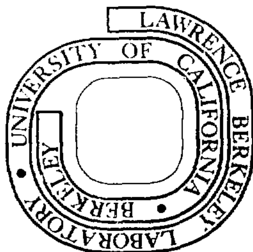

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ABSTRACT

Silicon single crystals were implanted with 100 KeV phosphorous ions to a dose of 2 X 10^{16} ions/cm^2 at both room-temperature and 600°C. They were isochronally annealed at temperatures ranging from 400°C to 900°C. Sheet resistivity measurements of the specimens were taken after each anneal, together with corresponding transmission electron micrographs.

The observations show that when a completely amorphous layer is produced by ion implantation at room-temperature, epitaxial recrystallization onto the single crystal substrate during annealing at 600°C leaves a dislocated surface containing secondary defects. There appear to be a significant difference in the number of defects per implanted ion between room-temperature and 600°C implants, when annealing to 800°C and 900°C.

Sheet-resistivity measurement showed that, above a critical dose, room temperature implantation followed by a 600°C post anneal is substantially more effective for achieving electrical activity of the phosphorous than is implantation at 600°C. But 600°C implanation followed by 800°C and 900°C post annealed is more effective than room-temperature implantation.

The observed annealing behavior is explained in terms of defects that form during the recrystallization process.

INTRODUCTION

For heavy ions of phosphorous implanted into silicon at room-temperature zones of severely damaged material are produced in addition to isolated point defects around the periphery of the zones. If the damage is not annealed during the implantation, an amorphous layer is eventually formed where the individual damage zones overlap.[1,2] An annealing treatment is then required both to return the sample to crystallinity and to put the phosphorous atoms onto electrically active sites (generally assumed to be substitutional positions). It is thought that the activation energy for epitaxial recrystallization depends on the Radius of the amorphous region and to a very rough approximation, the ratio of the recrystallization temperature for an amorphous region of radius R to that for an infinite volume (e.g. a flat interface) is given by

$$\frac{Tr}{T_\infty} = 1 - \frac{2\gamma iW}{RE_\infty}$$

where γi is the interfacial free energy between crystalline and amorphous Si, w is the activation volume for recrystallization (i.e. the volume of the 5 atom agglomerations which constitute amorphous Si, and E_∞ is the activation energy for an infinite interface. Choosing reasonable values for γi = 500 erg cm^{-2}, W = 2 x 10^{-22} cm^{-3} and E_∞ = 5 ev, the annealing temperature curve as a function of zone size can be determined. The temperature is about 600°C where zones of ~200Å have to be recrystallized. One can avoid the formation of an amorphous layer by holding the substrate at higher temperature during implantation.[1,2] For implantation performed at 600°C, a disordered region anneals

individually before the next ion strikes in its vicinity, thus preventing formation of the continuous amorphous layer even for high dose implants.

The characteristics of implanted phosphorous ions in silicon have been investigated by several authors using either radio-tracer[3-4] or electrical measurements.[5-13] Also, secondary defects in ion-implantation silicon have been observed by transmission electron microscopy. However, correlations between such defects and electrical properties of the ion-implanted layers are incomplete. Sheet resistivity and electron microscope observations have been made for B^+ implanted and annealed silicon by Bicknell and Allen. However, Bicknell et al. just investigated moderate doses which did not form continuous amorphous layers. Also, their characterization of the loops formed on annealing do not agree with similar observations in this laboratory.

In an effort to determine the effects of recrystallization according to these two different mechanisms on the secondary ion implantation defects, implants were performed to the same dose but at two different temperatures, room-temperature and 600°C. Transmission electron microscopy was used to study the detailed nature of secondary defects formed by the ion implantation and subsequent annealing. Four-point probe sheet-resistivity measurements[23, 24] were used to study the electrical property changes during the annealing. The annealing characteristics of layers implanted into silicon at 100 KeV with dose 2×10^{16} ions/cm^2 were measured and observed following isochronal annealing to 900°C. Room-temperature implants remain amorphous below 600°C and are not useful for most practical applications. 900°C was chosen as the upper annealing limit beyond which long-range diffusion would destroy any

advantage of profile control offered by the ion implantation technique.

This thesis reports on the measurements and conclusions of the study to date.

EXPERIMENTAL

N-type silicon wafers, 5 Ω-cm of (111) and (100) orientations were irradiated at both room-temperature and 600°C, with phosphorous ions at 100 KeV to a dose of 2 x 10^{16} ions/cm^{2}. The dose was chosen so as to produce a continuous amorphous layer in the room-temperature implant.

Pieces 1/2 in. x 1/2 in. were scribed from both (100) and (111) wafers for sheet resistivity measurements. The sheet resistivity specimens were annealed isochronally from 600°C up to 900°C in 100°C intervals for 20 minutes in a quartz tube furnace with dry nitrogen passing through it. After annealing, the sheet-resistivity measurements were performed by the four-point probe technique. After measurement, the pieces were ultrasonically cut into discs of 3 mm in diameter. They were then chemically thinned in a solution made up of two parts ($3HNO_3$:1HF) to one part (2.5 gm I_2 in 1100 ml CH_3COOH). The thinned samples were examined in transmission in a JEM 7A and a Philips 301 transmission electron microscope operating at 100 KeV.

RESULTS AND DISCUSSION

A. Electrical Properties:

(I) Implantation at Room-Temperature:

The changes in resistivity of (111) and (100) specimens phosphorous implanted at 100 KeV at room-temperature are shown in Fig. 1 during an isochronal annealing sequence.

There is a steady decrease in sheet resistance, between room-temperature to 600°C, as the anneal temperature increases. Webber, Thorn and Large[22] have shown that carrier mobility remains approximately constant in this region whilst the number of carriers increases. The steep fall in sheet resistance between 300°C and 600°C is due to annealing out of primary damage as the amorphous layer recrystallizes epitaxially onto the single crystal substrate. As indicated in the figure, approximately 80 percent of the implanted phosphorous atoms were on active sites following a 600°C anneal. The remaining 20 percent did not become active until annealing to a temperature of 900°C.

The sheet resistivity shows a steady decrease over the temperature region between 600°C and 900°C, but since the carrier mobility remains reasonably constant,[22] it is apparent that more carriers are becoming active. This also is confirmed by early work.[23-26] The good agreement between the phosphorous concentration profile after annealing at 600°C and 800°C suggests that very little long-range diffusion takes place during isochronal annealing between

those two temperatures and that the observed fall in sheet resistance is simply due to an increase in the number of active carriers.

(II) Implantation at 600°C:

Implantation at 600°C and the consequent annealing out of each individual ion track as it is formed prevents any build up of primary damage and the formation of a continuous amorphous layer. In this case, the sheet resistance of the implanted layer was initially higher than that which would be achieved in a room-temperature implanted specimen after 600°C unannealing. The sheet resistivity then fell continuously with increasing annealing temperature above 600°C. Comparison of these two implantation conditions by Shannon, Ford and Gard(13) have shown that the profiles of electrically active phosphorous suggests that the implantations made at 600°C where damage was being continuously annealed out enabled more of the implanted ions to enter channels throughout the duration of the implant and thus form a more pronounced tail on the depth distribution. Calculation of the total number of carriers to be expected for these two profiles suggests that the concentration of active phosphorous in the 600°C implantation should be somewhat below that achieved for a room-temperature implanted specimen which has been annealed at 600°C. This can account in part for the higher sheet resistance measured following the 600°C anneal of a layer implanted at 600°C

as compared to a room-temperature implanted specimen.

From our results, complete electrical activity (Max. number of carriers) is not observed until annealing to nearly 800°C. This necessity for high annealing temperature to achieve substantially complete activity of the phosphorous is found in almost all cases[6] where a continuous amorphous layer is not formed during implantation. This has been attributed to the presence of electrically active defect centers[17] [25] which compensate the dopant behavior of the implanted atoms.

B. Electron Microscope Observation of Damage Structure:

A series of micrographs and diffraction patterns obtained by transmission electron microscopy is shown in Figure 2-7.

(I) Implanted at Room Temperature:

A. At Unannealed State:

Figure 2 is a micrograph of the edge region of a specimen of silicon, having the (100) plane parallel to its surface. The region A, shows very strong amorphous diffraction rings; in region B, the selected area diffraction pattern consists of several diffuse rings as well as crystalline spots, and in region C, there is only a single crystal diffraction pattern. This confirms that a buried amorphous layer is sandwiched between a thin crystalline layer at the surface and the underlying crystal substrate.

Many small (100-200 Å) dark spots are seen in bright field micrograph (light spots in dark field). We believe

these spots are in the crystalline-amorphous interface since they are not found in specimens where the amorphous layer can be observed alone with the crystalline material stripped away. Also, these spots are strongly visible in dark field only when a crystalline reflection is selected rather than a diffuse ring arising from the amorphous material.

B. Annealed to 600°C-800°C:

At 600°C, recrystallization of the amorphous layer had occurred epitaxially so that the single crystal is reformed. The point defects develop into secondary defects which become visible by transmission electron microscopy such as black dot defects, perfect and faulted dislocation loops, dislocation dipoles. As seen from Figure 4 and 6 with increasing of annealing temperatures, dislocation loop density decreases and the average diameter of loops increases. These loops were analyzed by tilting the specimen in the microscope and examining both dark and bright field images. All these dislocation loops were determined to be interstititial type.[27,28,29,30] The streaking in the diffraction pattern could arise from thin platelets or rods and could be caused by a high concentration of dislocation loops lying on planes perpendicular to the foil surface.

C. Annealed to 900°C:

Dislocation networks were generted lying approximately parallel to the foil surface. It was confirmed by Tamura[30] using the g.b. = o criterion that the dislocation segments

comprising the network were all pure edge type lying approximately along the 211 directions. Burgers vectors were of the $\frac{a}{2}\langle 110\rangle$ type in the (111) film plane.

(II) Implanted at 600°C:

A. Figure 5 shows that an amorphous layer was no longer formed during implantation; black dot defects and complex dislocation entanglements were observed.

B. Annealed to 800°C:

Figure 6A and 6B shows these defects grew into dislocation loops. Comparing these pictures 6A, 6B, 6C and 6D shows that defect density is different. It can be seen that 600°C implantation followed by an 800°C post anneal 20 minutes results in lower defect density. This may explain why we get lower resistivity in 600°C implantation followed by an 800°C post annealing.

CONCLUSION

A detailed examination of the changes in electrical conductivity and secondary defects formed during post implantation annealing of phosphorous-implanted silicon has led to the following observations and conclusions:

(i) The results presented show a strong correlation betwen the electrical activity of phosphorous implanted silicon and its appearance in the electron microscope (e.g. the kind of defects, density of defects).

(ii) It can be seen that 600°C implantation followed by 800°C annealing reduces the defect density compared to room-temperature implantation and 800°C annealing.

(iii) For every room-temperature implantation report to date in which a large increase in number of carriers was found near 600°C annealing temperature, the total ion dose was sufficiently high to have formed an amorphous layer. If an amorphous layer is not formed (hot-substrate implantations), annealing temperatures of at least 700-750°C are required for the number of carriers to reach its maximum value.

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FIGURE CAPTIONS

Fig. 1. (a) The sheet resistance of phosphorous layers implanted into silicon at both room temperature and 600°C. Measurements are made following each successive isochronal annealing.

Fig. 2. (a) A bright field image of a N-type (100) silicon sample irradiated with 2×10^{16} p ions/cm^2 at room temperature. A buried amorphous layer is sandwiched between a thin crystalline layer at the surface and the underlying crystal substrate. The region marked A shows very strong amorphous diffraction rings and region B shows a crystalline-amorphous interface. The region C is a thick region which just shows a crystalline pattern.

(b) Shows a dark field image by placing the objective aperture at the crystal spot. Light spots are believed to be islands of crystal near the crystalline amorphous interface.

Fig. 3 Shows bright field image and dark field image of a N-type (111) silicon sample irradiated with 2×10^{16} p ions/cm^2 at room temperature.

Fig. 4 (a) A (111) orientation N-type silicon film bombarded with 2×10^{16}, 100 KeV p ions/cm^2 and annealed for 20 minutes at 600°C. Epitaxial recrystallization occurs.

(b) (100) orientation.

Fig. 5 (a) Shows a bright field image of (111) orientation N-type silicon film bombarded with 2×10^{16} p ions/cm^2 at 600°C.

An amorphous layer is no longer formed during the implantation. Black dot defects and complex dislocation entanglement were observed.

(b) (100) orientation.

Fig. 6 All specimens were implanted with 2×10^{16} p ions/cm^2 at 100 KeV and then annealed for 20 min. at 800°C.

(a) The (111) orientation implanted at 600°C.

(b) The (100) orientation implanted at 600°C.

(c) The (111) orientation implanted at room-temperature.

(d) The (100) orientation implanted at room-temperature.

Fig. 7 All specimens were implanted with 2×10^{16} pt/cm^2 at 100 KeV and then annealed for 20 min. at 900°C.

(a) The (111) orientation implanted at 600°C.

(b) The (100) orientation implanted at 600°C.

(c) The (100) orientation implanted at room-temperature.

(d) The (100) orientation implanted at 600°C.

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(100)

Annealing Temperature °C	Implanted at Room Temp. Ω/□	Implanted at 600°C Ω/□
Room Temp.	115.7	35.56
400	37.4	32.96
600	16.33	29.9
800	12.66	11.97
900	9.09	8.63

(111)

Annealing Temperature °C	Implanted at Room Temp. Ω/□	Implanted at 600°C Ω/□
Room Temp.	156.42	53.34
400	43.28	47.87
600	25.72	4668
800	13.9	13.42
900	9.96	9.10

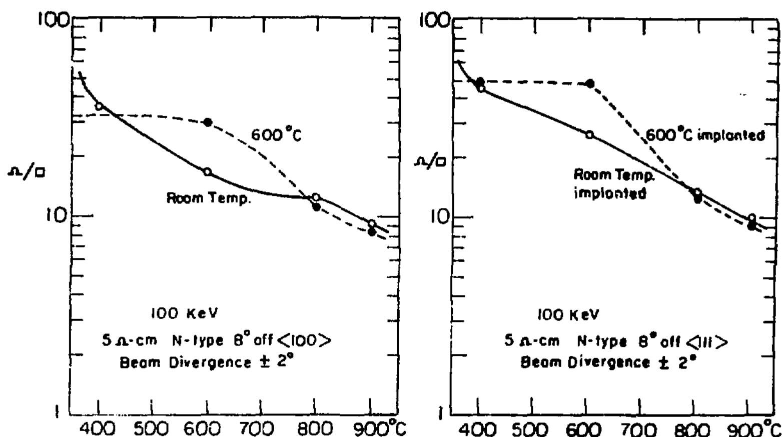

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Fig. 1