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A SEM TECHNIQUE FOR EXPERIMENTALLY LOCATING LATCH-UP PATHS IN INTEGRATED CIRCUITS*

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CONF-800703--1

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Latch-up in present bulk CMOS integrated circuits can be prevented by processing techniques such as lifetime control (gold doping[1] and neutron irradiation[2]), the use of epitaxial substrates[3], or by design layout techniques. In order to employ design solutions it is necessary to locate and analyze the latch-up paths in a given design; this analysis is complicated by the enormous number of possible paths present. Prevention of latch-up is presently accomplished primarily through processing techniques. These were easily found and proved to be effective generic solutions. The determination of actual latch paths has not been necessary.

However, future small geometry circuits may prove immune to some processing techhiques for latch-up prevention. Thus, the use of design layout solutions may become necessary to achieve latch-up control. This will require a practical technique for experimentally determining the latch paths in a design so that the layout can be corrected.

We present here a technique for using the scanning electron microscope (SEM) in the electron-beam-induced current (EBIC) mode to delineate latch-up paths in CMOS ICs. In the EBIC mode, the current produced by the collection and separation of the electron-beam-generated electron-hole pairs in the space charge regions of the device is measured and used to form an image. Since the collection of these carriers is dependent on space charge region width (and thus junction potential), anything that alters the depletion layer width will affect the collection efficiency. In particular, in a latch condition the junctions involved in the latch will be biased differently from those which are not, and thus the EBIC signal from those regions should be measurably different.

A simplified schematic of the circuit used in this technique is shown in Fig. 1. The EBIC current amplifier is connected between V_{SS} and V_{DD}, i.e., across the p-well/substrate junction, since this junction must be involved in the latch somewhere on the chip. The chip is latched by applying a voltage between any pads through which a latch can be

*This work supported by the U.S. Department of Energy.

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induced; in the figure the voltage is applied between V_{DD} and V_{SS}, as is usually done to induce latch-up through overvoltage stress. The coupling capacitor at the current amplifier input is necessary to prevent saturation of the amplifier from the applied DC voltage.

To validate the technique, it was employed on the RCA CD4007 where latch paths can be easily determined from consideration of the layout and applied bias. Fig. 2 shows the EBIC picture obtained when the circuit is not latched. Figure 3 is the image when the chip is latched by applying a positive voltage to the input protection diode at pin 3 and a negative voltage to the n+ source at pin 9 (see Fig. 4 where the EBIC photograph is superimposed on a secondary electron image showing the chip topography). The areas of the chip involved in the latch show up clearly as the brightest areas in this EBIC mode; when the 4007 is latched through a different input or output, different areas then become bright. The EBIC image obtained is very different from that for the unlatched chip (Fig. 2), or that for an avalanching junction.

That this technique is readily adaptable to an LSI circuit is shown in Fig. 5; a commercial 1K RAM was latched by overvoltage stress with all inputs at ground. The superimposed secondary electron and EBIC image shows clearly the latched area near the output buffer; a magnification of the latched area is shown in Fig. 6.

The experimental technique will be discussed in further detail, as will results for LSI circuits indicating where latch paths were found and the associated design implications.

References

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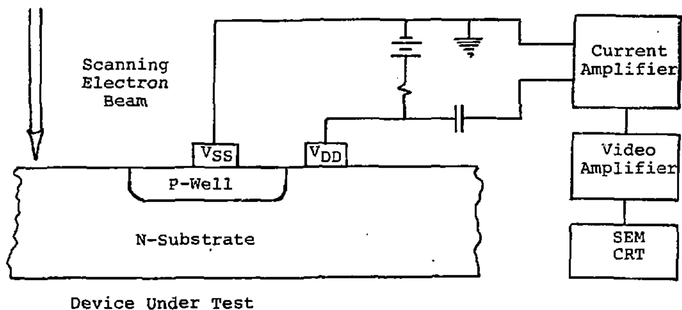

Figure 1. Schematic of EBIC Circuit for Detection of Latch-Up Paths

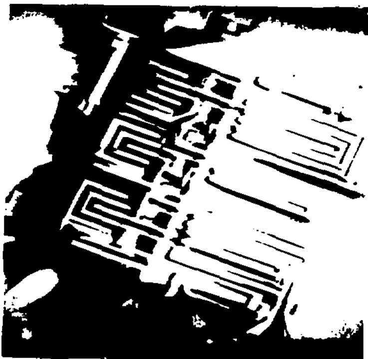

Figure 2. EBIC Image of the CD4007 in Unlatched Condition

Figure 3. EBIC Image of the CD4007 when Latched Between Pins 3 and 9.

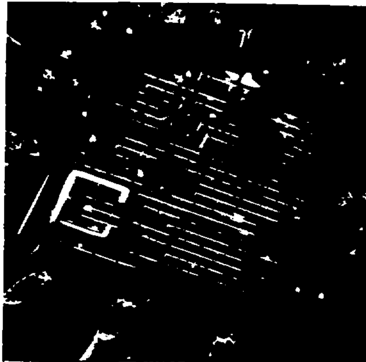

Figure 4. Superimposed Secondary Electron and EBIC Images of the CD4007 when Latched Between Pins 3 and 9.

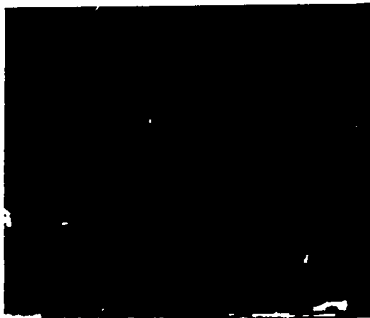

Figure 5. Superimposed Secondary Electron and EBIC Images of a Commercial 1K RAM when Latched by Overvoltage stress.

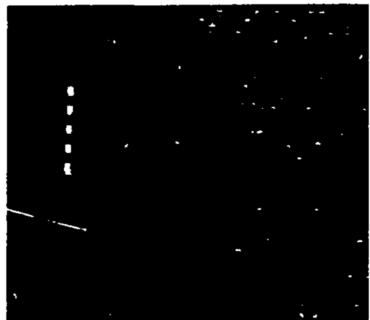

Figure 6. Enlargement of Latched Output Buffer Area from Fig. 5.