BNL-28117

CONF-800724--10

July 14, 1980

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First Experiences with a Fastbus system at Brookhaven

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Abstract

First experiences with a Fastbus system at Brookhaven.* L. B. Leipuner, R. C. Larsen, D. S. Makowiecki, W. M. Morse, T. K. Rudolf, W. P. Sims (Brookhaven National Laboratory), R. K. Adair, J. K. Black, S. R. Blatt, M. K. Campbell, H. Kasha, M. P. Schmidt (Yale University). A new concept in high energy data acquisition systems called Fastbus has been developed and implemented at Brookhaven. The system which is capable of sub-gigabit/sec speeds has been operating for some time now. A number of modules including an on-bus processor, a PDP11 interface, 32 channel coincidence latches, a 16 channel scaler, a 32 channel μ-clock device, a 60 nsec memory and a pre-determined time module have been developed and built. Features of the system include extensive use of ECL logic and a water cooled crate with conduction heat transfer within a module. The system is used in an on-line experiment at the AGS. Operating experience will be discussed.

*This work was supported in part by the U.S. Department of Energy under Contract No. DE-AC02-76CH00016.

Experiment #735, now being executed at the A.G.S. is implemented in FASTBUS. This is, to our knowledge, the first experiment to be done using this system. Briefly this data acquisition system is designed to operate and gather data from high energy physics experiments at sub-microsecond speeds. It is a 32 bit bus system capable of operating at near-gigabit rates. The bus can be segmented with each segment operating asynchronously when not communicating with each other. The system is based upon a very fast integrated circuit family, emitter coupled logic or ECL.

The experiment is described in another paper at this conference. Figure 1 is a schematic of the experimental apparatus. An event is accepted if a pair of charged particles originate in the space before the detectors and one, presumably a μ meson, stops and produces a detected decay in the polarimeter. All of the detectors are scintillation counters. There are more than 200 counters used and most are monitored individually. Each counter is connected to a NIM descriminator and most of the logic is done in a special trigger circuit built for the purpose. Most of the trigger logic is built with ECL but, having been built for a previous experiment, not in FASTBUS format. The apparatus is cylindrically symmetric with the finest segments 1/32 of 360° azimuthal angle width.

Most of the discriminators are directly connected to a set of 7, 32 channel × 2 deep, latches. Each real trigger is followed by a automatic second trigger to the latches to provide accidental information. These coincidence latches, capable of ∿ 3 nsec resolutions are the main input paths for data at the event level. The other path is through the μ clock device which contains 32, 100 nsec/tick, clocks. These clocks are all reset and started by a trigger and stopped by a pulse from the G counter presumably from the positron from the μ decay. They time out at 6.4 μsec. Figure 2 displays the data sources.

The counters, besides being connected to the latches are connected to trigger logic and to a "BOX" finder. The trigger logic looks for one of 6 types of triggers. The type is passed to the computer by setting one of the latches and the "OR" of all types triggers further data processing. The box finder determines which clocks to read and again passes the data on through the latches. The trigger logic provides information for scalers that keep track of the experiment on an accelerator pulse by pulse basis.

Data from the latches and clocks is passed to a processor which rejects events which are patently impossible and edits the data. Latch bits are translated to latch addresses. Only the clocks adjacent to the stopping block are read. All the encoded data for good events, is passed to a fast ($\sim$ 60 nsec) memory. The 4K by 16 bit memory can store $\sim$ 400 events, more than a single accelerator pulses worth. The controller inhibits the trigger while it is taking data. A PDP11 is connected to the memory through an interface. The memory accepts data at FASTBUS rates and sends it to the PDP11, on demand, at its rate. Synchronization with the AGS is provided by a predetermined time module. This module also contains an I/O register used to sense and control other parts of the experiment including the trigger logic. Figure 3 shows these paths.

Figure 4 depicts the FASTBUS view of the system. The horizontal line depicts the bus segment. There are 9 slave devices shown as circles and 3 master devices shown as rectangles on the bus. Slave devices do not initiate bus transactions whereas master devices can. The latches are only read in this experiment although there are masks within them which can be written to in a different environment. The predet can act as master or a slave but is depicted as a master. The controller acts only as a master and the

interface again can be either. The interface allows transactions between the PDP11's unibus and FASTBUS to take place. It also functions somewhat as a bus master taking care of such tasks as bus arbitration and broadcast commands. There is an interrupt facility included in it allowing, for this experiment, the predet module to interrupt the PDP11 at the beginning of beam, at the end of beam, and at another time when data can be read from late devices such as the A.G.S. intensity monitor.

The latch module is a coincidence latch device. It has a resolution of about 3 n noseconds. There are 32 channels in the device and each is double buffered. In this experiment each trigger is followed by another one some 75 nanoseconds later to give a measure of accidentals. The double buffering allows this without appreciable time penalty. The latches contain an elaborate masking arrangement to disable or enable latches quickly and individually. This feature is not used in this experiment. A single read presents the 32 bits to the bus.

The μ-clock module has 32 channels. It is designed to measure the time between a μ entering the polarimeter and its decay. Thirty-two 6 bit counters connected to a single crystal controlled oscillator are started with the trigger. If an input pulse is present sometime after that the counter is stopped. If none is present by time 6.4 μsec have elapsed the clock is stopped anyhow. A separate address on the bus is used to read each clock.

Memory is 4K words by 16 Bits and has a complete cycle time of some 60 nanoseconds. It can be re-configured with jumpers to operate as 2K × 32. There are three modes of operation; random access, first in-first out (FIFO) or first in-last out (FILO). Modules can be cascaded so that FIFO and FILO modes can extend over several modules. The memory is used in FIFO mode in this experiment with the controller feeding data to the memory at its pace and the PDP11 reading data at its pace.

The predet counts timing pulses from the A.G.S. It has within it a register which can be set by the PDP11. When there is a match between the counter and the register a write to the interface interrupt register is made. The match register is set first to "beam on" time. When that condition is satisfied the PDP11 is interrupted and "beam off" time is written to the match register. A third time is written when that match is made, etc. The cycle is repeated for each accelerator pulse. This module has a 16-bit general input register, a 16 bit general output register and a 1 bit inhibit register built in. The inhibit register listens to broadcast commands. If inhibit-on or inhibit-off is broadcast, this register goes on or off. It is used to inhibit data taking between machine pulses. The general input register is used only, at present, to sense the polarity of a precision magnet which is changed each pulse. The output register blows some horns and whistles.

The 16 channel scaler has 28 bits per channel. It runs at 100 Mhz when the proper chip is plugged into its front end. Individual channels can be turned off or on directly or may be controlled by the broadcast inhibit commands. Channels may be individually cleared, be made to read and clear, or cleared by broadcast commands. The inhibit and broadcast clear functions are individually controlled for each channel individually.

The controller is based upon the 10800 bit slice processor set. We have avoided installing the arithmetic logic unit so it is not really a computer, yet. It is, however, a processor and has decision making elements in it. It also has a priority encoding register used to reduce latch bits to latch addresses at hardware speeds. The "BOX" inputs are used to decide which clock inputs to read. The latches and clocks are read, encoded and then passed on to the memory. The device is micro-programmed and the program resides at present on PROM's.

The PDP11 interface is designed to allow information transfer in either direction and to be initiated from either the PDP-11 or a FASTBUS device. The whole 2^{18} address space of the PDP11 is directly addressable from FASTBUS. All of FASTBUS is addressable from the PDP11 through a set of 8 mapping registers. The controller accepts interrupts for the 11 by having a register such that when addressed by a FASTBUS device causes interrupt. Another register can generate a FASTBUS broadcast which goes to all modules. This is used to generate simultaneous inhibits, clears, etc. Bus arbitration responsibility also resides here. Thirty-two bit reads and writes by the PDP11 are accomplished with the use of additional registers in the interface.

The system uses a rather novel and quiet convenient cooling system. The crate is water cooled with a 1/4 inch water line supplying more than enough cooling for a 1500 watts crate. The cooling lines would not be noticeable in the usual maze of coaxial cables if they were not white. Heat is transferred from the chips to the crate by several conduction paths. For modules which dissipate less than 30 watts simple conduction to the cover plates via a conducting rubber pad suffices. For modules with up to 75 watts of dissipation an aluminum lattus under the chips is also used. A simple wedge mechanism provides the necessary thermal contact between the crate and modules. The system is quiet, clean, and effective.

With the exception of the latch modules all devices were built on wire-wrap kludge boards. This has worked rather well and we have had no trouble cooling these modules even at 75 watts. The modules can accomodate about 265 standard 16 pin DIP packages.

As of this writing the system has operated for several weeks with the usual shake down of soft chips etc. We are quite satisfied with it.

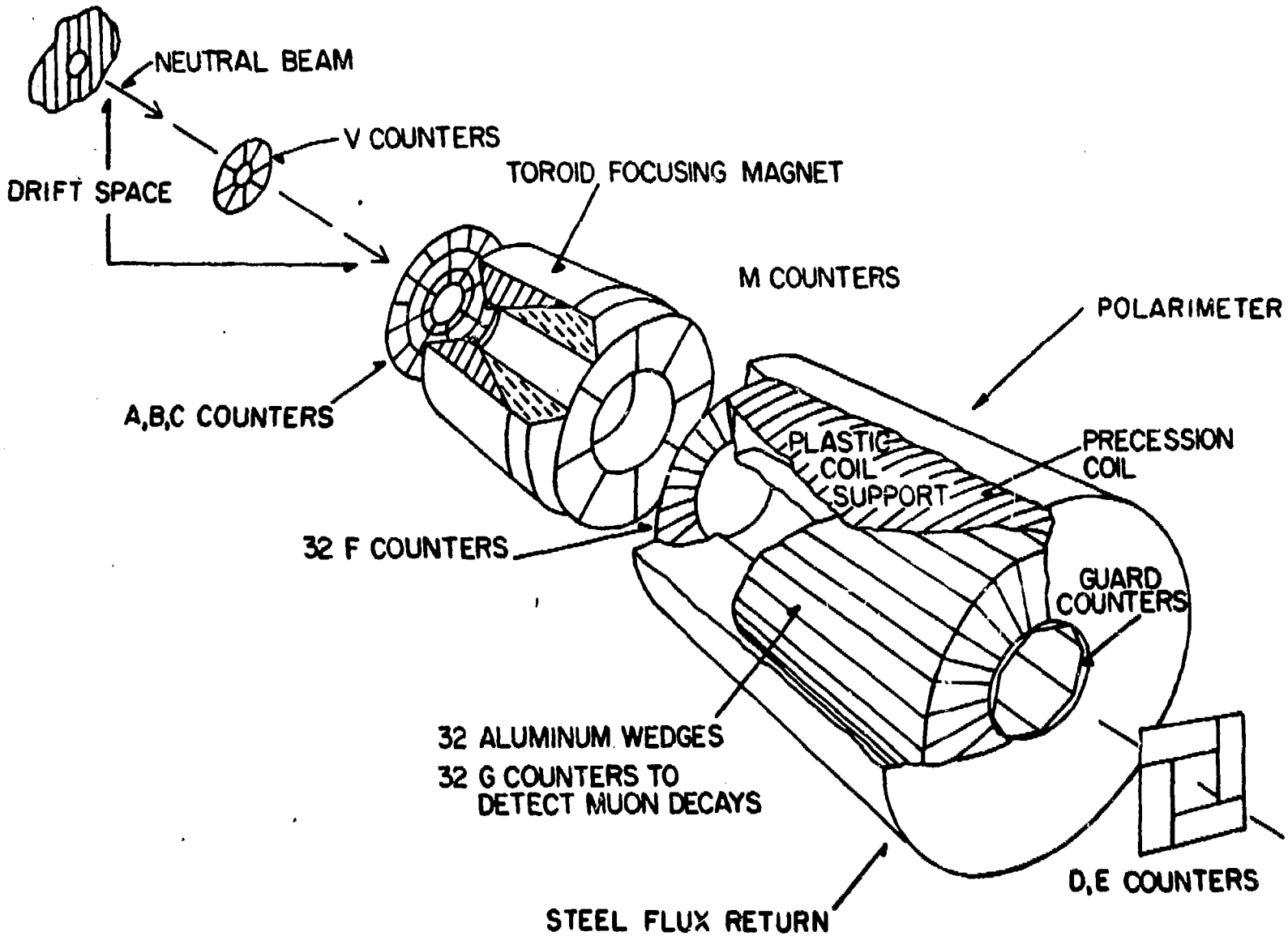

NEUTRAL BEAM
V COUNTERS
DRIFT SPACE
TOROID FOCUSING MAGNET
M COUNTERS
POLARIMETER
A,B,C COUNTERS
PLASTIC COIL SUPPORT
PRECESSION COIL
32 F COUNTERS
GUARD COUNTERS
32 ALUMINUM WEDGES
32 G COUNTERS TO DETECT MUON DECAYS
D,E COUNTERS
STEEL FLUX RETURN

Fig. 1

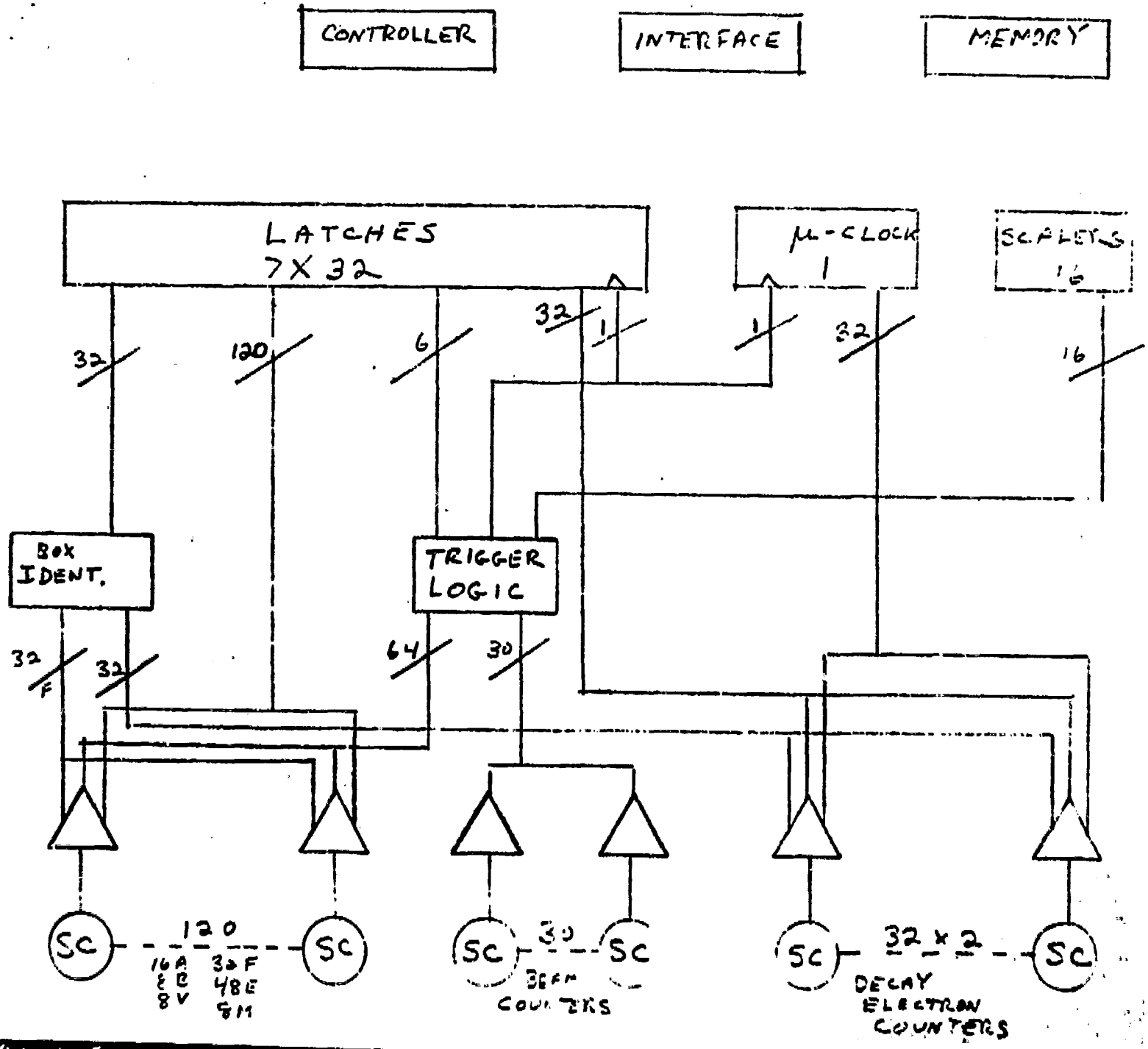

CONTROLLER
INTERFACE
MEMORY
LATCHES
7 X 32
μ-CLOCK
1
SCALERS
16
32
120
6
32
1
1
32
16
BOX
IDENT.
TRIGGER
LOGIC
32
32
64
30
SC
SC
SC
SC
SC
SC
120
16A
&
8V
32F
48E
&
81
30
BEAM
COUNTERS
32 x 2
DECAY
ELECTRON
COUNTERS

Fig 2

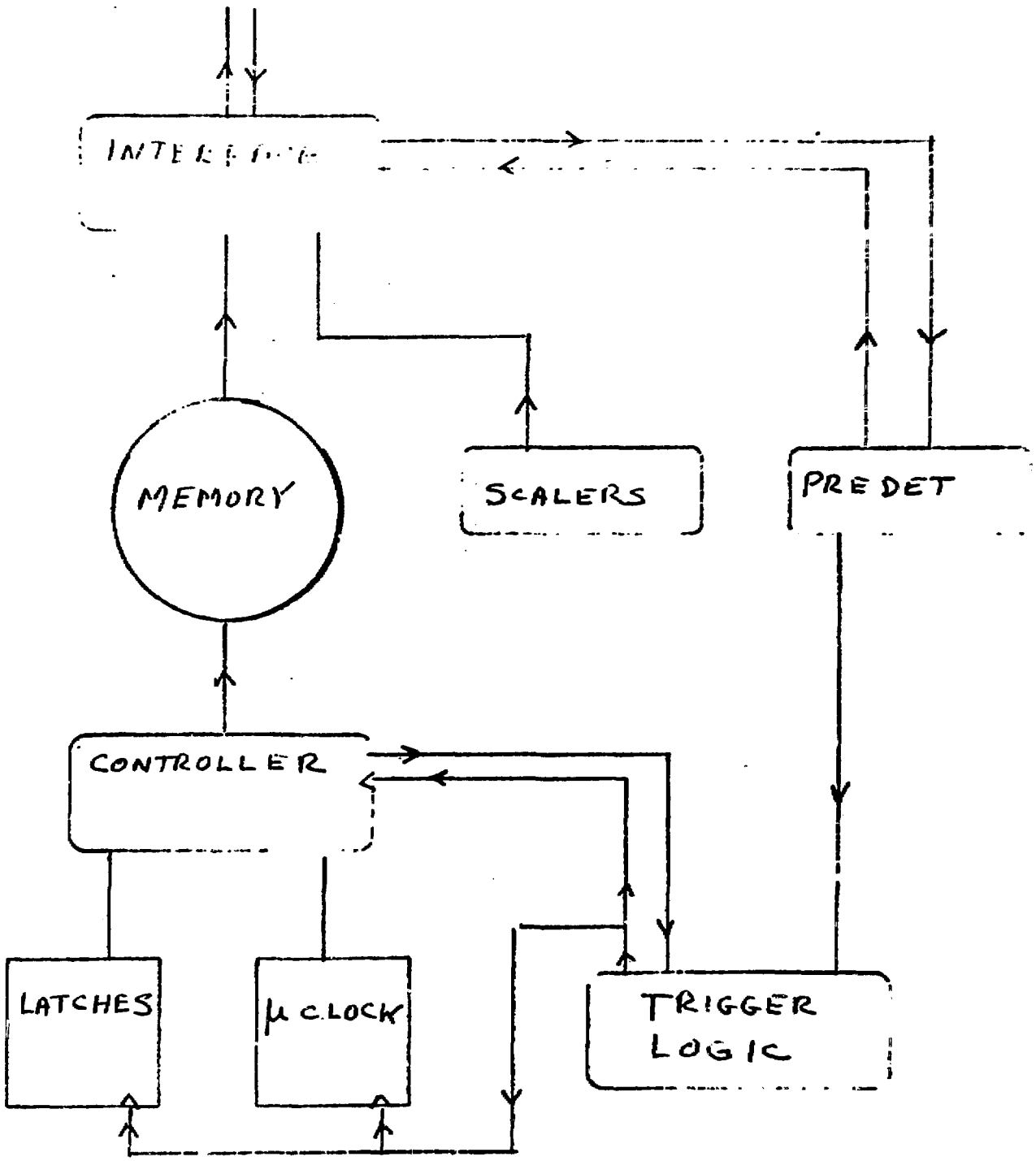
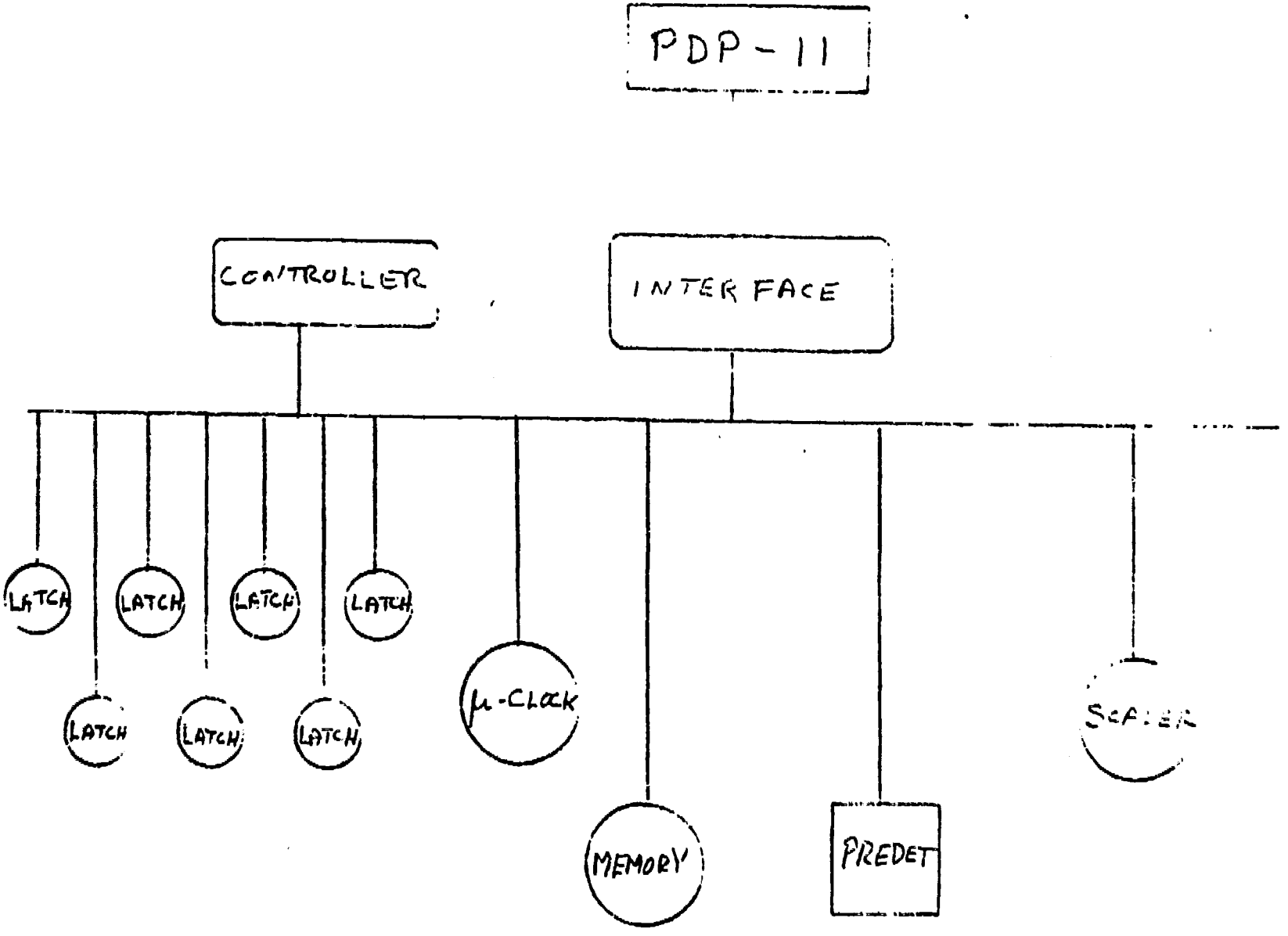

MEMORY
SCALERS
PREDET
CONTROLLER
LATCHES
μ CLOCK
TRIGGER
LOGIC

FIG 3


PDP-11
CONTROLLER
INTERFACE
LATCH
LATCH
LATCH
LATCH
LATCH
LATCH
LATCH
μ-CLOCK
MEMORY
PREDET
SCALER

FIG