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A FASTBUS SYSTEM USED IN A HIGH ENERGY EXPERIMENT

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Experiment #735, now being executed at the A.G.S. is implemented in FASTBUS. This is, to our knowledge, the first experiment to be done using this system. Briefly, this data acquisition system is designed to operate and gather data from high energy physics experiments at sub-microsecond speeds. It is a 32 bit bus system capable of operating at near-gigabit rates. The bus can be segmented with each segment operating independently when not communicating with each other. The system is based upon a very fast integrated circuit family, emitter coupled logic or ECL.

The experiment is one designed to measure time reversal invariance violation in K^+ decay into π^0, μ^+, and ν. The actual physical quantity measured is the component of polarization of the μ-meson which is in a direction perpendicular to the plane of decay.

Figure 1 shows the apparatus schematically. A good event is one in which the following sequence of events takes place. A K^+ decays in the region called "drift space". The π^0 decays into 2 γ rays, one of which proceeds down the apparatus to the lead glass counter in the lower right corner of the drawing. The μ^+ meson strikes one of the counters A or B; traverses the toroidal focusing magnet; and stops in one of the aluminum wedges of the polarimeter. The μ meson precesses in the weak magnetic field and then decays within 6.4 usec of stopping. The decay positron is detected by one of the 32 G counters.

All of the detectors are scintillation counters. There are more than 200 counters used and most are monitored individually. Each counter is connected to a NIM discriminator and most of the logic is done in a special trigger circuit built for the purpose. Most of the trigger logic is built with ECL but, having been built for a previous experiment, not in FASTBUS format. The apparatus is cylindrically symmetric with the finest segments 1/32 of 360° azimuthal angle width.

Most of the discriminators are directly connected to a set of 7, 32 channel × 2 deep, latches. Each real trigger is followed by a automatic second trigger to the latches to provide accidental coincidence information. These coincidence latches, capable of ∿ 3 nsec resolutions, are the main input paths for data at the event level. The other path is through the μ clock device which contains 32, 100 nsec/tick, clocks. These clocks are all reset and started by a trigger and stopped by a pulse from the G counter presumably from the positron from the μ decay. They time out at 6.4 μsec. Figure 2 displays the data sources. The counters, besides being connected to the latches, are connected to the trigger logic and to a "BOX" finder. The trigger logic looks for one of 6 types of triggers. The type is passed to the computer by setting one of the latches and the "OR" of all types triggers further data processing. The box finder determines which clocks to read and again passes the data on through the latches. The trigger logic provides information for scalers that keep track of the experiment on an accelerator pulse by pulse basis.

Data from the latches and clocks is passed to a processor which rejects events which are patently impossible and edits the data. Latch bits are translated to latch addresses. Only the clocks adjacent to the stopping block are read. All the encoded data for good events is passed to a fast (∿ 60 nsec) memory. The 4K by 16 bit memory can store ∿ 400 events, more than a single accelerator pulse's worth. The controller inhibits the trigger while it is taking data. A PDP11 is connected to the memory through an interface. The memory accepts data at FASTBUS rates and sends it to the PDP11, on demand, at its rate. Synchronization with the AGS is provided by a predetermined time module. This module also contains an I/O register used to sense and control other parts of the experiment including the trigger logic. Figure 3 shows these paths.

Figure 4 depicts the FASTBUS view of the system. The horizontal line depicts the bus segment. There are 9 slave devices shown as circles and 3 master devices shown as rectangles on the bus. Slave devices do not

initiate bus transactions whereas master devices can. The latches in this experiment are only read although there are masks within them which can be written to in a different environment. The predet can act as a master or a slave but is depicted as a master. The controller acts only as a master and the interface again can be either. The interface allows transactions between the PDP11's unibus and FASTBUS to take place. It also functions somewhat as a bus master taking care of such tasks as bus arbitration and broadcast commands. There is an interrupt facility included in it allowing, for this experiment, the predet module to interrupt the PDP11 at the beginning of beam, at the end of beam, and at another time when data can be read from late devices such as the A.G.S. intensity monitor.

The latch module is a coincidence latch device. It has a resolution of about 3 nanoseconds. There are 32 channels in the device and each is double buffered. In this experiment each trigger is followed by another one some 75 nanoseconds later to give a measure of accidentals. The double buffering allows this without appreciable time penalty. The latches contain an elaborate masking arrangement to disable or enable latches quickly and individually. This feature is not used in this experiment. A single read presents the 32 bits to the bus.

The μ-clock module has 32 channels. It is designed to measure the time between a μ entering the polarimeter and its decay. Thirty-two 6 bit counters connected to a single crystal controlled oscillator are started with a trigger. If an input pulse is present sometime after that the counter is stopped. If none is present by the time 6.4 μsec have elapsed the clock is stopped anyhow. A separate address on the bus is used to read each clock.

Memory is 4K words by 16 Bits and has a complete cycle time of some 60 nanoseconds. It can be re-configured with jumpers to operate as 2K × 32. There are three modes of operation; random access, first in-first out (FIFO) or first in-last out (FILO). Modules can be cascaded so that FIFO and FILO modes can extend over several modules. The memory is used in FIFO mode in this experiment with the controller feeding data to the memory at its pace and the PDP11 reading data at its pace.

The predet counts timing pulses from the A.G.S. It has within it a register which can be set by the PDP11. When there is a match between the counter and the register, a write to the interface interrupt register is made. The match register is set first to "beam on" time. When that condition is satisfied the PDP11 is interrupted and "beam off" time is written to the match register. A third time is written when that match is made, etc. The cycle is repeated for each accelerator pulse. This module has a 16-bit general input register, a 16 bit general output register and a 1 bit inhibit register built in. The inhibit register listens to broadcast commands. If inhibit-on or inhibit-off is broadcast, this register goes on or off. It is used to inhibit data taking between machine pulses. The genral input register is used only, at present, to sense the polarity of the precessing magnet which is changed each pulse. The output register is used for annunciators.

The 16 channel scaler has 28 bits per channel. It runs at 100 Mhz when the proper chip is plugged into its front end. Individual channels can be turned off or on directly or may be controlled by the broadcast inhibit commands. Channels may be individually cleared, be made to read and clear, or cleared by broadcast commands. The inhibit and broadcast clear functions are individually controlled for each channel individually.

The controller is based upon the 10800 bit slice processor set. We have avoided installing the arithmetic logic unit so it is not really a computer, yet. It is, however, a processor and has decision making elements in it. It also has a priority encoding register used to reduce latch bits to latch addresses at hardware speeds. The "BOX" inputs are used to decide which clock inputs to read. The latches and clocks are read, encoded and then passed on to the memory. The device is micro-programmed and the program resides at present on PROM's.

The PDP11 interface is designed to allow information transfer in either direction and to be initiated from either the PDP-11 or a FASTBUS device. The whole 2^{18} address space of the PDP11 is directly addressable from FASTBUS. All of FASTBUS is addressable from the PDP11 through a set of 8 mapping registers. The controller accepts interrupts for the 11 by having a register such that when addressed by a FASTBUS device causes an interrupt. Another register can generate a FASTBUS broadcast which goes to all modules. This is used to generate simultaneous inhibits, clears, etc. Bus arbitration responsibility also resides here. Thirty-two bit reads and writes by the PDP11 are accomplished with the use of additional registers in the interface.

The system uses a rather novel and quite convenient cooling system. The crate is water cooled with a 1/4 inch water line supplying more than enough cooling for a 1500 watts crate. The cooling lines would not be noticeable in the usual maze of coaxial cables if they were not white. Heat is transferred from the chips to the crate by several conduction paths. For modules which dissipate less than 30 watts simple conduction to the cover plates via a conducting rubber pad suffices. For modules with up to 75 watts of dissipation an aluminum lattice under the chips is also used. A simple cam mechanism provides the necessary thermal contact between the crate and modules. The system is quiet, clean and effective.

With the exception of the latch modules all devices were built on wire-wrap "kludge" boards. This has worked rather well and we have had no trouble cooling these modules even at 75 watts. The modules can accommodate about 265 standard 16 pin DIP packages.

The system has been used for about 500 hours of data taking. This winter the experiment will run for about another 1000 hours. For this next run the processor has been re-fitted with a RAM program memory in order to allow more rapid changes in its program. The "BOX" finder has been moved to the FASTBUS to accommodate additional counters and to eliminate some timing ambiguities in the system. The ease with which these changes can be made is impressive.

The next approved experiment to be done here with this equipment is E749. This will use a multi-segment system with both crate and cable segments. In addition to the modules described above we will also have the following. A crate to cable segment interconnect as well as a cable to crate segment interconnect will be developed. The multi-crate system will be interconnected with cable segments. Figure 5 illustrates this principle. The pulse height of some 160 lead glass counters will be read by FASTBUS ADC modules to be developed. Some 2500 wires of a proportional wire chamber system will be read. The plan at this time is to make the chambers part of a cable FASTBUS segment. Some logic will be done on the chambers themselves.

Much of the work now done in NIM modules can be done much less expensively now with ECL logic. We plan to make computer controlled discriminator for E749. They will not only have their thresholds and widths set by FASTBUS but we also plan to do our timing digitally with this system. It greatly reduces set-up time and makes much more effective use of accelerator time.

A feature of this system is its simple protocol and addressing. By concentrating on a simple tree structured system great simplicities can be obtained. The system is not restricted to tree structures but rather is optimized for them. This system provides automatic communications between segments only when needed. Paths are established by address assignments using a simple, easy to understand algorithm. Centralized facilities such as priority arbitration and broadcast are possible as there is only 1 segment interconnect leading into a segment in the primary system. There may of course, be many outgoing ones. Priorities can be changed dynamically to provide equal or partially biased orders. Broadcasts are handled in segment interconnects and require no additional hardware in master modules to originate these transactions.

Table 1 contains a list of modules which have been built and debugged as well as a partial list of new modules being worked on at this time using this protocol.

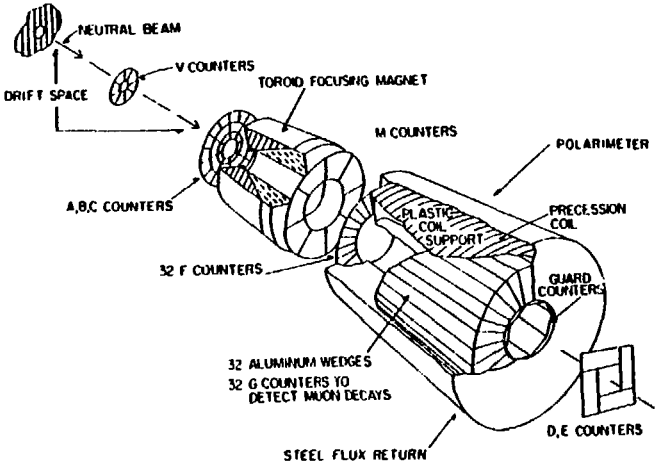
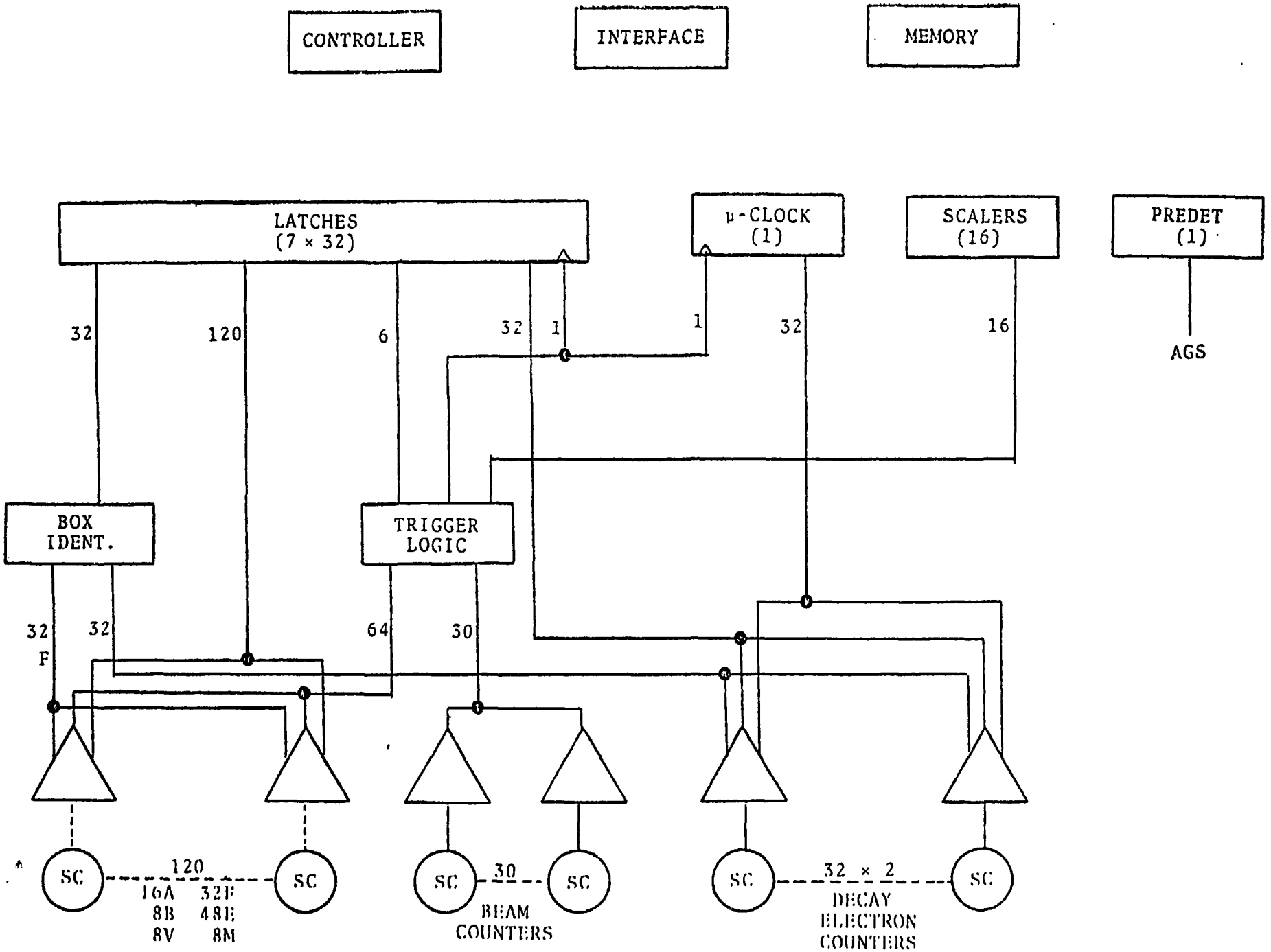

NEUTRAL BEAM
V COUNTERS
DRIFT SPACE
TOROID FOCUSING MAGNET
M COUNTERS
POLARIMETER
A,B,C COUNTERS
PLASTIC COIL SUPPORT
PRECESSION COIL
32 F COUNTERS
GUARD COUNTERS
32 ALUMINUM WEDGES
32 G COUNTERS TO DETECT MUON DECAYS
D,E COUNTERS
STEEL FLUX RETURN

Fig. 1


CONTROLLER
INTERFACE
MEMORY
LATCHES
(7 × 32)
μ-CLOCK
(1)
SCALERS
(16)
PREDET
(1)
AGS
32
120
6
32
1
1
32
16
BOX
IDENT.
TRIGGER
LOGIC
32
F
32
64
30
SC
120
16A 32F
8B 48E
8V 8M
SC
SC
30
SC
BEAM
COUNTERS
SC
32 × 2
DECAY
ELECTRON
COUNTERS
SC

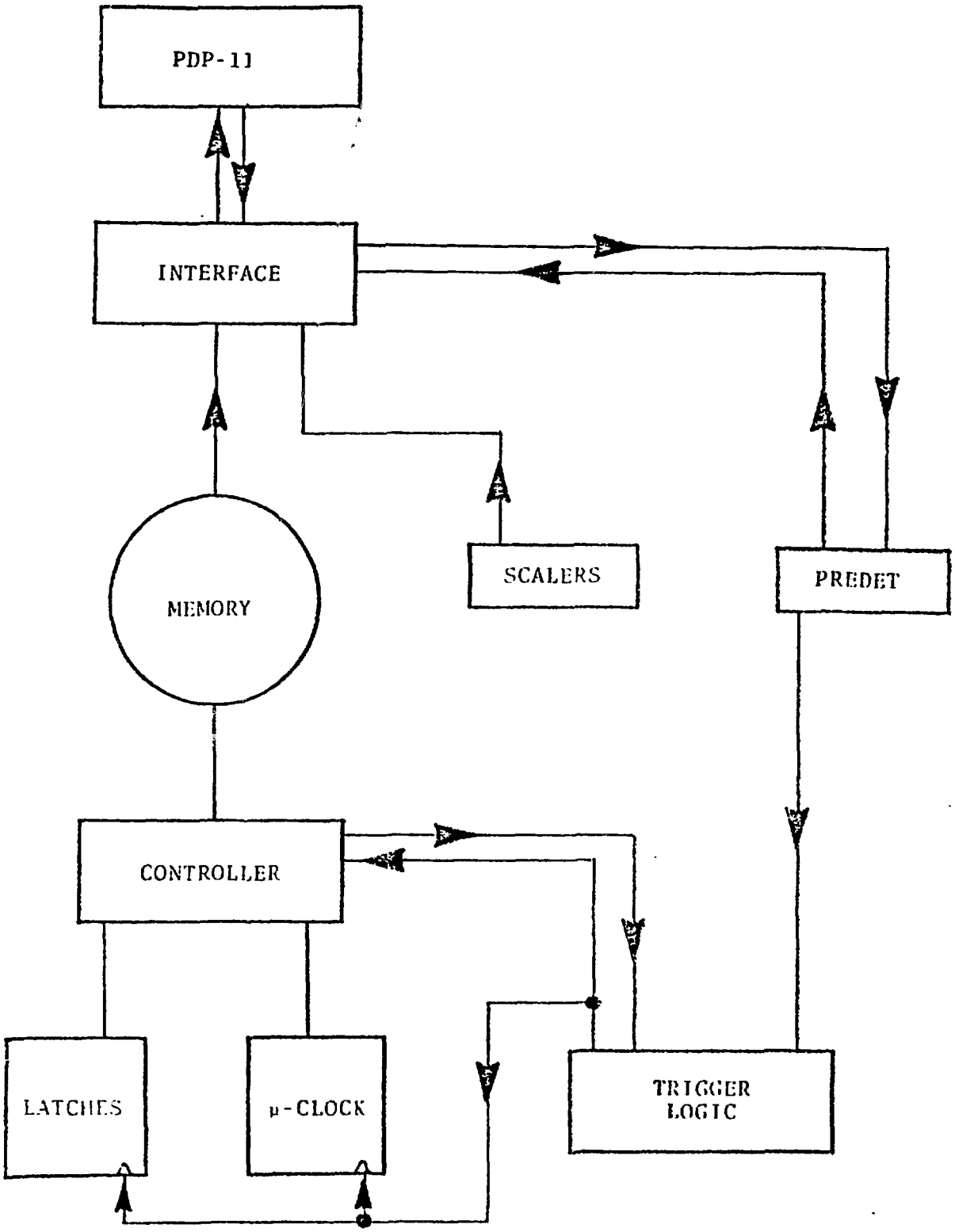
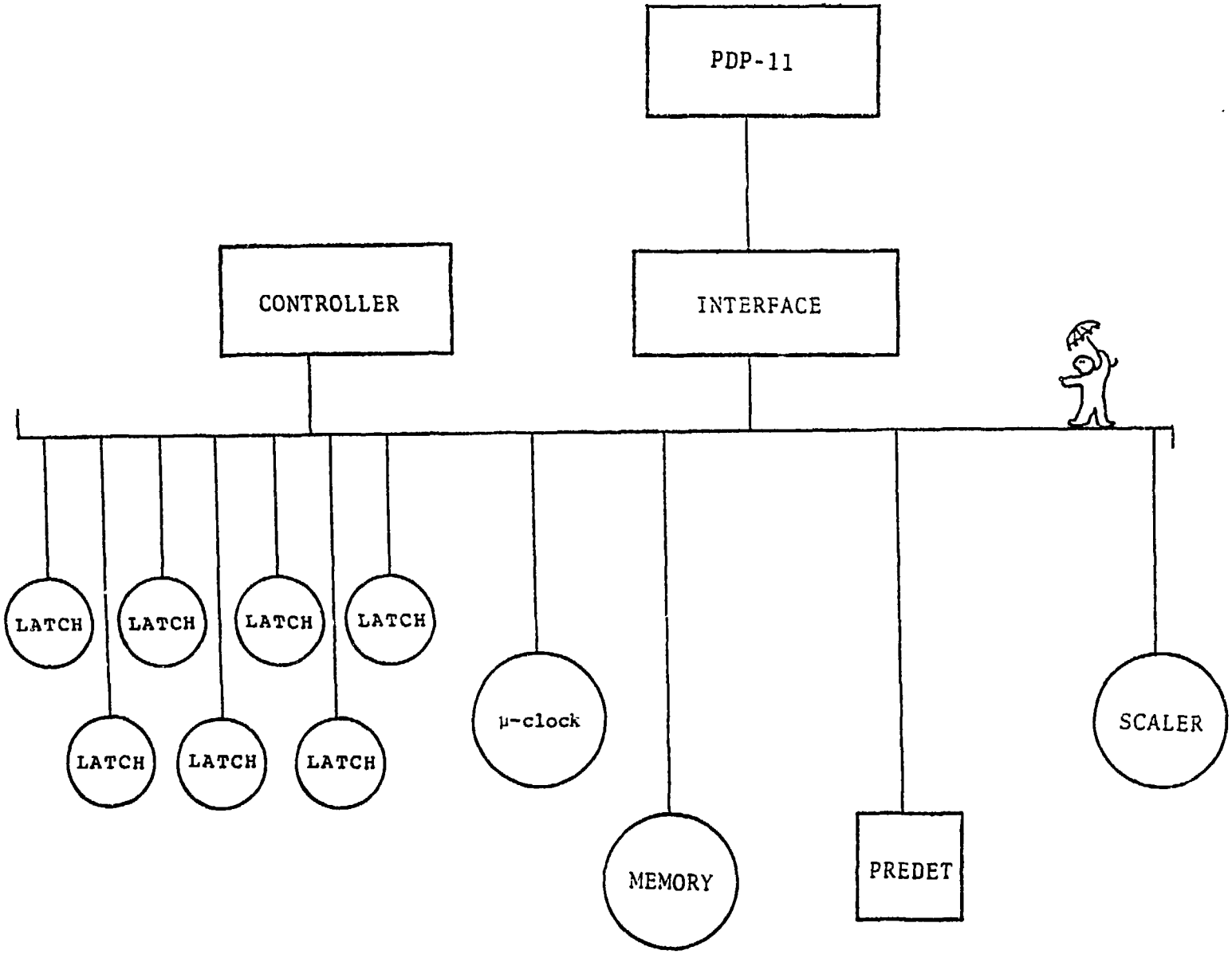

PDP-11
INTERFACE
MEMORY
SCALERS
PREDET
CONTROLLER
LATCHES
μ-CLOCK
TRIGGER
LOGIC

Fig. 3


PDP-11
CONTROLLER
INTERFACE
LATCH
LATCH
LATCH
LATCH
LATCH
LATCH
LATCH
μ-clock
MEMORY
PREDET
SCALER

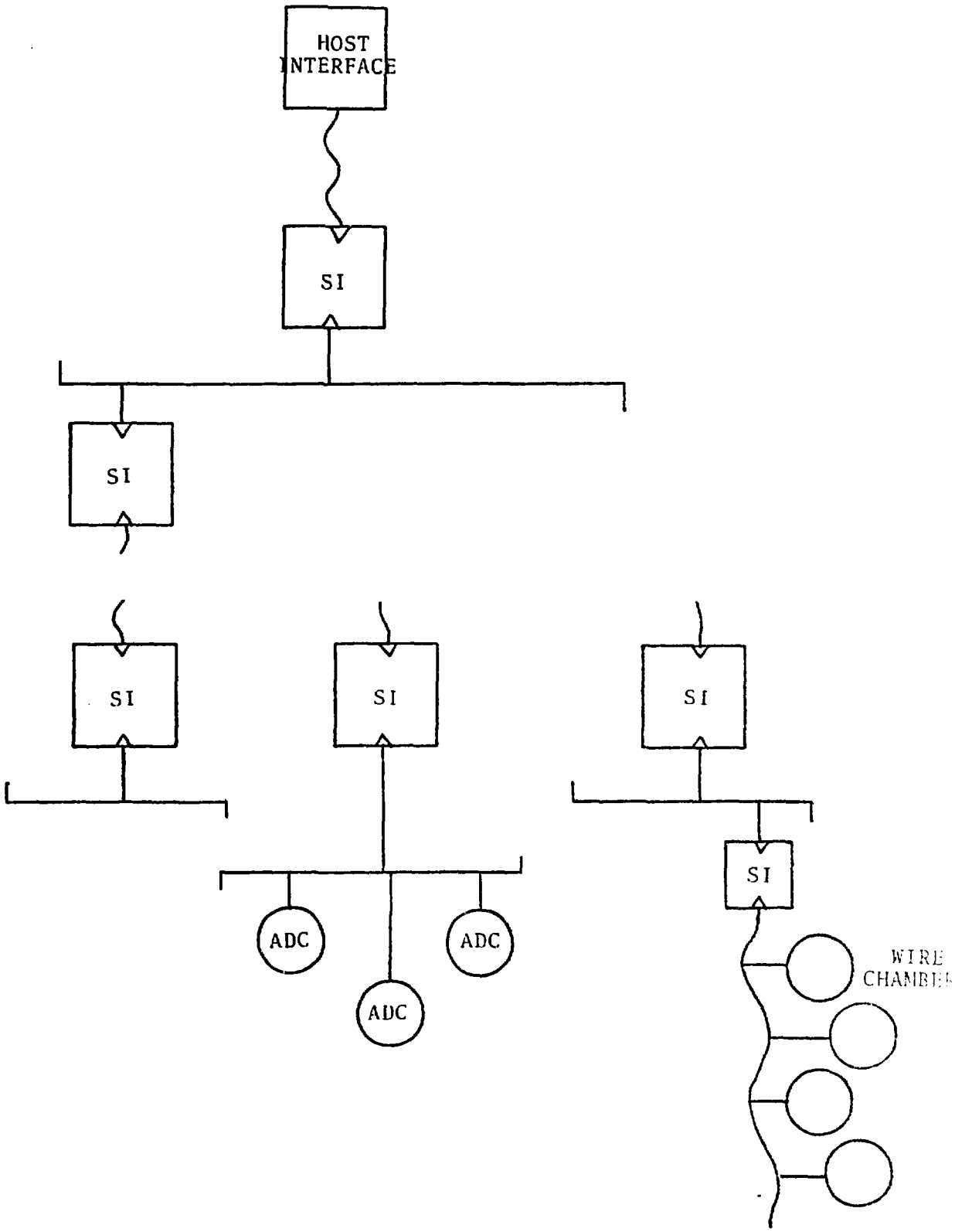


Fig 5

FASTBUS PROTOTYPE WORK AT BROOKHAVEN NATIONAL LABORATORY

FB Water Cooled Crate*	D. Makowiecki/W. Sims
FB Conduction Cooled Module*	D. Makowiecki/W. Sims
FB to PDP11 Interface Alternate Protocol*	T. Rudolf
FB 16 Channel Latch Alternate Protocol*	D. Makowiecki
FB Memory Alternate Protocol*	W. Morse
FB Controller (2 Modules) Alternate Protocol*	M. Campbell
FB Muon Clock 32 Channel Alternate Protocol*	W. Morse/S. Blatt
FB 16 Channel 24 Bit Scaler 30 MHz Alternate Protocol*	L. Leipuner
FB 16 Channel 32 Bit Scaler 100 MHz Alternate Protocol*	D. Makowiecki
FB Test Box Alternate Protocol*	T. Rudolf
FB Pre-determined Timer Alternate Protocol*	H. Kasha
FB Kludge Card Alternate Protocol*	D. Makowiecki
FB Temperature Test Conduction Cooled Module*	D. Makowiecki
FB NIM to ECL to NIM Level Converter Type W Module*	T. Rudolf
FB Segment Interconnect Alternate Protocol	T. Rudolf
FB X# Channel ADC Alternate Protocol	L. Leipuner
FB X# Channel Discriminator Alternate Protocol	L. Leipuner
FB Proportional Wire Chamber Alternate Protocol	L. Leipuner
FB 2nd Generation Host Interface to PDP11's Alternate Protocol	T. Rudolf
FB on Card Switching Power Supplies	L. Leipuner

* Units debugged and operational.

Table 1.

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