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Mini- and Micro-Processors and Fastbus in the Experimental Program at BNL

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——— DISCLAIMER ———

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The use of small processors in the experimental program at Brookhaven will
be reviewed. FASTBUS, a new data acquisition system, as developed at BNL.
will also be reviewed. New directions that are planned in these areas
will be discussed.

At this time there are three efforts at Brookhaven which are at all unusual. One is
the extensive mini-computer network used in a ν-e scattering experiment, E734. Another
effort is the experiment which explores the concept of using a large number of microprocessors
to replace or supplement a large processor for off-line or on-line data processing. These
two efforts are described in papers published in these proceedings so I will only comment
upon them in this writing.

Our detectors have become quite sophisticated (complex) in recent years. Large scintil-
lation counters with photomultipliers at each end provide some position information from
the difference in arrival time at the photomultiplier. The sum of times provides position-
independent event times. Drift chambers, of course, provide much of their position informa-
tion from the delay of the signal at the detecting wires. The ν-e scattering group has
dealt with the data acquisition problem by tagging each unit of data with the time, as well
as the position and magnitude of the signal. The pattern recognition then must operate in
four rather than three dimensions. In this experiment the data rate is small so the added
burden is small and an essentially dead-timeless system results. It will be interesting to
see if the technique extends to higher rate experiments.

The costs for computing the data from experiments can approach or exceed the other
costs of an experiment. One approach to reducing these costs, the use of large numbers of
inexpensive microprocessors, has been explored by a group at BNL. Many microprocessors are
being developed and the business is fiercely competitive. Their results and extrapolations
are described in Paper No. 57.

The needs of present and future experiments exceeds the presently available standards
for electronic systems. The detectors available can easily provide data at rates exceeding
present system capability if used in simple ways. Multi-level triggers and trigger abort
systems require a much more sophisticated system than is presently generally available.
FASTBUS is therefore being developed.

At Brookhaven we have developed, and used for about a year now, a FASTBUS system. It
may be true that someone here is not familiar with the system. For this person I will pro-
vide a review of its important properties. The system is primarily a segmented computer
bus system. It is segmented so that groups of devices may communicate simultaneously. Only
when devices on different segments communicate are any segments connected together. Devices
are addressed with 32 binary bits allowing for about 4×10^9 locations. This number is

large enough to match computers and memories expected for the next decade. Data words are also 32 bits wide to accommodate large bandpass or data rates. Data may be transferred in single words or in blocks of words. The data transaction may be done in handshake mode in which the transmitting device and the receiving device each acknowledge each transfer. Approximately 10^7 32 bit words per second may be transferred in this mode. If a higher rate is required a non-handshake mode may be used for about three times the handshake rate, or about 10^9 bits per second. It is frequently necessary to speak to a number of units at the same time. The turn-on or clear of a group of scalers is an example of such a requirement. FASTBUS provides a broadcast mode for this purpose. In order to provide maximum speed and still be inexpensive the ECL level standard has been adopted for the bus. This allows the use of ECL integrated circuits to interface the bus to modules.

The Brookhaven effort has used a water-cooled, conduction-transfer system to carry away the heat generated by modules. Figure 1 shows such a crate. Heat from the circuits is transferred to the edges of modules by conduction. Either the cover plate of the module which makes thermal contact with I.C.s or a grid with segments under the chip or both is used to transfer heat to the module edges. A conducting layer in a multi-layer board could be used. The module is held in contact with the crate by means of a locking cam mechanism. The one-quarter inch tube that feeds cooling water to the crate is hardly noticeable in the forest of co-axial cables connected to the crate.

The Brookhaven system uses an architecture which is quite simple and very powerful. The system is basically tree structured, although it is possible to use non-tree paths. The basic tree structure allows great simplification of the whole system. Each segment in a FASTBUS system is connected to another one through a device called a segment interconnect, or SI. In a basic tree structure there is one and only one SI leading into the segment. There may be many SI's leading out of a segment, of course. Data transfer can be initiated in either direction through an SI and the data can pass in either direction. The single incoming SI provides a home for segment utilities such as the segment arbitrator which determines the next segment master. Unless there are greater than six masters in a segment, the time required for this arbitration is less than that required for a data transfer. Since this arbitration takes place during the previous transfer no additional time is required for arbitration. If there are more than six masters on the segment a time slightly greater than one transfer time is required. The incoming SI provides a natural home for broadcast protocol. Having the arbitrator centralized permits a dynamic rearrangement of priorities. Any master need only write to a register in the SI to cause a broadcast.

It is perhaps worthwhile to discuss here the routing algorithm of the Brookhaven system. This is illustrated in Fig. 2. The basic scheme is as follows. All addresses below each SI are assigned adjacent. There can be gaps in address assignments. Indeed, to allow for expansion there should be large unassigned blocks in each segment. This address assignment scheme allows the SI to be set up with only two words. The set could be the lowest address, say, and the highest address + 1, or the base address and the width (or total number of addresses). The routing algorithm is then simply as follows:

IF THE REQUEST ORIGINATES ABOVE . . ⊃I AND IS WITHIN THE RANGE OF
ADDRESSES OF THE SI THE CONNECTION IS MADE. IF NOT, THE SI IS MUTE

IF THE REQUEST ORIGINATES BELOW AN SI AND THE ADDRESS IS NOT IN THE
RANGE OF THAT SI THE CONNECTION IS MADE. IF NOT, THE SI IS MUTE

If a connection is called for, the SI requests the segment beyond at its own priority.
This scheme automatically establishes communication between all modules. If additional
paths are required they may be established by means of address mapping SI's which change
addresses of information passing through them.

Experiment 735 at the AGS at Brookhaven has been operating for about a year now. The
experiment searches for CP or T violation in $K^+ \to \pi^0 + \mu^+ + \nu$ decays. An out-of-decay
plane polarization component of the μ meson would indicate the searched for symmetry law
violation. A schematic of the apparatus is given in Fig. 3. The apparatus has a 32-fold
symmetry. Mu-mesons from the decay region traverse several counters which define the
angular region of the decay and are then focused on a polarimeter. The polarimeter consists
of a set of 32 Al wedges in which the μ's come to rest. Counters at the entrance announce
the arrival of the μ meson and counters elsewhere reject events in which the μ leaves. A
fraction of the positrons from the μ decay are detected by counters sandwiched between the
wedges. A weak magnetic field precesses the mesons after they come to rest. All the
detector elements are scintillation counters.

The FASTBUS system contains the following modules:

    7 - 32 channel latches
    1 - 32 channel μ clock
    1 - processor
    1 - 4K × 16 bit (or 2K × 32 bit) 30 nanosec memory
    1 - PDP11 Unibus interface
    2 - 16 channel scaler modules
    1 - Pre-Det
    1 - look-up module (box finder)

Triggers are generated by an off-bus ECL based device. The trigger records all the
photomultiplier hits in the latches and starts the 32 μ clocks. A decay positron hit in a
polarimeter counter pair stops its corresponding clock. The processor reads the latches
and discards all patently impossible events. It converts the hit patterns to bit addresses.
These addresses are stored in the memory. The processor then consults the "Box Finder" to
determine the relevant μ clocks to read. The event can be aborted at any time the processor
decides that event is impossible. The memory is operated in a FIFO (first in, first out)
mode with the processor feeding events in and the PDP11, through the interface, reading
them out. A typical event is only 10 words long and we store fewer than 100 events per
pulse so the memory is much more than sufficient.

The PDP11 is interrupted at the beginning of an AGS pulse, at the end of the pulse and again somewhat later when intensity information is available. The Pre-Det (predetermined time) module on FASTBUS generates these interrupts. The scalers are read and cleared by the PDP11 through the interface. The interface generates broadcasts to enable and disable modules during the AGS cycle on command from the PDP11.

This system has been operating for about a year now. During the initial debugging period we developed several tools which include a semi-static off-line device, a microprocessor connection to the bus and an ODT-like debugging routine for use on the PDP11. A microprocessor module and its software is being prepared for future on-bus debugging. After the initial debugging the system has been quite stable. We believe that this is due to the excellent thermal environment provided by the cooling system.

Our next experiment, 749, will be implemented with an extended FASTBUS system. The extensions will include several segments, some of them cable segments. The detector will include lead-glass Cerenkov counters and proportional wire chambers, as well as scintillation counters. We plan a new interface in which the crate is connected to the computer with a cable segment. Cable segments will be used will be used to read the proportional wire chambers as well. At least one new processor, this one with an ALU, will be developed. We expect to be ready by the end of this year.

At Brookhaven we have been building a very powerful FASTBUS system which is still relatively simple. One should examine each element of complexity in systems such as these and carefully weigh the gain in utility against the cost in money, difficulty in use, difficulty in debugging, difficulty in maintenance and difficulty in understanding. Without the ability to understand, in depth, what electronics and computers are doing to data, we may produce bad physics.
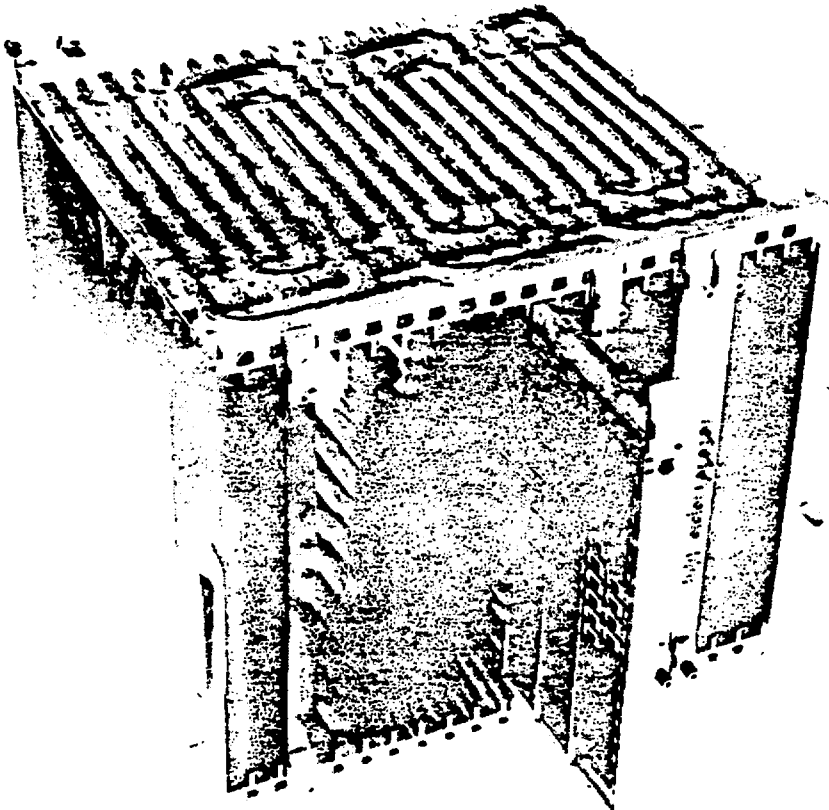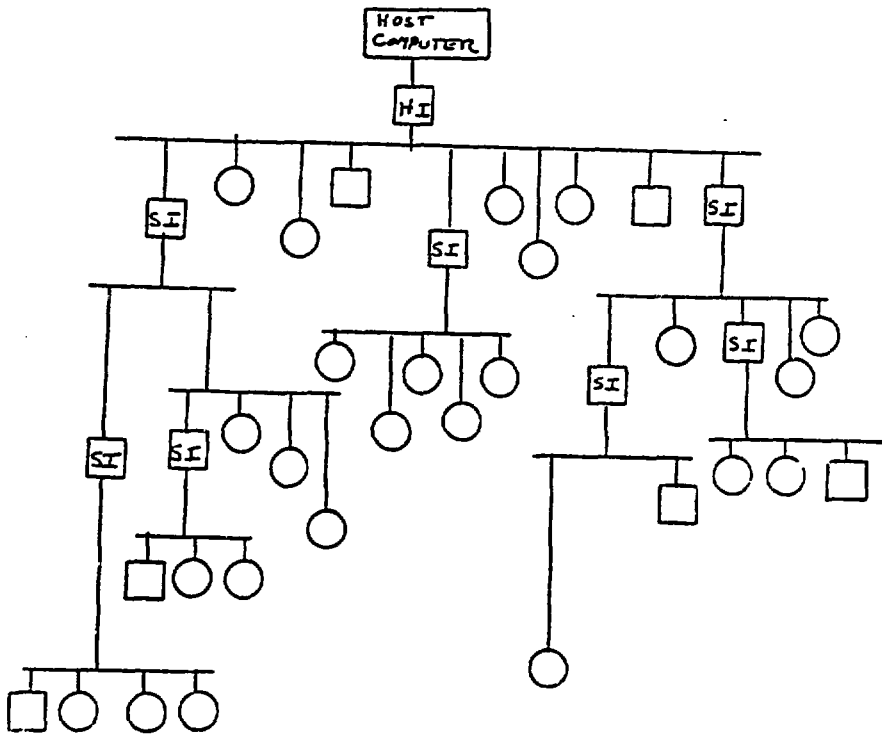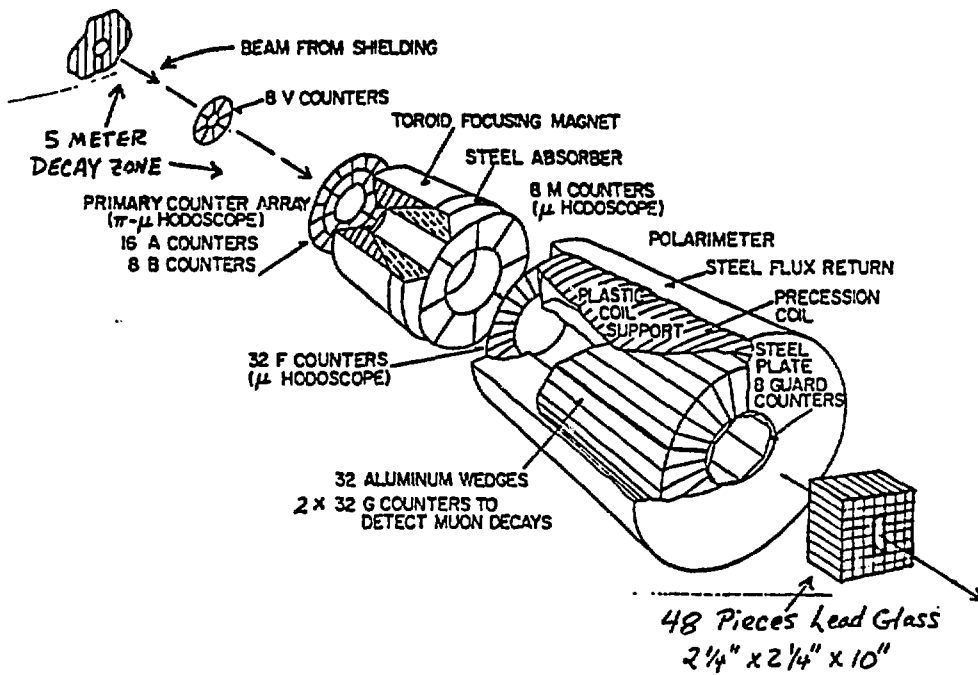
Fig. I

Fig. 2

Fig. 3