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A ONE NANOSECOND RESOLUTION TIME-TO-DIGITAL CONVERTER

C. Legrêle and J.C. Lugol
DPhPE/MF, CEN Saclay, 91191 Gif-sur-Yvette Cedex, France

A one-nanosecond resolution time-to-digital converter for the SPES I detection system near Saturne II has been built. Full ranges are 1 µs or 8 µs. A 125 MHz gated oscillator triggered by the start gives after a four-phase demultiplier a set of 16 signals of 32 ns period delayed by 1 ns. The stop memorizes 32 different configurations for the fine count in Gray code. The differential non linearity is ± 0.25 ns.

INTRODUCTION

For the SPES I spectrometer detection near Saturne II, we have built a one-nanosecond resolution time-to-digital converter. This module is in CAMAC standard, while the inputs are in fast NIM electronic logic. The full range is selectable : either 1.024 µs or 8.192 µs. The 8.192 µs range is used for the measurement of drift time in 50 cm long drift chambers (Horizontal coordinate) and the 1.024 µs range is used for the measurement of time difference in the cathode delay line read out (Vertical coordinate).[1] The coding is performed during the time between start signal and the stop signal.

CONVERTER PRINCIPLE

The start signal triggers a 125 MHz gated oscillator. This signal drives a four-phase demultiplier device that consists of two circuits of two-stage ring counter. One is driven by the direct signal, the other is driven by the out-of-phase signal. We obtain four 32 ns period symmetrical signals delayed by 4 ns each from the other. One of these 32 ns period signals is counted in a binary counter as a coarse count during the time difference between start and stop signals. Each signal from the four-phase demultiplier is delayed successively by 1, 2 and 3 ns. Thus we have 16 signals of 32 ns period delayed by one nanosecond. These signals generate in Gray code 32 different configurations which correspond with "0" to "31" values of the fine count. The stop signal memorizes this configuration in a D register. When the time difference changes for 1 ns, there is only one bit that changes, the other remaining stable. A decoder made with Exclusive-OR gates and priority encoders gives bits for the fine count. The Fig. 1 gives a block diagram of the converter. This principle is quite close to the principle described in Reference .

CIRCUITS DESCRIPTION

I. Gated oscillator and demultiplier

The start and the stop signals are translated to ECL level by 10190 translators. The gated oscillator is built with a MC 1660 gate. A simplified schematic of this oscillator is given on the Fig. 2. The delay cable and the propagation delay of the gate assure the frequency to be 125 MHz. The two demultiplier stages are ring counter made with 11C70 D flip flop. The timing of the signals H_A, H_B, H_C and H_D at the outputs of the device are shown on the top of the Fig. 3.

II. Configuration decoder

After delaying each signal by 1, 2 and 3 ns, the 16 resulting signals (ϕ_1 to ϕ_{16}) are fed as data to a MC 10131 D flip flop register. The clock of the register is the stop signal. ϕ_1 to ϕ_{16} which are delayed by 1 ns to the other, are memorized to give 32 different configurations. One configuration differs to the next by only one bit. This is a Gray code in a "thermometer scale". These 32 configurations must be decoded in 5 binary bits giving the fine code. This part of the circuit, after the memorization, is built in TTL logic in order to be read by CAMAC. The decoder consists of Exclusive-OR gates and of two priority encoder circuits shown on Fig. 4. The logic equation is the following :

$$B_i \oplus B_{i+16} = S_i \qquad i = 1 \text{ to } 15 .$$

S_1 to S_{15} are applied to the inputs of the cascaded priority encoders.

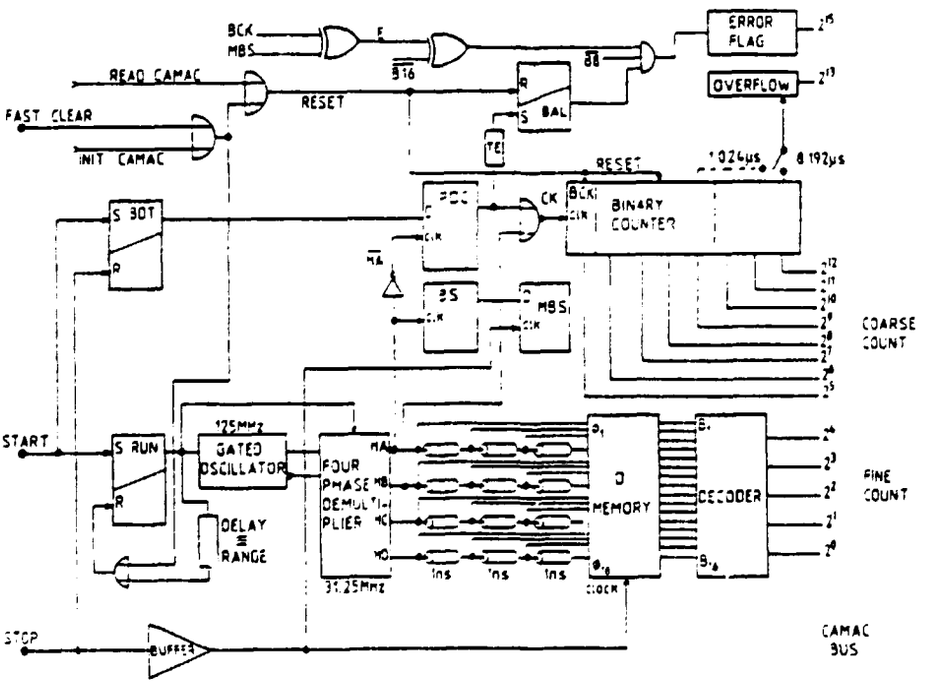

Fig. 1 - Block diagram of the time-to-digital converter.

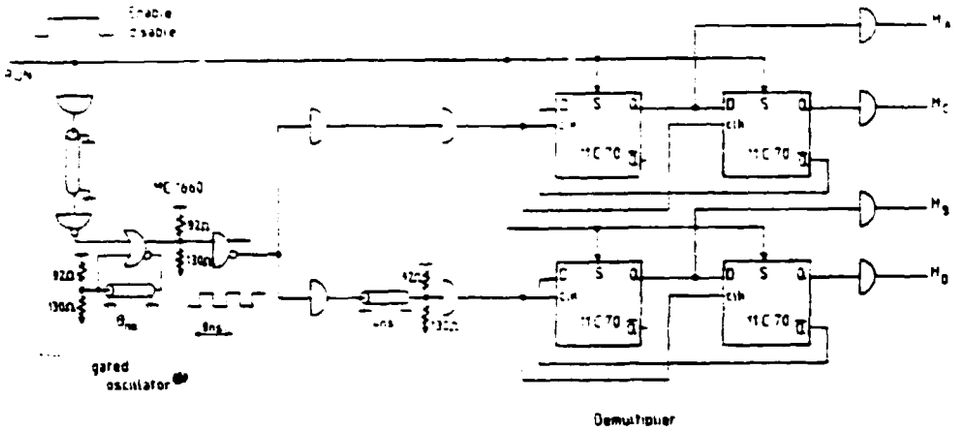

Fig. 2 - Simplified schematic of the gated oscillator and of the demultiplier.

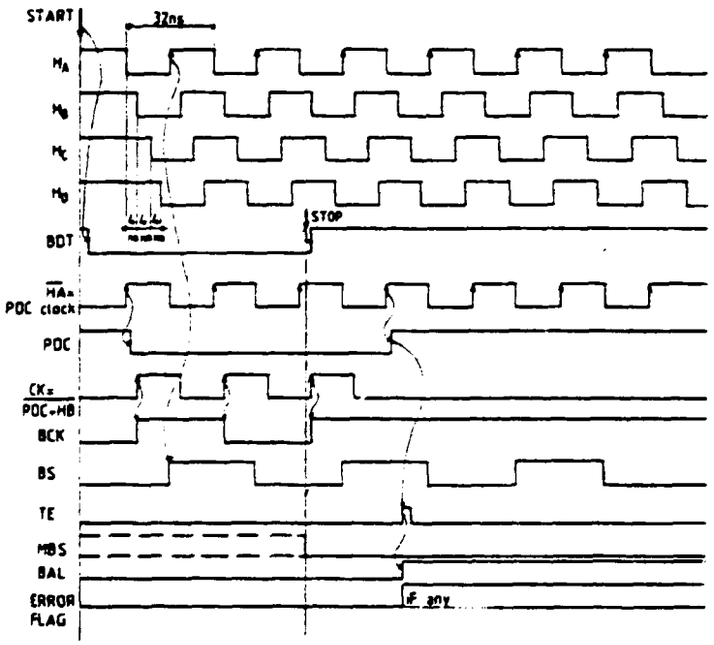

Fig. 3 - Timing of the converter.

III. Coarse count

The signal H_B in coincidence with the PDC register giver the signal CK which is counted in a binary counter as the coarse count. PDC register is a synchronization of the time difference between start and stop signals, related to the phase of H_A signal. An overflow flag is provided to the CAMAC bus.

ERROR CORRECTION SYSTEM

We have built a circuit to detect error caused by the arrival of the stop signal just when the fine count is changing from "31" to "0". In this case, the coarse count may have an error of ± 32 ns. To have the simplest circuit, we do not build a self correction system. We just put an error flag read with the numerical value by the CAMAC. We compare the first bit BCK of the coarse count to the MBS signal which is the memorized state of BS just at the time of the stop signal. This additional bit BS has twice the period of H_A. (See on Fig. 3). If there is no error, BCK and MBS must keep a constant relationship between them. So the value of E given by the following equation :

$$BCK \oplus MBS = E,$$

must be equal to 1 for the configurations "0" to "15", and must be equal to 0 for the configurations "16" to "31". Error flag given by the following equation :

$$\text{ERROR FLAG} = (E \oplus \overline{B_{16}}).\overline{B_5}.BAL,$$

is generated only when $\overline{B_5} = 1$ (that means configurations "24" to "31" and "0" to "7"), and during BAL when the conversion is completed after the trailing edge of PDC. BAL is reset after the reading sequence by CAMAC. Because of that error occurs just at the time of the changing of the fine code from "31" to "0", it occurs during, may be 0.3 ns for the whole period of 32 ns. For a given spectrum, the number of false codings is not very important ; i.e. few %. It is not a waste of time of treating this error by software in the data acquisition program. When an error occurs, we have to add or subtract 32 ns to the converted number : we add 32 ns when the fine count is "0" and we subtract 32 ns when the fine count is "31". Thus, we avoid the use in the module of adders and subtracters like in Reference 2.

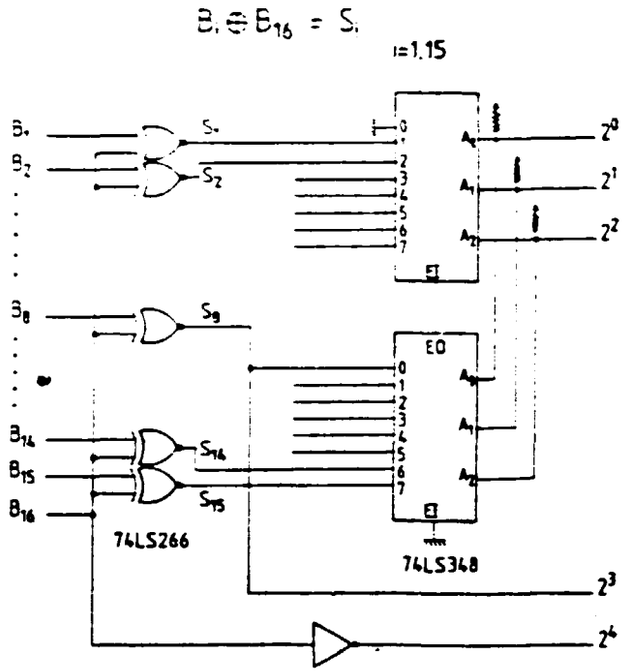

Fig. 4 - Schematic of configuration decoder.

DIFFERENTIAL NON LINEARITY

The D flip flop used in the configuration memory have dispersed Set up times and Hold times. Also, the width in time of each channel is not a constant. In our case, with a not so hard sorting of these D flip flop, the differential non-linearity is about ± 25 %. The Fig. 5 gives the spectrum obtained with random time differences. Each channel on the X-axis represents the width of the resolution : 1 ns. On the Y-axis, there is the counting rate which has a mean value of about 17 000 per channel. The spectrum should be flat, because each channel must have the same probability to be fed. The pattern of differential non-linearity is, of course, periodic with 32 ns period. The channel width varies from 0.75 ns to 1.25 ns. A very severe D flip flop sorting would improve the differential non-linearity.

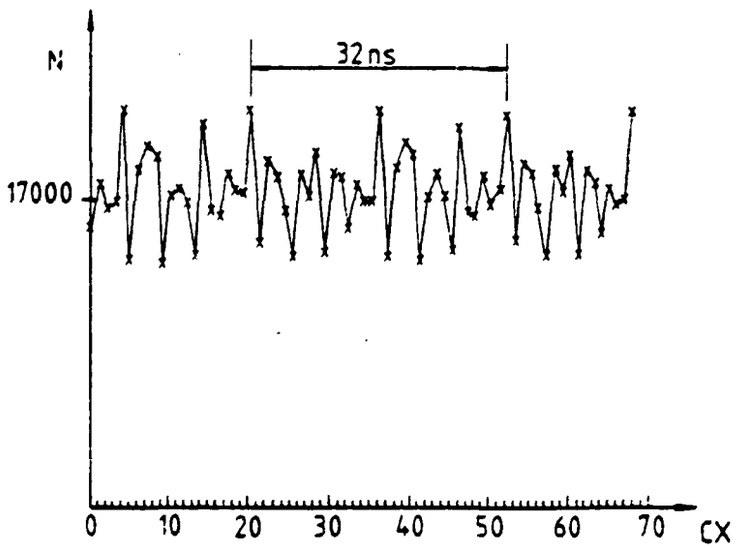

Fig. 5 - Spectrum of random time differences showing the differential non-linearity.

PRESENTATION

The Fig. 6 shows a view of the module. We can see on the front panel four test outputs for checking the H_A, H_B, H_C and H_D signals. A fast clear input is provided on the front panel to avoid a conversion before is completed, this input is in fast NIM standard.

REFERENCES

1. "SPES I detection system" ; Compte Rendu d'Activité du Département de Physique Nucléaire 1979 - 1980, Note CEA-N-2207, p. 233, section IV.1.
2. E. Festa and R. Sellem, "A multistop time-to-digital converter", Nucl. Instr. Meth. 188 (1981) 99.

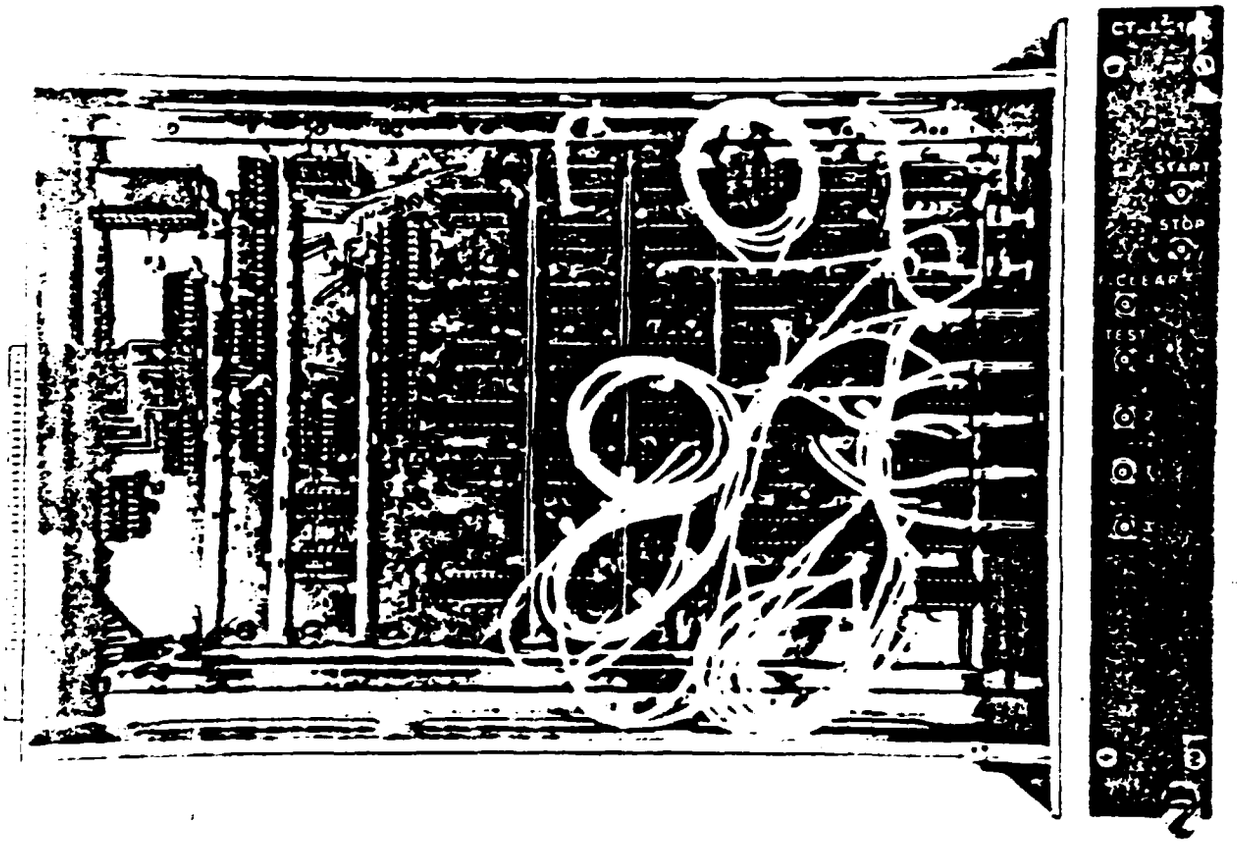

Fig. 6 - View of the module.