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A NEW PREAMPLIFIER FOR PARTICLE DETECTORS

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A NEW PREAMPLIFIER FOR PARTICLE DETECTORS

Abstract

A new peamplifier for particle detectors has been designed and built for the Fermilab VTPC by Fujitsu of Japan. The device, designated MB43458, is a semi-custom monolithic assembled in a small, low mass package. The purpose of this report is to document the preliminary tests which have been done thus far. Tests are continuing to expand upon the results presented herein.

I. Circuit Description

The Fujitsu MB43458 is a 4-channel preamplifier which comes in a small outline, 14 pin package. The basic circuit is a common base input amplifier similar to the well-known Radeka hybrid preamp. A schematic of one channel of the Fujitsu chip is shown on the next page in Fig. 1. Some input and output protection is provided by diodes and the output is back-terminated in an equivalent 50Ω . The base of each preamplifier is brought out to a pin. Only one 12 V power supply is needed to operate the device. Other data sheets for the MB43458 are given in Sect. XI.

II. Gain

A small printed circuit board was built which accommodated 6 amplifier chips and associated surface-mounted passive components. (See Fig. 2.) The circuit allows for easy testing of 24 different channels on 6 different chips. Tests were done to check the gain uniformity of the chips using the circuit

MB43458 回路図

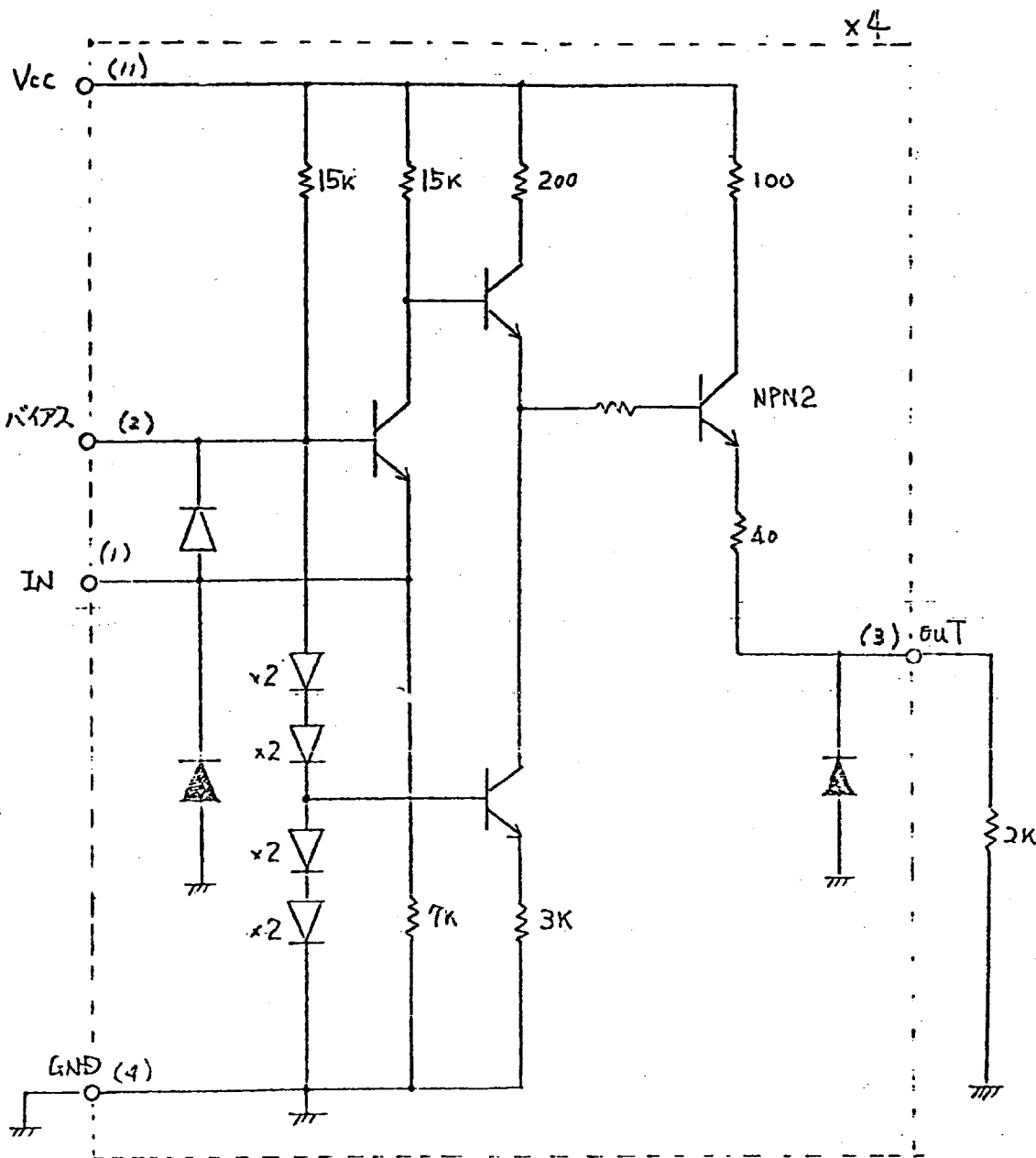


FIGURE 1 - ONE CHANNEL OF FUJITSU PREAMPLIFIER

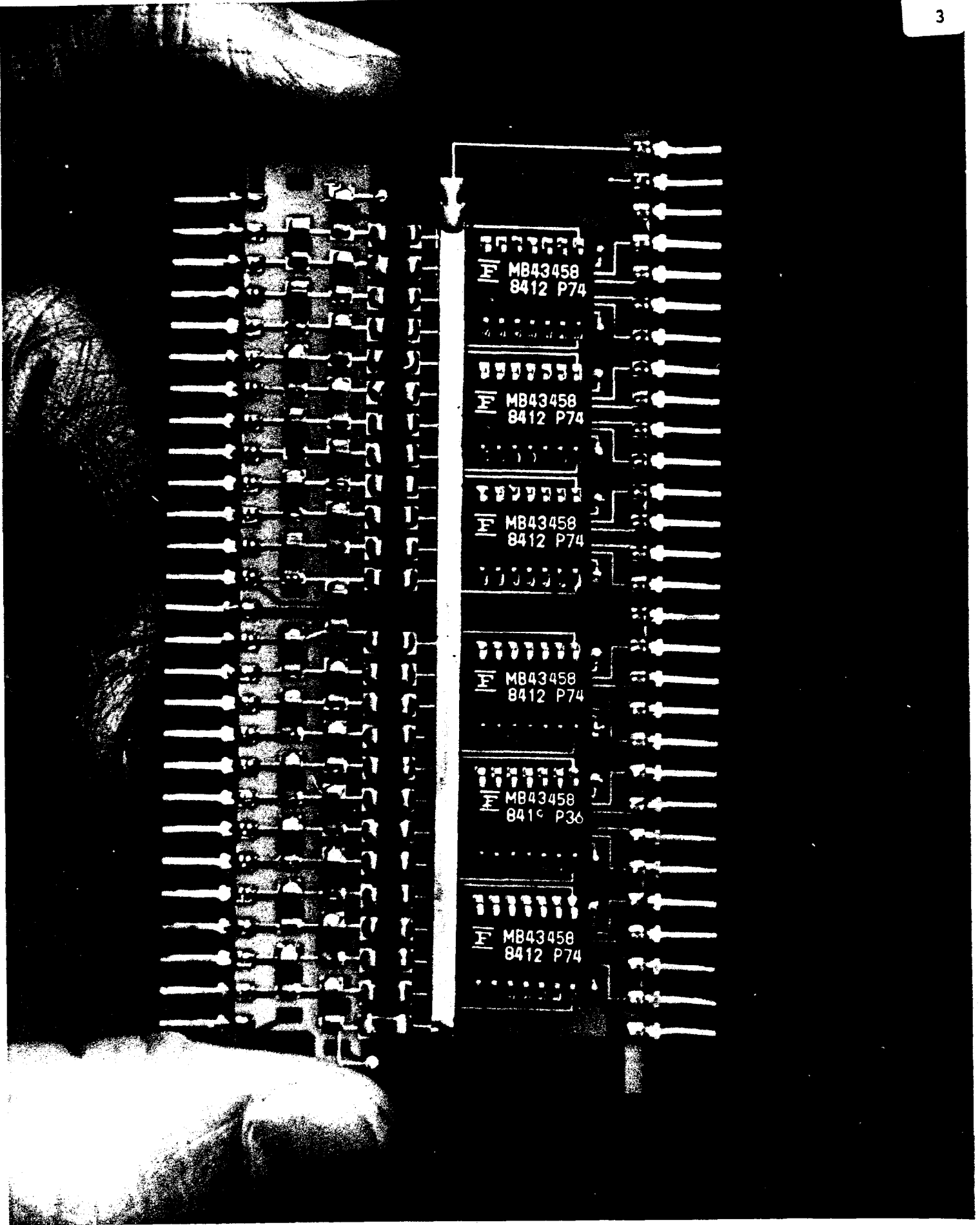


FIGURE 2 - 24 CHANNEL PREAMPLIFIER CARD

shown in Fig. 3. Results of the test showing gain variations are in Table 1. Before each measurement, the temperature of the chips was allowed to stabilize.

Table 1 - Gain Uniformity, $T_A = 23.5^\circ\text{C}$, $R_L = 560\Omega$

Chip No.	Injected Charge ΔQ	Peak Output Pulse			
		Ch 1	Ch 2	Ch 3	Ch 4
1	0.42 pc	96.0 mv	96.0	100.0	99.0
2	0.42 pc	98.5	98.0	100.5	100.5
3	0.42 pc	96.0	96.0	100.0	99.0
4	0.42 pc	97.5	95.5	99.0	99.0
5	0.42 pc	96.5	95.5	100.0	99.5
6	0.42 pc	96.0	96.0	99.0	99.0

As can be seen, gain variations for a given channel from chip to chip is quite low. There is a somewhat larger gain variation from channel-to-channel on a given chip (about 4%). However, the gain variations are consistent from chip-to-chip.

Gain variations with temperature were also seen. In an ambient of 23.5°C and the chip at the same temperature, the gain of each channel was found to be 7-8% higher than that shown in Table 1. The temperature of the chip is largely determined by the current in the output transistors. With about 10 ma in each output transistor ($R_L = 560 \Omega$), the surface temperature of the chip was found to be about 48°C . Measurements showed that the gain temperature coefficient was about $-0.2\%/^\circ\text{C}$.

The test circuit injected 0.42 pc into each channel via a 10 pf capacitor and a 100Ω series resistor. For a test signal of 0.42 pc, the absolute gain was found to be about 235 mV/pc.

III. Rise and Fall Time

The MB43458 response to a small charge input is relatively clean. There are no overshoots or kinks in the output. The circuit in Fig. 4 was used to look at the preamp response time. (While the circuits in Figs. 3 and 4 are slightly different, the test results would be essentially the same with either circuit.) Use of a small bypass capacitor on the beam input pin decreases signal rise time by 0.5 to 1 nsec.

Figure 5 compares the output of the Fujitsu to a Radeka hybrid preamp shown in Fig. 6 for the same charge injection circuit. (The Radeka was run at +6V, -10V to minimize output distortion.) As can be seen, the Radeka has a kink in the output that the Fujitsu does not have. Table 2 compares the response of the 2 amplifiers.

Table 2 Rise and Fall Times (10-90%)

Amplifier	Rise Time	Fall Time
Fujitsu MB43458	6 ns	30 ns
Radeka	4 ns	80 ns

The Radeka has a slightly faster rise time and the Fujitsu has a much faster fall time. A faster fall time allows for better double pulse resolution. Fast rise time may or may not be an advantage depending on the type of gas used. (See Sect. IX for more details.)

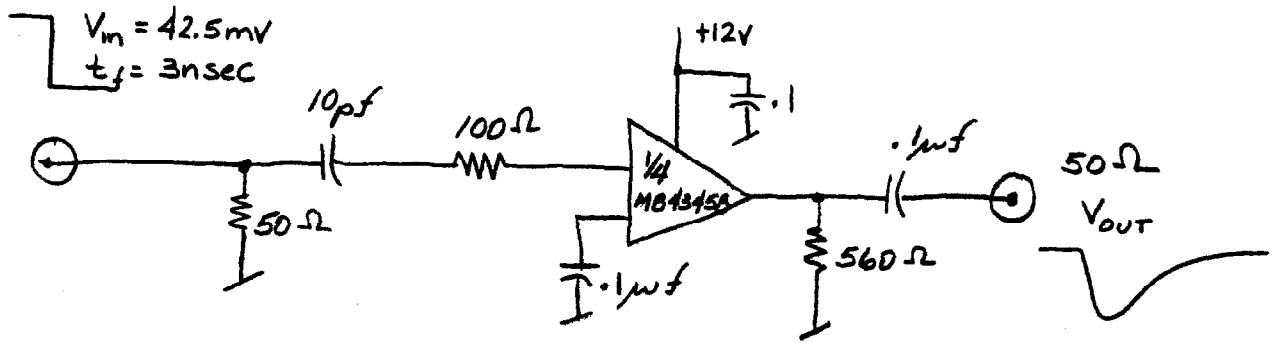


FIGURE 3 - GAIN TEST CIRCUIT

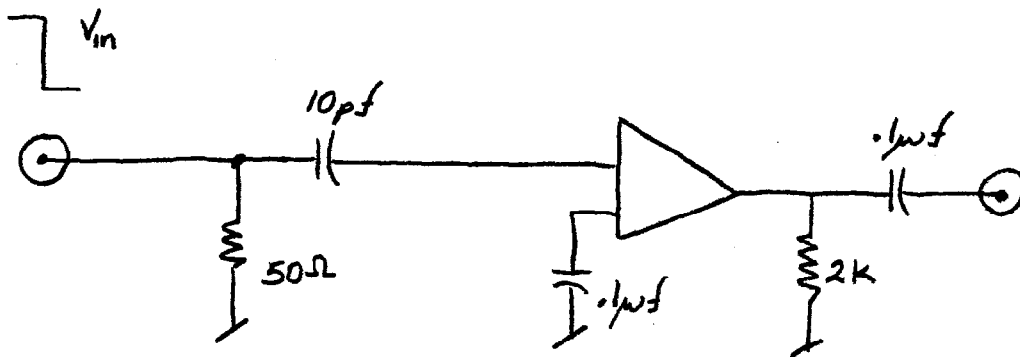
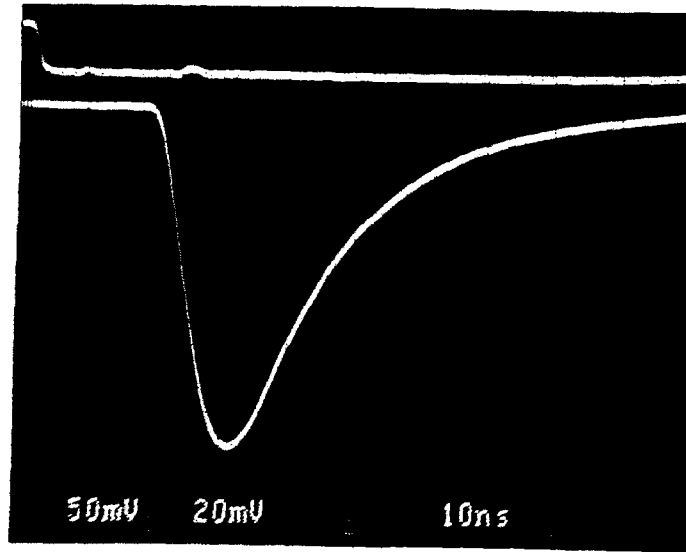


FIGURE 4 - RESPONSE TIME TEST CIRCUIT

FUJITSU MB4345B

V_{in} 50mv/div

V_{out} 20mv/div



RADEKA

V_{in} 50mv/div

V_{out} 20mv/div

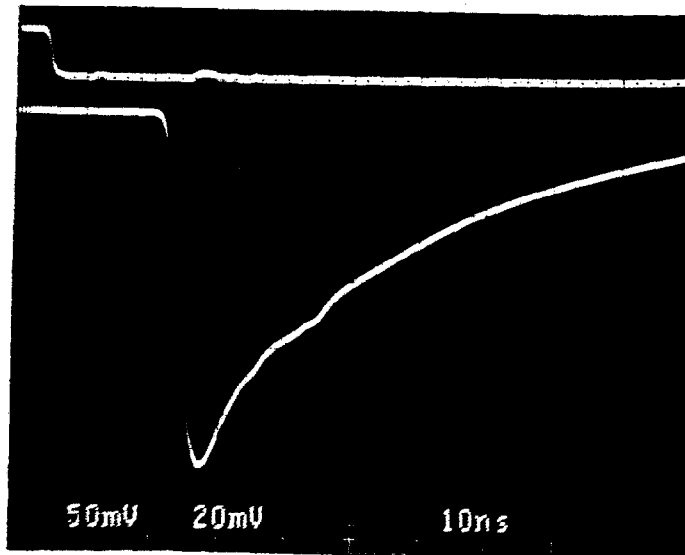
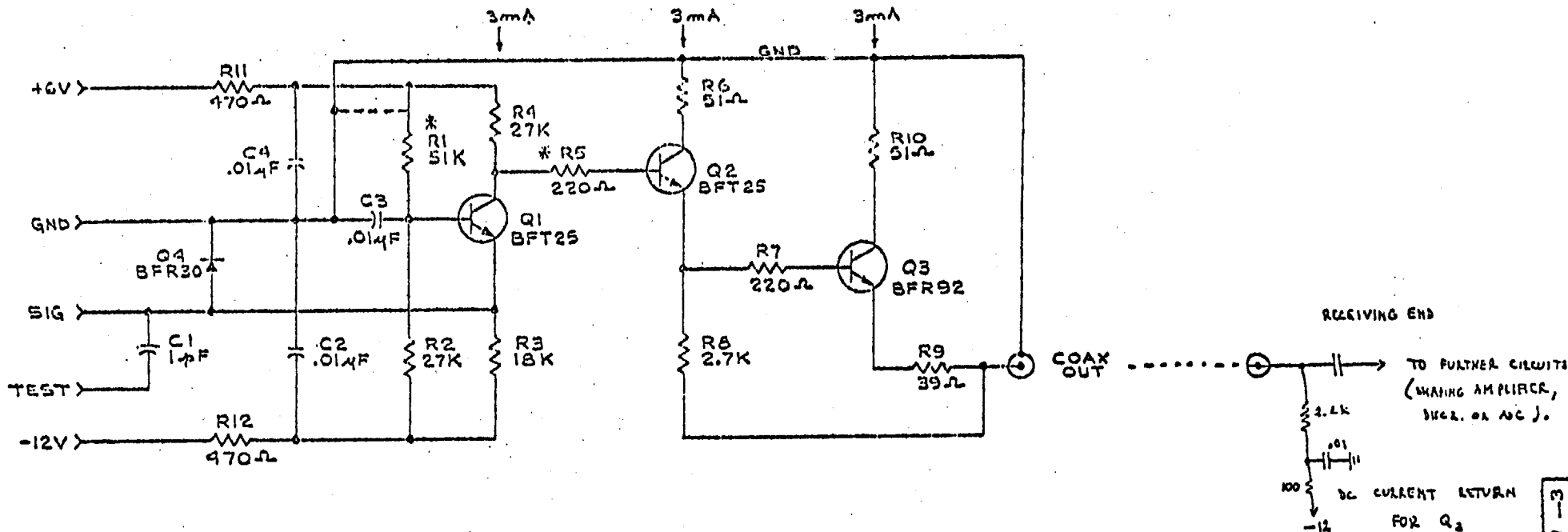
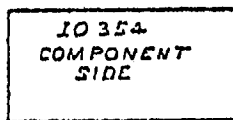


FIGURE 5 - AMPLIFIER RESPONSE TIME



*** CERAMIC VERSION**

R1 = 24K TO GND
 R5 = 15 REPLACED WITH CONDUCTOR
 C1 = 0.3 pF



M1 = BFR-30
 V1 = BFT-25
 P1 = BFR-92

(STANDARD DIP SOCKET)

For questions call V. Radeka,
 BNL, FTI - 666-1266

FIGURE 6 - RADEKA PREAMPLIFIER

DATE	6-15-82	NAME	HOME
BY	S. GRAVIER	REVISION	1
BROOKHAVEN NATIONAL LABORATORY ASSOCIATED UNIVERSITIES, INC. UPTON, N. Y. 11973			
COMMON BASE PREAMP. FOR 100 ANODE CHANNEL PC VERSION			
IO 354 - 1 - 3			

IO 354 - 1 - 3

IV. Dynamic Range and Linearity

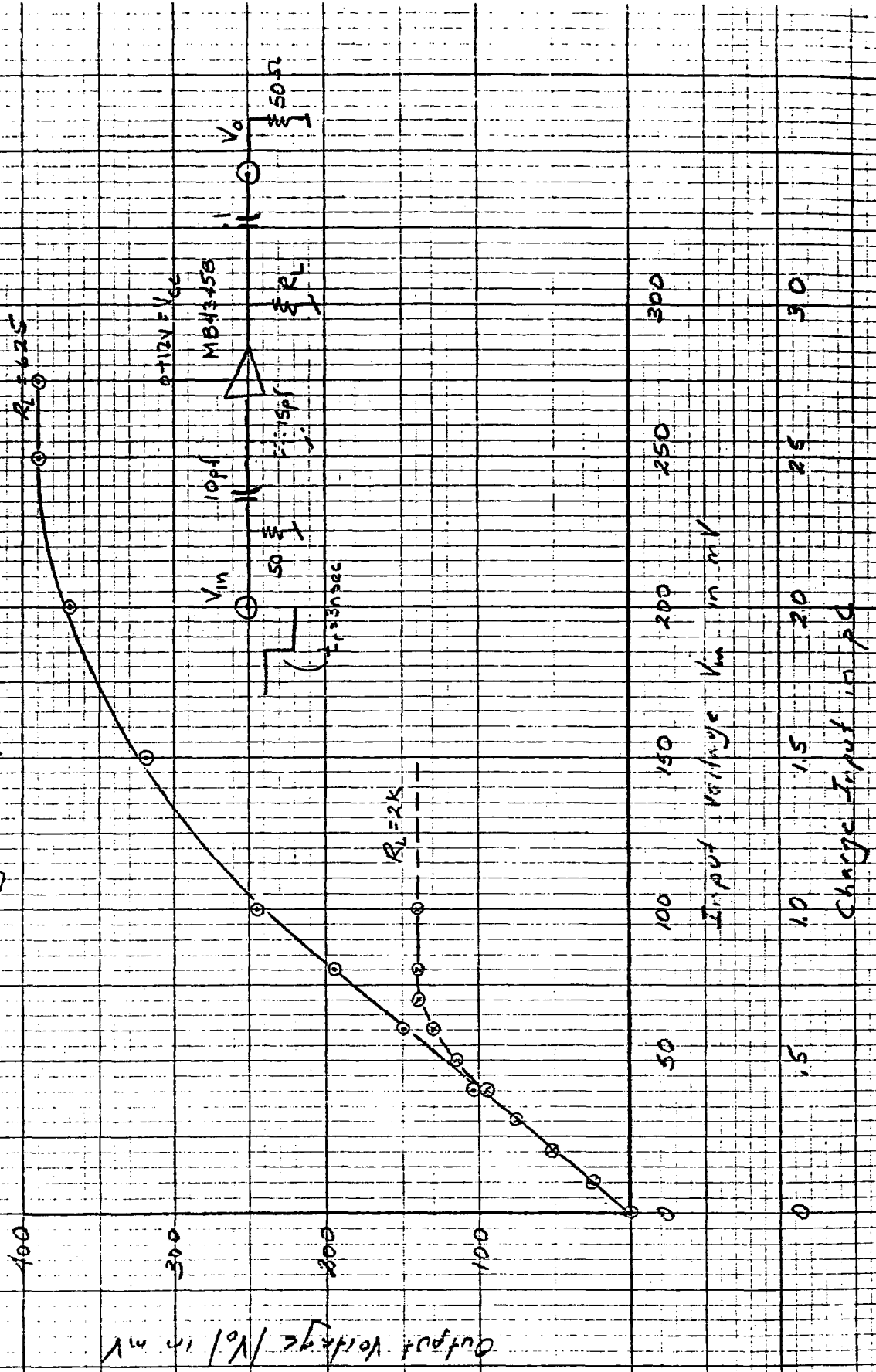
The Fujitsu is a non-inverting amplifier with an emitter follower output. For negative input pulses, the output transistor tends to cut-off. Larger output pulses can be accommodated by lowering the output resistor, R_L , and standing more current in the output transistor or by adding a separate PNP emitter follower stage. Lowering R_L of course increases considerably the dissipation in the device. For $R_L = 2K$ each channel typically draws 4 ma with 2.9 ma in the output transistor. Decreasing the load resistor from 2K to 625 Ω increases device dissipation from about 30 mW/channel to about 70 mW/channel. Figure 7 shows the MB 43458 output characteristic for negative inputs. For positive input pulses, the output is linear to about +400 mV and saturates at about +1 V (with $R_L = 625 \Omega$).

An emitter follower circuit was built to extend the output range for negative inputs while minimizing device dissipation. Although the circuit performed well, the parts count/amplifier channel was significantly increased.

V. Crosstalk

In order to measure channel to channel crosstalk accurately, the MB 43458 should be mounted on a p.c. board with appropriate bypassing as close to the chip as possible. For minimum crosstalk, it was found that each chip should have a 0.1 μ fd bypass capacitor directly across the +12V and ground pins. In the tests described here, chip capacitors of X7R material were surface mounted on the p.c. board. Crosstalk levels were found to be sensitive to the p.c. board layout. To minimize p.c. board effects, crosstalk measurements were made with the input and bias pins of non-driven channels

Figure 7 - MB43458 Dynamic Range for Negative Inputs



4-11-84
R.V.V.

lifted slightly from the board. Connection of the bias pins to the board for our layout had little effect on the crosstalk. Connection of other input pins to the board introduced some capacitively coupled signal into the other channels output. Besides changing the magnitude and shape of the crosstalk, in some cases the capacitive crosstalk was large enough to change the sign of the crosstalk observed. Care must be exercised in designing the p.c. board for the MB4345B.

Figure 8 shows the test circuit used to measured crosstalk and Fig! 9 shows a typical crosstalk signal. In general it was found that crosstalk was of opposite sign, and varied in magnitude by as much as a factor of 2 from channel-to-channel. Crosstalk of the chip is typically less than 1%. Table III presents typical crosstalk measurements for an input signal that has a fall time of 1.5 ns and an associated output amplitude of 200 mV.

Table III MB4345B Crosstalk Measurements at $V_o = 200$ mV

Peak Output Signal			
<u>Ch 3</u>	<u>Ch 4</u>	<u>Ch 1</u>	<u>Ch 2</u>
-200.00 mV	+ 1.25 mV	+ 1.30 mV	+ 0.90 mV
+ 0.80	-200.00	+ 1.65	+ 1.5
+ 1.10	+ 1.80	-200.0	+ 1.50
+ 1.20	+ 1.50	+ 1.90	-200.0

The maximum crosstalk is seen to be about 0.95%. Small changes in signal fall time did not change the chip crosstalk. The p.c. board capacitive effects however were of course rise time dependent.

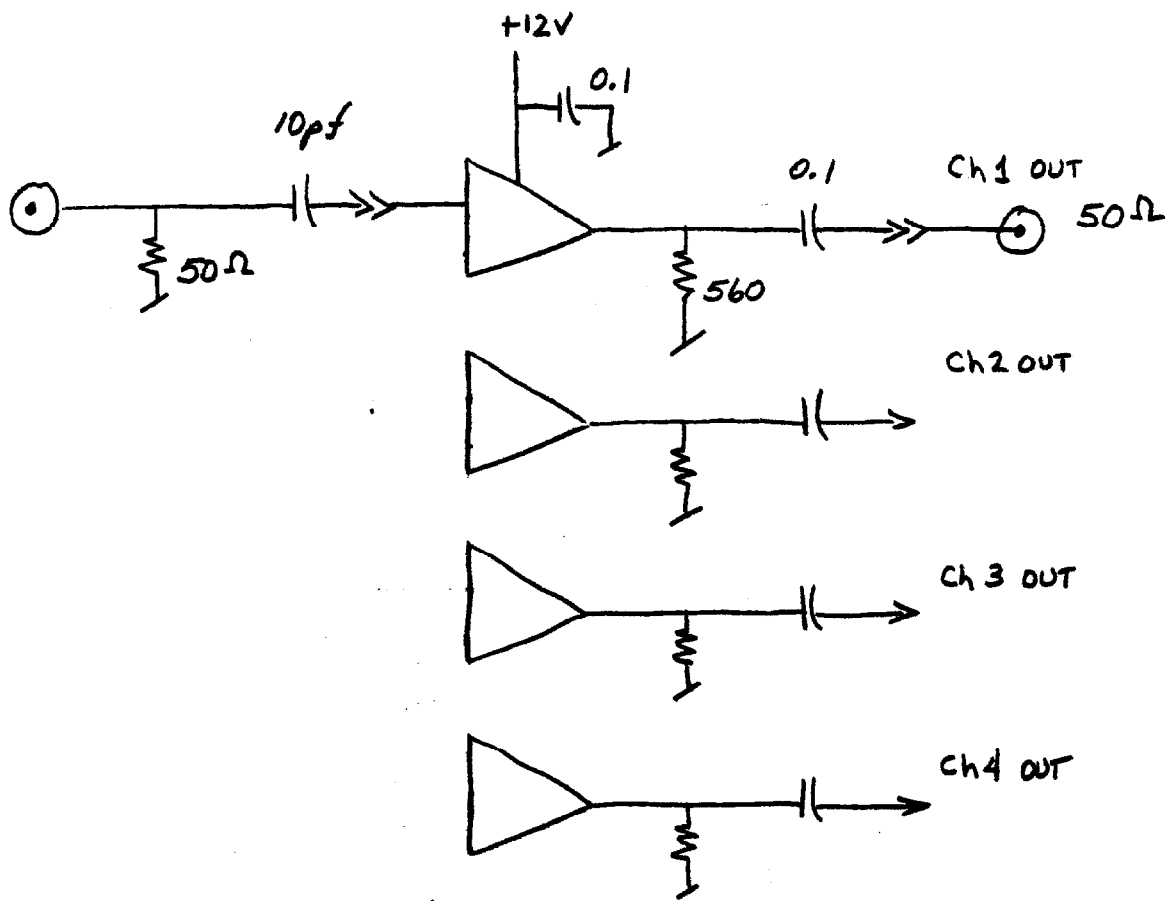


FIGURE 8 - CROSSTALK TEST CIRCUIT

CH3 OUTPUT

CH2 CROSSTALK

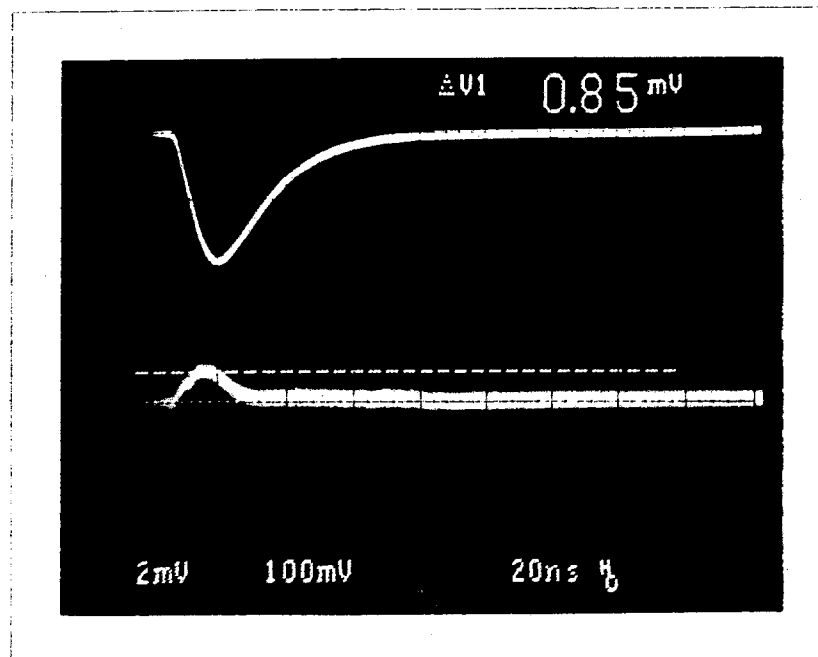


FIGURE 9 - TYPICAL CROSSTALK

VI. Noise Measurements

The MB 43458 noise characteristics were measured using a LeCroy QVT. For comparison, measurements were also made on a Radeka common-base hybrid preamp. All of the tests were completed with the circuit shown in Fig. 10.

Noise measurements were made for different gate widths on the QVT. The results are summarized in Table IV.

Table IV Noise Measurements with Input Capacitance of 25 pf

Gate Width	<u>Equivalent Input Noise</u>	
	MB 43458	Radeka
50 ns	3840 e RMS	3450 e RMS
100	4050	3400
200	4380	3800
400	5530	4000

For both devices, noise increases as the gate width increases. The signal pulse width from the Fujitsu is about 50 ns compared to 100 ns for the Radeka. Therefore, in additional tests a 50 ns gate was used for the Fujitsu and a 100 ns gate for the Radeka. An important consideration is how noise changes as a function of input capacitance. Measurements were made for different input capacitances by changing the shunt capacitor shown in Fig. 10. Results of these tests are shown in Table V.

Table V Noise Measurements vs. Input Capacitance

Device	Gate Width	<u>Equivalent Input Noise</u>		
		<u>Input Capacitance</u>		
		25 pf	47 pf	72 pf
MB 43458	50 ns	3840	5170	6750 e RMS
Radeka	100 ns	3400	3660	4500 e RMS

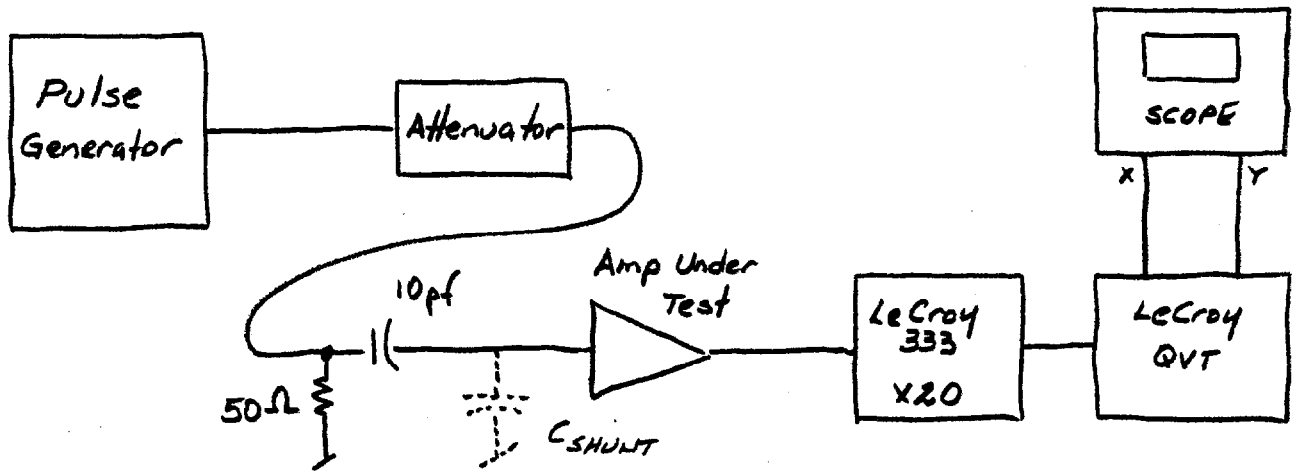


FIGURE 10 - NOISE TEST CIRCUIT

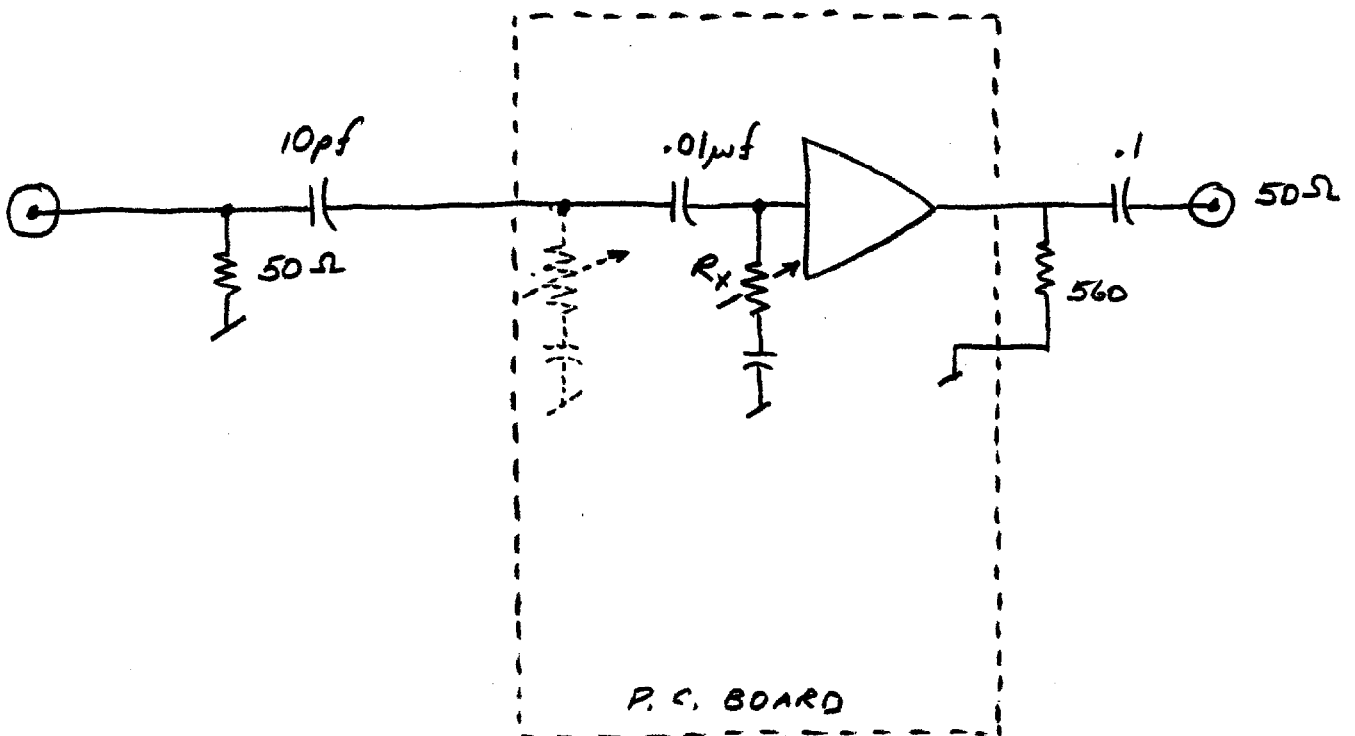


FIGURE 11 - INPUT IMPEDANCE TEST CIRCUIT

As is readily seen, input noise at low input capacitance is comparable for the Fujitsu and Radeka preamps. However, as capacitance increases, noise in the Fujitsu increases more rapidly than in the Radeka preamp.

VII. Input Impedance

A simple charge injection circuit was used to measure the dynamic input impedance of the Fujitsu MB 43458 (see Fig. 11). In order to get an accurate measurement, the amplifier was mounted on a small printed circuit board with good bypassing and ground. The pot, R_x , in Fig. 11 was adjusted until the output signal was 1/2 of the signal with $R_x = \infty$. When the output is at half value, R_x is equal to the input impedance. The pot was removed and measured to determine its value. The value obtained for input impedance varied slightly depending on where it was measured. At the input pin to the chip, Z_{in} was found to be about 96Ω . At the input to the p.c. board, Z_{in} was found to be about 106Ω . The difference is attributed to circuit board impedance. If good ground connections are not made to this board, higher values for input impedance will be found.

VIII. Input Protection

Whenever a preamp is run on a wire chamber, there is always a chance that a high voltage arc-over will occur and damage the amplifier input as shown in Fig. 12. The amount of damage is proportional to arc voltage and the size of the capacitor being discharged. The MB 45453 has input diodes as seen in Fig. 1 to help protect the device. Additional components, however, are

required to provide adequate protection for high voltage arc-overs. Those additional components may either be series resistors to limit the discharge current, parallel bypass diodes to shunt the discharge current, or a combination of both. Tests were run simulating arc-overs and different types of protection was checked. The chip buster circuit shown in Fig. 13 was used to simulate an arc-over. The capacitor C_x represents a capacitor storing energy which is to be discharged by an arc. A series of discharges is initiated by bringing contacts A and B close together. Resistor, R_s , and capacitor, C_s , are part of a relaxation oscillator which continually recharges C_x . For a conservative protection circuit, values of C_x two or more times larger than expected in practice were used in the tests.

Tests were done with and without bypass diodes and with many different combinations of voltage, and values for C_x and R_x . The simplest type of added protection is a series resistor to limit the discharge current. With $C_x = 500$ pf and $R_s = 100\Omega$, the preamp input was blown on the first discharge at +3 kV. With C_x reduced to 333 pf and R_s still 100 Ω , the preamp withstood 20 discharges at +3 kV. Thus under some operating conditions, a series resistor of 100 Ω can provide adequate input protection. Under some conditions, however, a series resistor as large as 100 Ω is undesirable.

Other tests were done with shunt diodes (type BAV99 in a SOT-23 package), but without a series resistor ($R_s = 0$). These tests showed that at +3 kV and a capacitance $C_x = 1000$ pf, the MB 43458 survived for 1/2 sec of continuous discharges and at 2.5 kV, survived for more than 10 sec. It is clear that the diodes by themselves provide more protection than a 100 Ω resistor. (Note, when shunt diodes are used, a series capacitor must be used to avoid upsetting the DC bias at the chip input.)

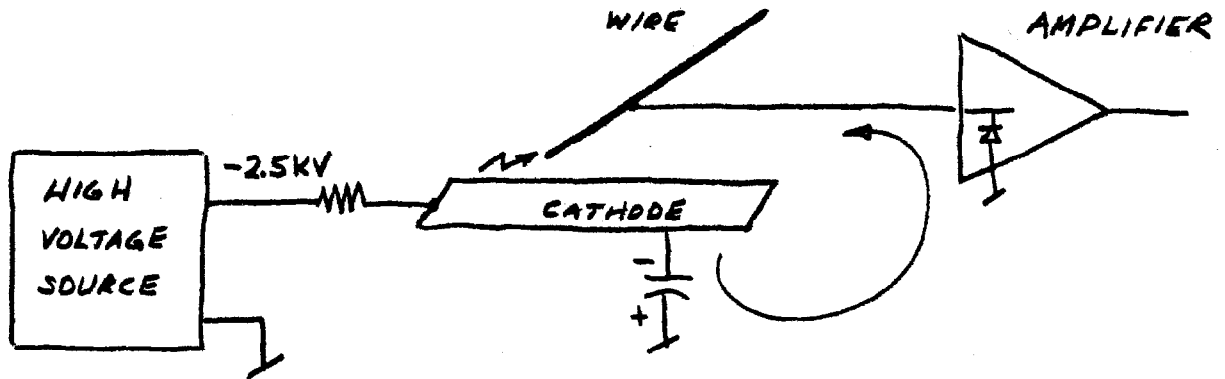


FIGURE 12 - WIRE ARC-OVER IN WIRE CHAMBER

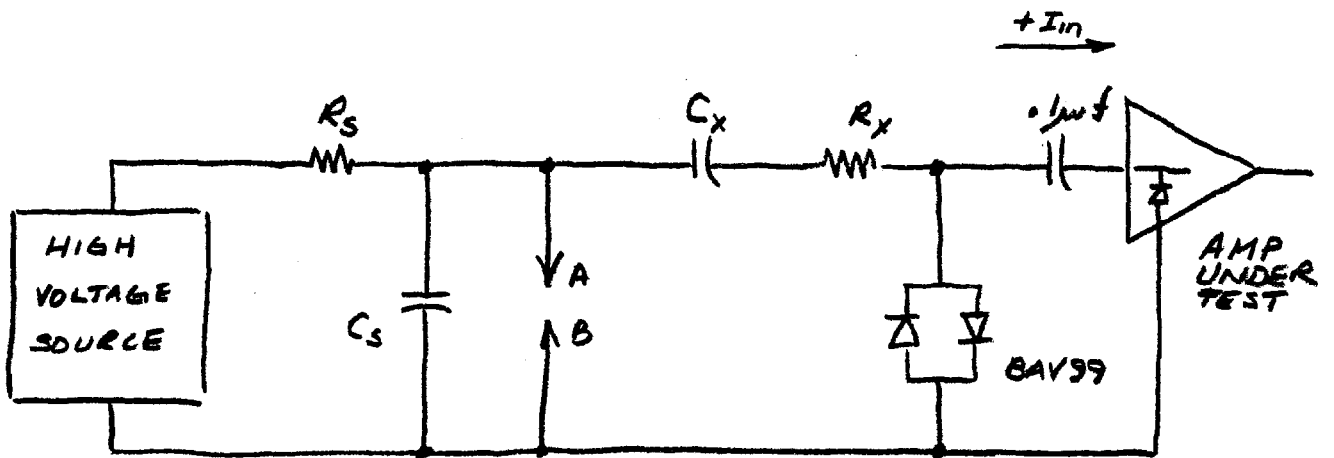


FIGURE 13 - CHIP BUSTER CIRCUIT

When the polarity of the high voltage supply was made negative to simulate positive input currents during a discharge, shunt diodes alone did not provide as much protection as for negative input currents. At a discharge voltage of -3 kV and C_x equal to only 333 pf, the input was blown after a couple of arcs. By adding a small series resistor, $R_s = 10\Omega$, in front of the diodes, protection was increased so that at $C_x = 1000$ pf and $V = -3$ kV, the preamp withstood 5 seconds of continuous discharges before failure. Shunt diodes along with a small series resistor ($R_s = 10\Omega$) form a reasonably conservative input protection circuit.

During all of these tests, it was found that when one channel of the 4 channel device was blown, the other channels were unaffected in gain and noise. After any given channel had withstood many discharges but not failed, its gain and noise characteristic was also unchanged.

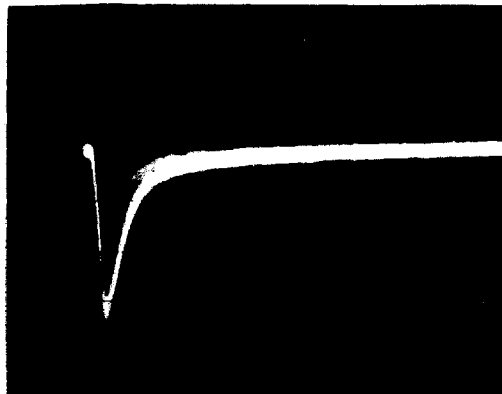
IX. Performance with Test Chamber

A small test chamber was set up with an FE55 source to see how the MB43458 compares with a Radeka hybrid preamp under actual operating conditions. Figure 14 shows a series of amplifier output waveforms for 2 different setups. The Fujitsu was run at +12 V with a load resistor of 625 and the Radeka was run at +6, -10 V with $R_L = 2.2$ K. Figures 14a and b show the two amplifiers run with HRS gas and 1600 V on the chamber. As can be seen, the signal rise time, which is limited by the gas, is the same for both amplifiers. The peak amplitude of the Radeka signal is large, but the fall time of the Fujitsu is considerably faster.

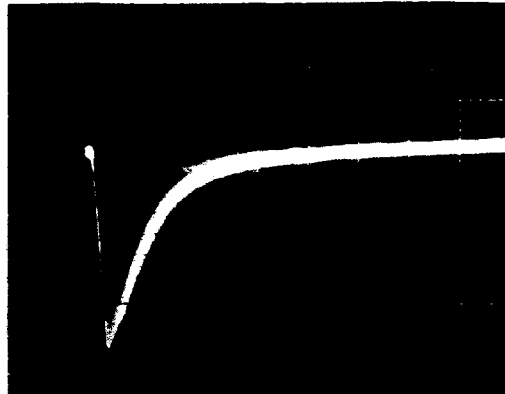
FUJITSU MB4345B

RADEKA

a)

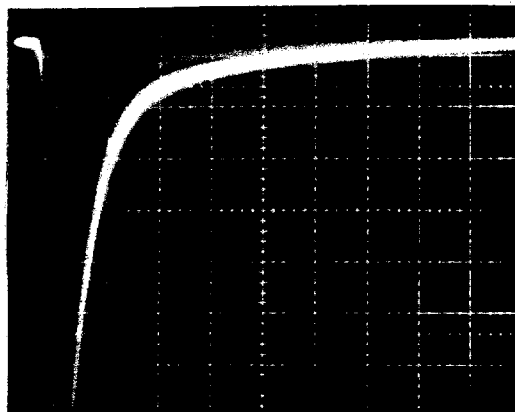


b)

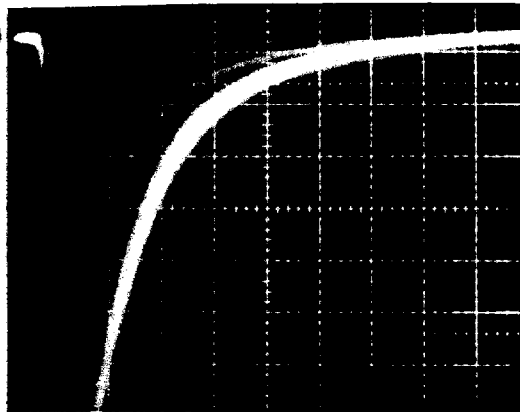


5mv/div
100ns/div

c)

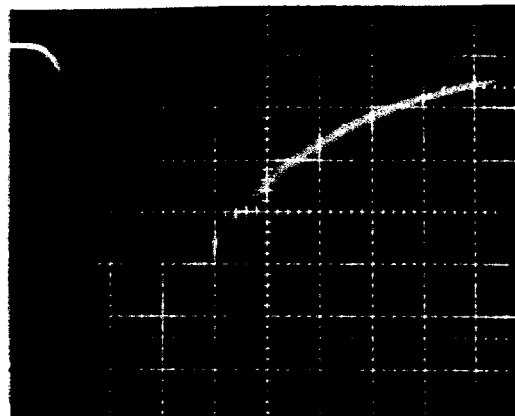


d)

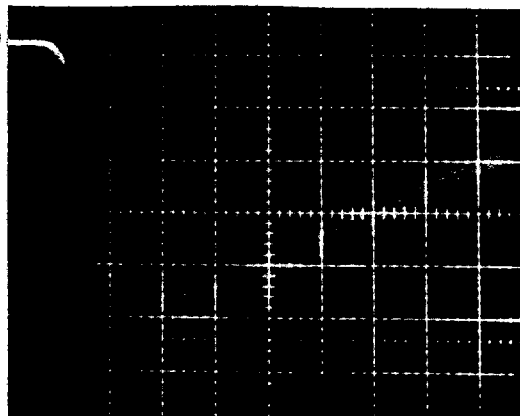


5mv/div
50ns/div

e)



f)



10mv/div
10ns/div

FIGURE 14 - TEST CHAMBER WAVEFORMS

Figures 14c, d, e f show operation with a Fast Gas (50% Argon 50% ethane) and 2000 V on the chamber. In this case, signal amplitudes and rise times are essentially the same for both devices. The fall time of course is still faster with the Fujitsu. Thus double pulse resolution is inherently better with the Fujitsu preamp. Alternately, if the signal is to be integrated for charge division, a larger signal would be obtained from the Radeka. A qualitative look at the widths of the signal traces shows that the noise obtained with each device is comparable when operated on the test chamber.

X. Status

Work is continuing to evaluate the Fujitsu MB43458 chip. At the present time Fermilab's VTPC detector is planning to use the preamplifier on its wires. Plans call for about 3000 channels to be built with 24 channels per printed circuit card. Each card with appropriate input protection and crosstalk networks would measure approximately 1.5" x 3.0". New printed circuit layouts for the VTPC are currently under development.

MB43458 規格表

1984 MAR 29
S 59. 3.29
I 版

VTPC PREAMPLIFIER
(VTPC用プリアンプ)

MAXIMUM RATINGS

最大定格 (Ta = 25°C)

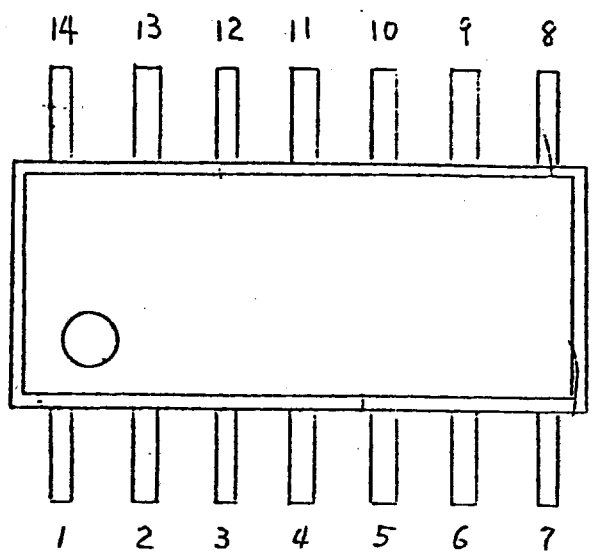
項目	記号	条件	定格値	単位
電源電圧	Vcc		16	V
端子電圧				V
許容損失	PD*	Ta ≤ 75°C	280	mW
動作温度	Top		-20 ~ +75	°C
保存温度	Tstg		-55 ~ +125	°C

* 5cm×5cmのセラミック基板実装時 CERAMIC HEATSINK

RECOMMENDED OPERATING CONDITIONS
推奨動作条件

項目	記号	MIN	TYP	MAX	単位
電源電圧	Vcc	11.5	12.0	12.5	V
動作温度	Top	-20	+25	+75	°C

端子配列図

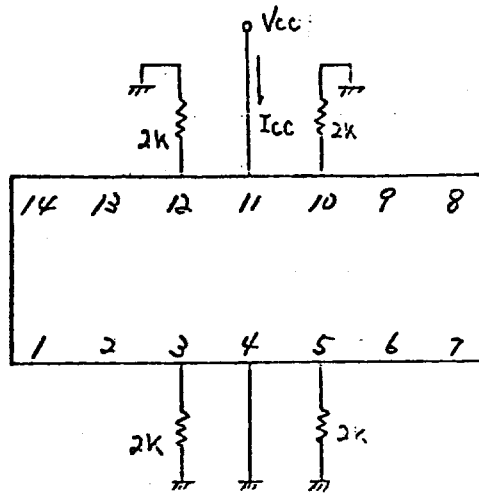


(TOP VIEW)

ピンNo	記号	機能
1	IN1	CH.1 入力端子 INPUT PIN
2	B1	バイアス端子 BIAS PIN
3	OUT1	出力端子 OUTPUT PIN
4	GND	GND 端子
5	OUT2	CH.2 出力端子
6	B2	バイアス端子
7	IN2	入力端子
8	IN3	CH.3 入力端子
9	B3	バイアス端子
10	OUT3	出力端子
11	Vcc	電源端子
12	OUT4	CH.4 出力端子
13	B4	バイアス端子
14	IN4	入力端子

TEST CIRCUITS
測定圖

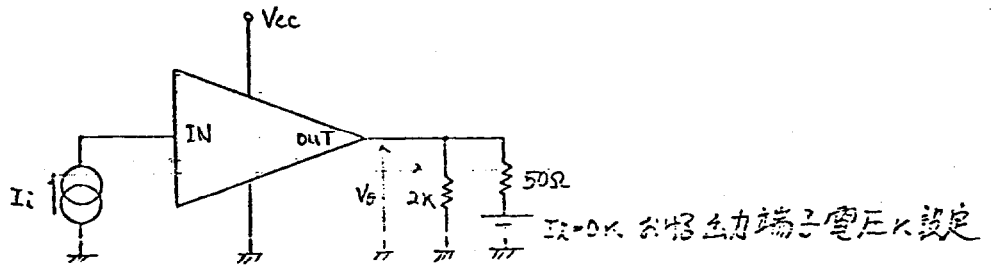
FIGURE 1
圖 1



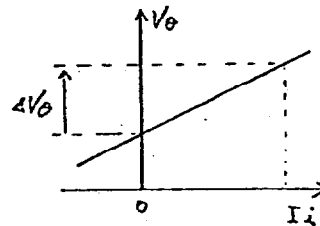
INPUT 入力端子 Pin 1, 7, 8, 14-
OUTPUT 出力端子 Pin 3, 5, 10, 12
BIAS 偏置端子 Pin 2, 6, 9, 13-

FIGURE 2

圖 2 各 Amp K 対以 下圖回路を構成する。



$I_i = 0K$ 各出力端子電圧K設定



$$1/0_{om} = \Delta V_o / I_i$$

FIGURE 3

圖 3 各 Amp K 対以 下圖回路を構成する

