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THE SLAC MARK II UPGRADE DRIFT CHAMBER FRONT END ELECTRONICS *

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Abstract

The SLAC Mark II detector is being improved by the addition of a new main drift chamber and associated electronics to prepare it for operation as the first detector at SLC. Presented here are the initial signal processing electronics, the preamplifiers, amplifiers and discriminators for the 5832 sense wires, which are located on the detector itself. The performance of the detector is established almost entirely by the drift chamber and this electronics.

1. Overview

See Fig. 1. The front end electronics consists of a 6-channel preamplifier mounted on the face of the drift chamber connected to a postamplifier through 20 feet of coaxial cable. The postamplifier is mounted on the outer face of the detector magnet iron and in turn is connected through long runs of twisted-pair cables to a sampling ADC (for dE/dx measurements) and a multi-hit TDC,[3] both located in a remote electronics building.

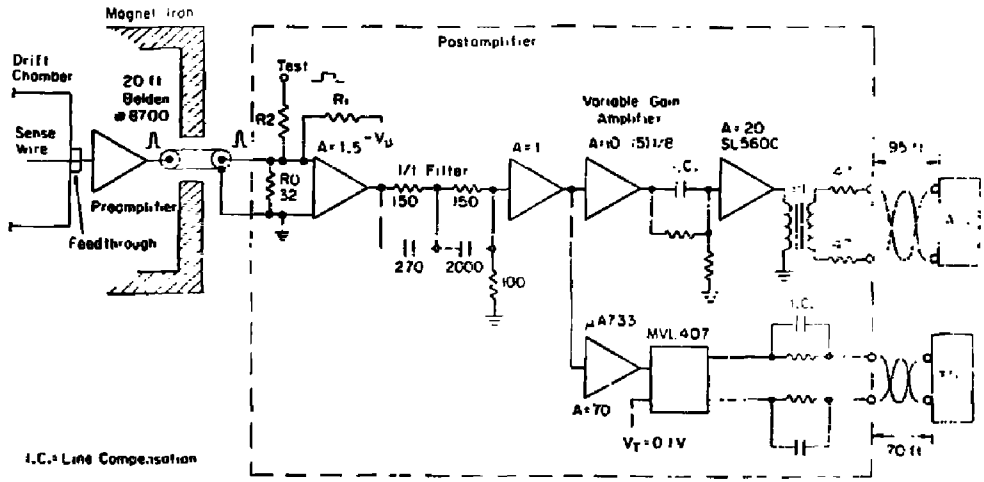
The postamplifier contains a line-receiver followed by a two-pole filter, to cancel the 1/t tail characteristic of drift chamber pulses, followed by a two-fold fanout driving timing and dE/dx measuring channels.

A timing channel consists of an amplifier and a discriminator; a dE/dx channel, of a variable-gain amplifier and line-driving amplifier. Both channels contain filters to pre-compensate the signal shape for the output line distortion.

The postamplifier also receives a calibration signal from a calibration fanout module and transmits it to the four preamplifiers that drive it.

2. The Drift Chamber

See Fig. 2. The new drift chamber has 972 identical cells with six sense wires per cell, yielding a total of 5832 wires and electronics channels. Each sense wire is 2.3 meters long and has an ohmic resistance of 205Ω and a transmission line character-



DRIFT CHAMBER ELECTRONICS

Figure 1 (See Ref. 6)

istic impedance of 390Ω. The development of this chamber has been reported at a previous session of this conference[4] so only the major contributions to the pulse shape will be mentioned here.

Figure 3 shows the pulse shape calculated by successively

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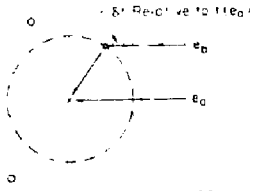
convoluting the single electron pulse shape (curve 1), with a diffusion gaussian with $\sigma = 6$ nsec corresponding to the maximum drift distance (2), then with a geometric function accounting for the variation in drift path length with impact parameter (3), then with a single pole function representing the preamplifier risetime of 9 nsec (4), and finally with the transfer function of the tail-cancelling filter (5). The assumptions are that 80 primary electrons are uniformly distributed along the ionising particle track, that the track is parallel to the sense wire plane, and that the drift field is uniform. The calculated shape agrees with the average pulse shape and has the same rise and decay times to ±5 %. Individual pulses differ strongly from the average, mostly in irregular structure in the trailing edge due to variations in electron drift time. The characteristic positive-ion drift-time is 2 nsec for this chamber, implying a pulse tail amplitude of 2 % peak amplitude 100 nsec after the pulse leading edge for a single electron. The actual drift chamber pulse, the sum of 80 electrons, has a much larger tail, 20 – 25 % at 100 nsec, due to the dispersion in the electron collection time.



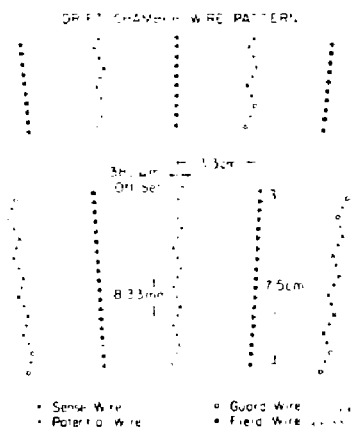


Figure 2

3. The Preamplifier

See Fig. 4. The preamplifier is a voltage amplifier mounted on the aluminum end plate of the drift chamber so that only a few centimeters of PCB trace and jumper cable connect the sense wire to the preamplifier input. The mounting brackets are brass bars soldered to the preamplifier card ground plane at one end, and bolted at the other end to stainless steel studs which are tapped into the drift chamber. The use of stainless steel was not desirable for good grounding but was required for strength, as these studs hold the sense/potential wire feedthroughs and had to be of relatively small diameter. The connection between the copper and steel will be made using star washers and after coating with De-oxide (TM).

The preamplifer input resistance is determined by the equivalent paralleled resistances of the crosstalk compensating resistors, the calibration resistor and the terminating resistor, which is set to 510Ω so that the input resistance will be equal to 390Ω, thus terminating the sense wire in its transmission line characteristic impedance. At the other end of the sense wire is open,

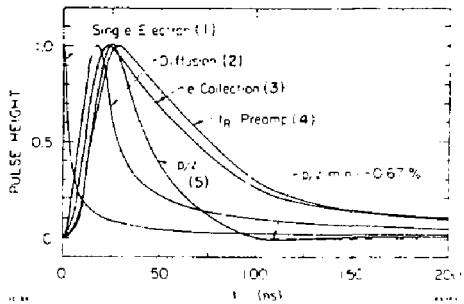


Figure 3

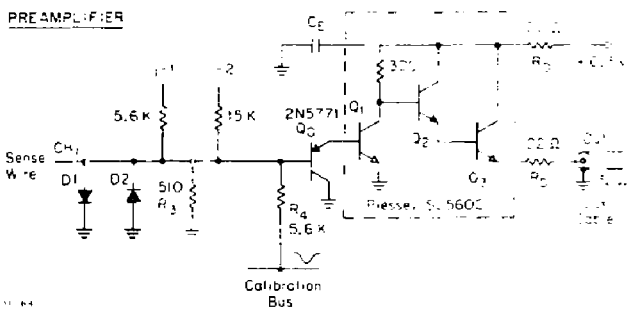


Figure 4 (See Ref. 6.)

there would otherwise be multiple reflections which would degrade the multi-hit performance.

Resistors compensate for crosstalk between adjacent channels and adjacent-once-removed channels. The crosstalk voltage is the sum two components. A positive voltage is induced on the sense wire, approximately 7 % of the signal voltage, by positive ions in the drift chamber. A negative voltage is due to capacitive coupling between channels in the drift chamber, feedthroughs, and preamplifiers, which is approximately 2 - 3 % of the signal voltage, but narrower, because of differentiation, than the signal and positive crosstalk. Since the net crosstalk voltage does not have the same shape as the signal voltage, it would be expected that the crosstalk cancelling network could not be a single resis-

tor, but would have to contain some pulse-shaping components. However, the crosstalk cancelling signal is shaped by reflection in the sense wire transmission line, 18 nsec total reflection time, which by good fortune produces the required cancelling shape to a very good approximation. Thus the resistors need be only adjusted empirically to minimise the crosstalk, reducing it to 0.8 – 1.5 % of the signal voltage. See Fig. 5.

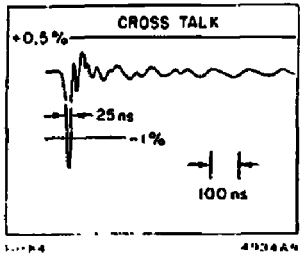


Figure 5

The remaining components directly connected to the input are the protective diodes D_1 and D_2 and the resistor R_4 through which the calibration pulse is injected.

The amplifier configuration is an emitter-follower driving a Plessey SL560C, a bipolar integrated vhf amplifier. The emitter-follower is used to improve the risetime, which would otherwise be substantially increased by the Miller capacitance of the first stage of the SL560C. The net voltage gain is 25; the current gain is $25 \times 390\Omega = 10mV/\mu A$, and the risetime is 9 nsec.

The linearity is shown in Fig. 6. The gain increase in the 1 – 5 mV range of V_{in} is due to the small bias current relative to signal current in Q_3. The gain decrease for the higher values of V_{in} is due to the same effect in Q_1, except that the Q_1 bias current is being decreased by the signal, whereas the Q_3 bias current is being increased, so that the non-linearity of Q_3 dominates for small signals, and that of Q_1 at large signals. The time resolution is not significantly affected by non-linearity in the preamplifier. At present it is planned to correct this curve with the computer, but there is also the option of increasing the bias current in Q_3 by means of a pulldown resistor in the postamplifier which is connected to the Q_3 emitter. Particle identification goals require that measurements of charge on individual wires be linear to ±1%. This goal can be met by software corrections, based on the calibration response, or by increasing the Q_3 bias current from 1.5 to 10 mA.

The noise at the amplifier input is $15.5\mu V$ rms, which decreases to $14\mu V$ (37 nA) when the amplifier is connected to the chamber. The source capacitance is large (30 pF), but this configuration does not show an increase in noise with source capacitance, as do amplifiers with common-base input transistors. A common-base transistor amplifier has three times less noise for source capacitances less than 10 pF, but degrades to essentially the same noise performance with 30 pF source capacitance.

The major noise source is the input termination resistor, with thermal noise equal to $11\mu V$ and shot noise equal to $6\mu V$, for a total noise of $13.5\mu V$. When this is added in quadrature with the amplifier series noise of $7.5\mu V$, the result is $15.5\mu V$.

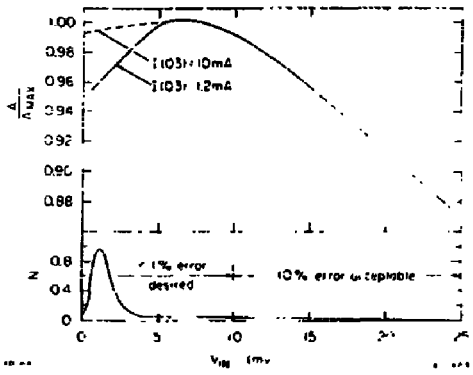


Figure 6

The effect of the noise on time resolution is given by

$$\sigma(t) = \frac{\sigma(V)}{dV/dt} \quad \text{at the threshold voltage}$$

$$= \frac{30mV}{(30mV/\text{nsec})}$$

$$= 1 \text{ nsec}$$

The values for $\sigma(V)$ and dV/dt are measured at the discriminator input at the 100 mV level on the input pulse. The gain from the sense wire to this point is 1930.

The drift chamber space resolution is $150\mu m$ or 3.0 nsec of drift time, so the contribution of the noise to other sources of error in the total space resolution is relatively small. However, EMI voltages will not be known for this detector until Spring 1985, when it will be installed in PEP. The experience of the Mark III at SPEAR, and of the Mark II vertex detector at PEP, has been that the EMI from the stored beams is 150 to $200\mu V$ (peak). Therefore, considerable care is being taken to avoid ground loops in the connection of the HV, power, monitors and preamplifiers to the drift chamber. Also, there will be an increased effort to shield the beam and other transmitters in SLC, the eventual site for the Mark II Upgrade.

The absence of a stabilising resistor in series with the emitter of Q_1, or any other negative feedback, increases the change in amplifier gain with changes in temperature or amplifier supply voltage, V_{cc}.

$$\frac{(dA/A)}{dV_{cc}/V_{cc}} = 1.7$$

$$\frac{(dA/A)}{dT} = 0.002/\,^{\circ}C$$

This requires that V_{cc} be regulated to 15 mV for 5 % gain stability and that the temperature not change by more than 2.5 °C in 6–8 hours, a typical interval between calibrations. Experience in operating the Mark III shows that these conditions are readily met and the benefit realised from not reducing gain by negative feedback is more significant, namely that higher gain

in the preamplifier reduces the effect of EMI on the circuits following the preamplifier.

There are some design considerations required by the relatively inaccessable location of the preamplifiers inside the detector magnet.

A) The power dissipation of the preamplifier is 83 mW per channel or 500 W for 6000 channels. Both the preamplifiers and the drift chamber must not be subject to temperature fluctuations larger than a few degrees Centigrade, so cooling will be done using boil-off gas from liquid nitrogen.

B) The appearance of a short to ground within a preamplifier should not cause a fire or more than one channel to fail. Resistor R_0 is large enough so that the preamplifier side of it can be reduced to 0 volts safely.

C) An oscillation in one channel should not force any of the other 5831 into oscillation. The decoupling between channels is sufficiently high so that the effect of one oscillating channel is to increase the noise in its neighbors, but not to cause them to oscillate. Also, the DC voltage at the emitter of Q_3 is controlled at the postamplifier. An oscillating channel could be biased off remotely.

The resistor R_D back-terminates the cable to the postamplifier and also protects the preamplifier from damage in the event of shorts in the output cable or postamplifier input. Termination of the preamplifier to postamplifier cable is required to reduce reflections to less than 1 %, which again, as for crosstalk and baseline shift reduction, is needed for good multi-hit resolution.

4. The Postamplifier

See Fig. 1. The postamplifiers are mounted on the detector magnet in 12 crates. Each module contains 24 channels and is driven by four preamplifiers, each connected to it through eight 32Ω coaxial cables (Belden 8700): six are signal cables, one a low-voltage power cable and one a calibration cable.

The cable was chosen for small outside diameter, minimum signal distortion and good mechanical strength. The consequence of satisfying these requirements was the selection of a cable with a fairly large diameter center conductor, which, combined with the small O.D., determined the low characteristic impedance of 32Ω . This low impedance increases the nonlinearity of the preamplifier, but was the concession made to obtain the other advantages.

The input circuit consists of a 32Ω terminating resistor, R_0, a resistor for injection of a test pulse, R_2, pads on the PCB for loading a transformer should it be necessary to isolate postamplifier and drift chamber grounds, and pads for loading a pull-down resistor, R_1, to provide the option of increasing the bias current in Q_3 of the preamplifier.

The input amplifier is an inverting buffer with voltage gain of 1.5.

The two-stage R-C filter shapes the drift chamber pulse to return to baseline within 100 nsec with less than 1.2 % residual amplitude. (See Fig. 7.) It compensates not only the $1/t$ tail of the drift chamber signal, but the distortion produced by the preamplifier cable and also the pulse-shaping effects of the preamplifier.

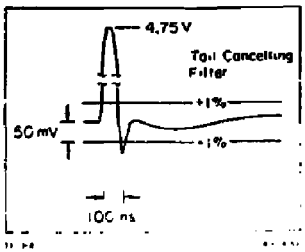


Figure 7

An emitter-follower buffers the tail-cancelling filter, driving both the timing and dE/dx channels. The timing channel uses a $\mu A733$ integrated amplifier with a voltage gain of 70, and a LeCroy MVL407 comparator. The amplifier has good risetime (4nsec) and good overload recovery; the gain returns to 70 within 12 nsec after a 4x overload. The MVL407 threshold error is 3 mV, which produces negligible error at the nominal setting of 100 mV, which corresponds to $50\mu V$ at the sense wire. The threshold may be varied between 30 mV and 1 volt, to accomodate future changes in system gain due to drift chamber voltage or gas changes. The output signal is a full ECL differential signal with pulse-width equal to time-over-threshold. The network on the output reduces the tail on the signal due to line distortion (Fig. 8).

The dE/dx channel adapts to changes in system gain with a variable-gain stage[5] (Fig. 9). The relative gain can be set from 0 to 15 in integer steps by biasing on the appropriate combination of the four input transistors with their gains of $\frac{1}{8}-\frac{2}{8}-\frac{4}{8}-\frac{8}{8}$. The gain setting is controlled by four bias-voltage busses on each module, each bus connected to the same binary-weight transistor on all 24 channels, and driven directly from a bus on the crate backplane. Thus all modules in a crate and all channels in a module must have the same gain setting. Following the variable-gain amplifier is a line-compensating network and a Plessey SL660C. A transformer converts the Plessey output signal from single-ended to differential. The output is back-terminated to minimize reflections to improve multi-hit performance.

6. Calibration

See Fig. 10. A central pulse generator provides the calibration pulse for all channels. It is pre-shaped to resemble a drift chamber pulse so that the shape at the input to the ADC also resembles drift chamber signals. The pulse generator can also produce a pair of pulses with different amplitudes and arbitrary separation in time. The fanout from the calibrator to 6000 channels is a tree of resistor-dividers, coaxial relays and complementary drivers, a circuit with good gain and delay stability. The long run of cable from the calibration pulser location to the postamplifiers is made through a cable with $10ppm/\deg C$ delay stability. The postamplifer to preamplifier calibration cables will be matched in delay to less than 0.5 nsec. The channel-to-channel variation in delay in the pulser-to-preamplifier fanout is less than 0.5 nsec. The channel-to-channel uniformity of calibration input pulse heights is better than ±4%, with systematic errors less than ±1% The fanout system can also pulse portions

of the electronic system for crosstalk studies and can pulse the postamplifier inputs for test purposes.

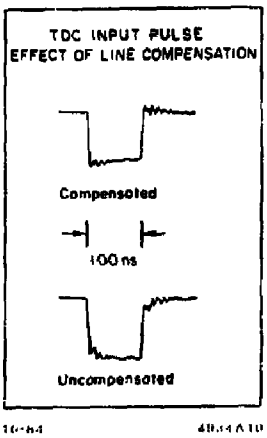


Figure 8

7. Summary

The preamplifier, postamplifier, and cables described have been extensively tested on prototypes of the Mark II drift chamber. Performance of these prototypes has been discussed in Reference 4. The electronics has been seen to contribute insignificantly to drift-time and pulse-height resolutions and to multiple-hit performance. In addition, the circuits have been found to be stable, and should be sufficiently flexible to accommodate a variety of operating conditions and environments. The full system is currently being implemented and will be operational along with the new drift chamber in Spring 1985.

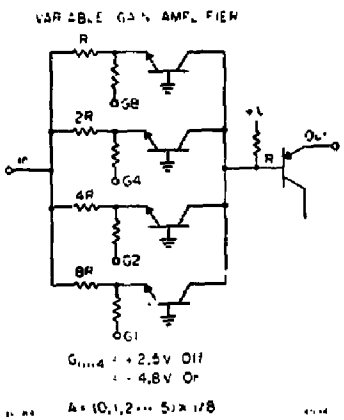


Figure 9 (See Ref. 6.)

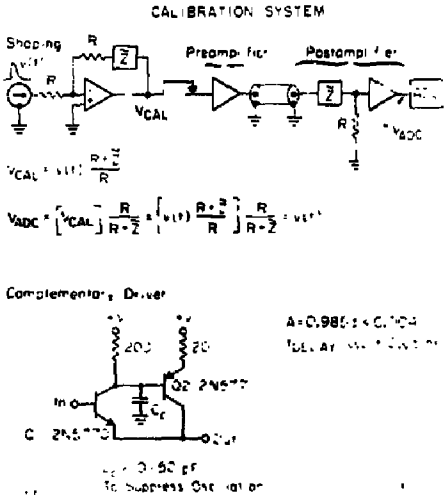


Figure 10 (See Ref. 6.)

References

1. University of California, Santa Cruz, California 95064.
2. Institute of High Energy Physics, Academia Sinica, P.O. Box 918, Beijing, People Republic of China.
3. LeCroy 1879 TDC.
4. ?. Burchat, et al., "The New Drift Chamber for the Mark II Detector at the SLAC Linear Collider," these Proceedings.
5. V. Radeka, BNL, aided in the design.
6. Schematic does not show DC biasing or power filter components.