Fermi National Accelerator Laboratory

FERMILAB-Conf-85/156
2530.000

THE RABBIT SYSTEM
LOW COST, HIGH RELIABILITY FRONT END ELECTRONICS
FEATURING 16 BIT DYNAMIC RANGE*

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October 1985

*Presented at the IEEE Nuclear Science Symposium (NPS), San Francisco, California, October 23-25, 1985.

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Abstract

A new crate-based front end system has been built which features low cost, compact packaging, command capability, 16 bit dynamic range digitization, and a high degree of redundancy. The crate can contain a variety of instrumentation modules, and is designed to be situated close to the detector. The system is suitable for readout of a large number of channels via parallel multiprocessor data acquisition.

Introduction

The RABBIT (Redundant Analog Bus Based Information Transfer) system is the front end portion of the data acquisition system presently being implemented at the Collider Detector Facility (CDF) and E-706 at Fermilab. For CDF [1] there are approximately 100,000 individual signal sources consisting of photomultiplier tubes; strip, wire, and pad chambers; drift chambers; and drift chambers with current division readout. The 2000 ton detector must move 100 feet between the assembly hall and the collision hall. Typical cable runs between the detector and the control room are 200' long.

A very large detector offers the opportunity to design a consistent, optimized system with the prospect that the engineering costs can be small compared to those of production. The new system can then be less expensive than one assembled from modules already existing, but not optimally matched to the requirements. The initial plan was to design all the electronics in FASTBUS as the instrumentation system of choice for large detectors. As the design proceeded, it became apparent that FASTBUS would not be suitable. Many needed items were not available when this design was begun. Furthermore, the required dynamic range could not be achieved in a system with cohabiting digital circuitry powered by switching power supplies.

It was therefore decided to design a system which would be optimized for front end electronics. Previous experience with large liquid argon [2] and proportional chamber systems gave promise that the techniques used there could meet the dynamic range requirements of the CDF experiment.

Design Requirements

The CDF detector operates in the main ring tunnel at Fermilab where access is not possible during machine operation. Since the production of a useable quantity of antiprotons will take on the order of eight hours, an access will result in a similar loss of useable beam time. It is thus essential to design so that satisfactory operation can be achieved with access only during weekly maintenance.

The overriding design specification was that the system should be able to read many calorimeter channels for which the ratio of full scale signal to calibration signal would be of the order of one thousand to one.[3] It was further desired that the calibration signal be measurable to an accuracy of 1%. Thus the system needed to perform over a 100,000 to one dynamic range.

Electronics Location

In the past, ADC systems with wide dynamic range were attempted by using two amplifiers of different gain, but it has generally proven difficult to calibrate the gain ratio. The primary difficulty is that the gain calibration involves splitting wide bandwith signals with the result always strongly dependent on rise time. Further, transmitting signals of even moderate dynamic range over long distances to a control room is difficult unless the signals are first preamplified with rather complex circuits. Since much of the front end electronics was already needed on the detector, the decision was made to put all of it there and to make it as reliable as possible.

System Design Concepts

With the opportunity to design a very large system from scratch, it was decided to formulate design rules which would be applied consistently to the entire detector.[4] The following are some of these guiding design concepts:

1) Low level signals would be digitized as close as possible to their source.

2) Circuits would be designed for low power, would not be densely packaged, and would thus have low temperature rise to promote reliability. All circuits would be designed for operation at high temperature so that operation could continue if the cooling were to fail. All circuits were to be burned in at elevated temperature to reduce infant failures.

3) Redundancy would be provided if possible wherever a single component failure could cause loss of many channels of data.

4) All processing would be located in the control room. Logic at the detector would be limited to simple register operations. Registers at the detector would be readable to provide for testing.

5) There would be only digital links (with parity added) between the control room and the detector so that problems could be detected.

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6) Circuits were to be designed to be insensitive to power supply fluctuations at the 10% level to reduce problems associated with power distribution. Circuits should continue to operate in the event of overvoltage due to normal power supply failure modes.

7) All systems would contain built-in test features to perform electronics calibrations and verify operation to within specifications. Sufficient monitoring would be built in so that all power supply levels and generated signals could be monitored.

8) All power supplies would be of the linear type, because noise from switching type supplies proved to be an obstacle in achieving the required dynamic range. In order to reduce supply size, permit operation close to the crates, and to minimize power dissipation at the detector, all supplies would be operated from tightly regulated 3 phase 400 cycle motor generator sets. The supplies would be designed so that normal failure modes would not produce voltages in excess of the circuit tolerance.

9) Operation would be such that the digital bus to the control room would never be active while low level signals were being acquired. The system would alternate between periods of noisy operation, with the digital readout bus active; and quiet operation, when signals would be amplified and captured in track and hold circuits.

10) The crate would contain two independent buses, each capable of multiplexing analog and digital signals.

11) All cards would contain a PROM which would contain the Module Name, Serial Number, Revision Number, and Property Number.

12) Integrating amplifiers would be designed so that their input impedance would be resistive and matched to the cable impedance. Where possible, sources would be back-terminated with the cable impedance to reduce the possibility of oscillation.

13) Wide gain range would be achieved by integration of signals with precision capacitors. If additional gain range were needed, it would be achieved by post-amplification of the integrator output by operational amplifier techniques with precision resistors.

Implementation

The requirements of low cost, low power density, and redundancy lead to large card designs since otherwise there is no space left on the card for circuitry. The card chosen is 16.875" tall by 12.75" deep, or 5 by 6 Americard units (the size of a standard American Credit Card). The card is taller than it is deep for economical use of card space. The long connector edge provides sufficient space for input and output connections at the back of the card, allowing input connections to be permantly attached to the crate while cards are changed.

The crate design contains 25 card positions. One is permanently assigned to the timing and control module, and two are assigned to digitizer modules, leaving twenty-two useful positions.

There are two nearly independent read-out buses. Each bus is connected to its own digitizer module and has an independent digital bus path to the control room. Each crate has two complete sets of power supplies powered by separate power mains. Power is distributed independently on each bus with the two power sources joined by a Shottky diode "OR" at the card. Since the diode drop cannot be accurately controlled, the circuits are designed to be insensitive to the expected voltage variation. Each supply set has a capacity of 680 watts. The policy is to limit the load to approximately 70% of the supply rating. During normal operation the redundant pair operates at 35% of its rated load where operation is quite cool. No effort is made to balance the loads.

The primary method of measurement is to convert a signal to a sampled voltage. This is always done twice, once for the measured quantity and once for a reference. For CDF ADC's this is done by taking two measures of an integrated signal, once before the interaction time and once after. For fixed target ADC circuits, each channel contains a delay line whose output is sampled before and after the signal exits the delay line. Time to digital circuits usually involve a current source, an integrating capacitor, and measurement of both the capacitor reset voltage and the timed voltage. These dual samples are then carried through the system as a differential pair. The differential scheme is always used. For example, when measuring a power supply voltage the local ground is connected to the low side of the differential pair. Most non-signal interferences tend to appear as common-mode noise on the differential pair and thus cancel in the differrence circuitry of the digitizer module. In particular, ground loops appear as slowly changing common mode signals since their rate of change during the sample interval is small.

Major Components

The following lists only the major system components. The listed cards are being produced in quantities of 75 to 600 cards. There have been several hundred one of a kind modules built for various tests, some quite sophisticated. For example, one early module was a very slow, very linear digitizer module built around the ICL 7104 ADC chip. With an appropriate sample and hold circuit this allowed highly precise measurements to be made of elements like bus settling time, amplifier linearity, sample and hold droop, and other items critical during the design phase.

The following brief specifications are presented to give some idea of the range and precision of the designs. A more detailed look at one of these designs, the PM ADC, is presented in a companion paper at this conference.[5]

The Scanning Processor (MX)

The MX (One more than the earlier design - the M7 in octal)[6] controls the digitizer module at the detector and

interfaces to FASTBUS for upstream data processing. The MX downloads pedestal values to the EWE-II and buffers event data for processing by FASTBUS.

The MX is a four address ECL processor with two independent buses for communication over distances of several hundred feet to up to four EWE-II digitizers on each bus. It communicates to FASTBUS for off-loading data. It contains a four event buffer and lists for controlling up to 8 EWE digitizers. It can process a complex four address instruction every 100 ns.

A typical instruction is C = A*X + B where A,B,C, and X are indexed. There is also an instruction for defining a stack for use with subroutine calls as well as efficient instructions for controlling the EWE list. The MX is used for acquiring and correcting data from the RABBIT system as well as collection and processing of calibration data.

The Digitizer (EWE-II)

The EWE-II (Event Write Encoder - Version 2) accepts pedestals, channel addresses, and control words from an MX. It addresses the selected channel and digitizes the sampled-and-held voltage. Digitization can be made to be contingent on the presence of interesting data by requiring that the channel output be greater than pedestal by a pre-selected threshold value.

The EWE-II contans a 16 bit successive approximation analog to digital converter with 17 us conversion time. The total time required for bus settling and threshold comparison is 3 us. Threshold comparison can be made within 0.1% of full scale. A variety of gain, threshold, polarity and offsets can be MX selected. Linearity is better than 0.01%. Temperature stability is < 1 count per degree C.

The Timing Gate Generator (BAT)

The BAT (Before After Timer) receives a front pannel signal from the trigger system and generates timing signals required to control the acquisition of data by various front end modules. The BAT contains separate TDC circuits to monitor all the timing signals it generates. It also contains a crate reference voltage, a computer controlled variable reference voltage, a computer controlled timing generator for testing TDC circuits, a temperature monitor, and read out of power supply voltages.

PM ADC

The PM ADC card contains twelve photomultiplier channels. Each channel reads the signal and the signal amplified by a factor of 16. Both signals are digitized by the sysytem to 16 bits. The x1 to x16 ratio is accurate to 0.1%. Average photomultiplier tube current is also read for calibration of the detector by a source. A fast output signal is provided for use by the trigger system. This design is described in detail in a companion paper at this conference.[5]

PM TDC

The PM TDC card contains eight common stop TDC's. The individual starts are the amplified and discriminated sums of 2 phototube dynode outputs. Discriminator threshold is appriximately 1 mv (sum of the two inputs). Full scale range is 3 microseconds and the response is linear. Individual and OR'ed timing signals are available at the front panel.

In laboratory bench tests, the response lies within 1/2 nsec of the best straight line for the first 600 nsec of the 3 microsecond range. Intrinsic timing jitter is about 200 psec and temperature coefficients are typically 100 psec per degree C.

MUON ADC/TDC

The Muon ADC/TDC card contains eight identical sections, each servicing the two ends of a charge-division drift tube operating in limited streamer mode. Each section contains two charge integrating amplifiers for charge division position measurement along the wire and one TDC for drift time measurement of position transverse to the wire. Full scale for the integrators and the TDC are 250 pC and 3 microseconds respectively. Response is linear for both charge and time. In laboratory bench tests, intrinsic integrator noise is less then 20 fC and intrinsic TDC jitter is typically 1/2 nanosecond. The common-stop TDC is started by a low level discriminator which sums the outputs from the wire ends. TTL timing signals from the TDC's and certain analog sums from the integrators are available on front panel connectors for trigger purposes.

In cosmic ray tests with the drift tube detectors, the system achieves 3 mm (0.07%) spatial resolution along the 5 meter long wire and 200 micron position resolution across the 8 cm wide drift cell.

LAC ADC/TDC

This card, designed for the large liquid argon calorimeter of Fermilab experiment E-706, contains 16 high gain-bandwidth charge integrating amplifiers and four two-hit capacity common-stop TDC's which are started by low level discriminators connected to the summed outputs of four integrators. Full scale charge and time are 50 picocoulombs and 2 microseconds respectively.

Trigger signals derived from the integrator outputs are available at front panel connectors. The integrator outputs are delayed in 800 nanosecond packaged delay lines before reaching the sample-and-hold circuitry in order that the front panel outputs can be part of the overall trigger decision. The TDC stop signal is derived from one of the sample-and-hold gating signals.

Capacitances of the E-706 detector pads will range from 0.1 to 10 nanofarads. The amplifiers will be connected to the detector by low impedance (6 to 12 ohm) strip lines with 60 nanosecond propagation delay. The

amplifier open loop response has been designed so as to result in an integrator input impedance of 12 ohms, with expected variations of 15% to 20%. In the present prototype versions, the overall system is stable and achieves 10% to 90% rise times of 150 nanoseconds with a 2 nanofarad detector capacitance and 12 ohm strip line back-terminated with 10 ohms at the detector. Noise charge is well described by Sigma(q) = 4.9*sqrt(C), where Sigma(q) is in femtocoulombs and C is the capacitance, in nanofarads, of the detector plus interconnecting strip line. For E-706, typical detector and cable capacitance will be of the order of 10nf, resulting in about 15fC noise charge. The TDC's are expected to measure hit times to better than 10 nanoseconds, after time slewing is removed with amplitude-dependent corrections, in spite of the rather long (500ns) charge collection times in the calorimeter.

Production of 600 LAC cards (9600 channels) will begin early in 1986.

WIRE AMP

A thirty two channel negative input card with a full scale charge sensitivity of 75 pC and 16 bit resolution.

STRIP AMP

A thirty two channel positive input card with a full scale charge sensitivity of 15 pC and 16 bit resolution.

HI WIRE

A thirty two channel negative input card with a full scale charge sensitivity of 250 pC and 16 bit resolution.

POWER SUPPLIES

Power is supplied by modular 210 cubic inch, 10 pound units each with 340 watts capacity in various voltage combinations. The supplies are linear with [3mv RMS noise and ripple and efficiency of 65 - 75%. These supplies operate from 120/208V, three phase, 400 Hz MG sets. Bayonet mounting with snap in connectors allows easy change.

Operational Results

The system has recently finished the first engineering run in the Fermilab B0 collision hall. There were three accesses during five operating weeks. About 100 cards were returned to the shop during the process of installation, the largest return category being modules which were operational but which were mis-diagnosed in the field because there existed only preliminary installation diagnostic programs. About 10 real failures occurred during the 90 shift installation period. After the detector was moved into the collision hall, there were 5 control modules changed, of which only two or three now appear to have been real failures. There were no electronics failures in approximately 10,000 installed front end channels and no failures in seven operating MX's. Operation of all channels was periodically monitored by reading pedestals, and through calibration runs using the on-board pulsers. Since the redundant features of this system are yet to be implemented, this relatively low failure rate is attributed to the conservative designs, the low operating temperatures, and to the laboratory burn in and testing.

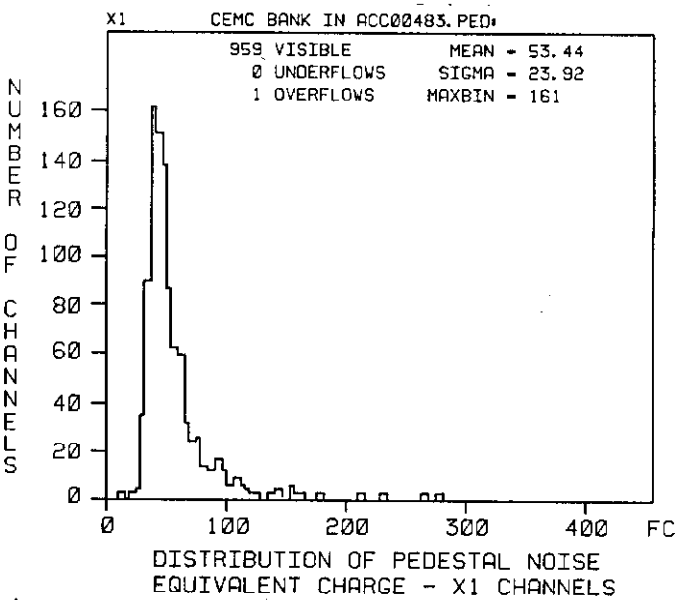

Figure 1. Pedestal noise run for 960 photomultiplier channels on the CDF detector. This is the X1 channel which directly integrates the signal. Full scale is 750 pC.

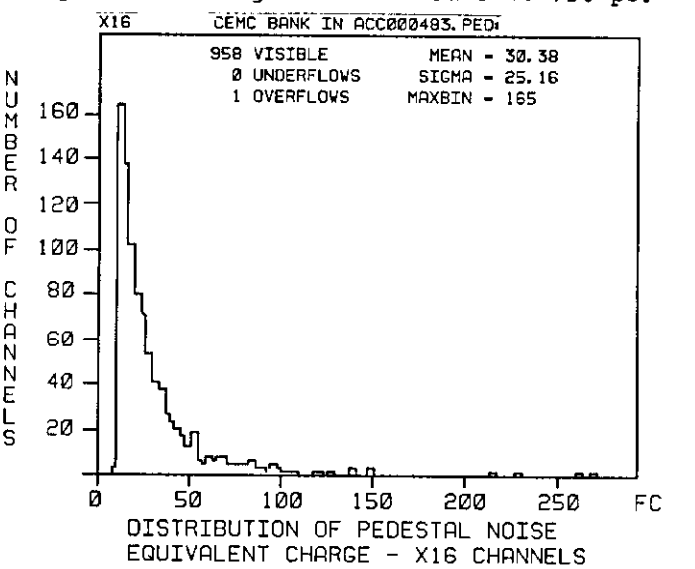

Figure 2. Pedestal noise run for for the channels of Figure 1., where the signal is amplified by a X16 amplifier after the track-and-hold.

There is only a small difference between the noise level measured in the laboratory and the system noise level on the detector. In the laboratory, this is typically 1 to 2 counts RMS out of 65,535 counts full scale. Figure 1. is a pedestal run taken on the detector showing the RMS noise for 960 PM channels. Figure 2. is the same measurement for the X16 channels on these amplifiers. It should be noted that the X16 noise is somewhat less than 16 times the X1 noise which is consistent with the reduction

of ADC quantizing error since the converter used is not of full 16 bit accuracy. Another explanation for somewhat higher noise on the detector is that the software does not yet take advantage of the skip-if-under-threshold feature of the EWE-II's and, furthermore, that only 12% of the final number of MX's are reading out the entire detector, with the result that the track-and-hold circuits must be stable for 40 times their design hold time.

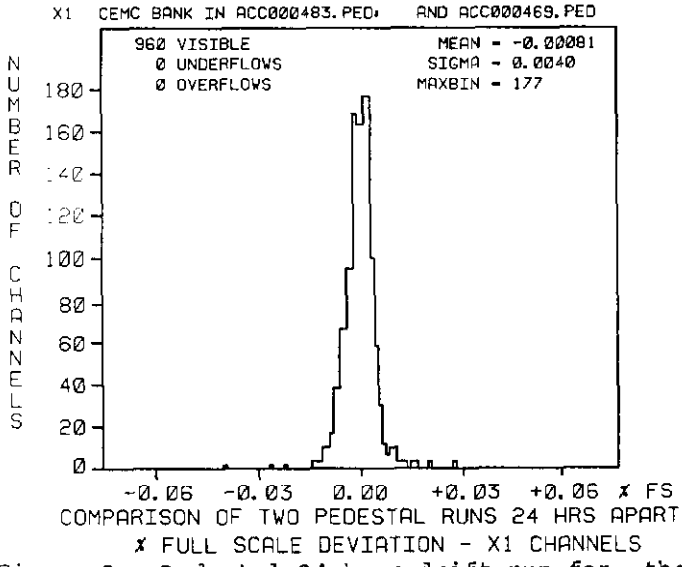

Figure 3. Pedestal 24 hour drift run for the channels of Figure 1. Distribution is for all channels.

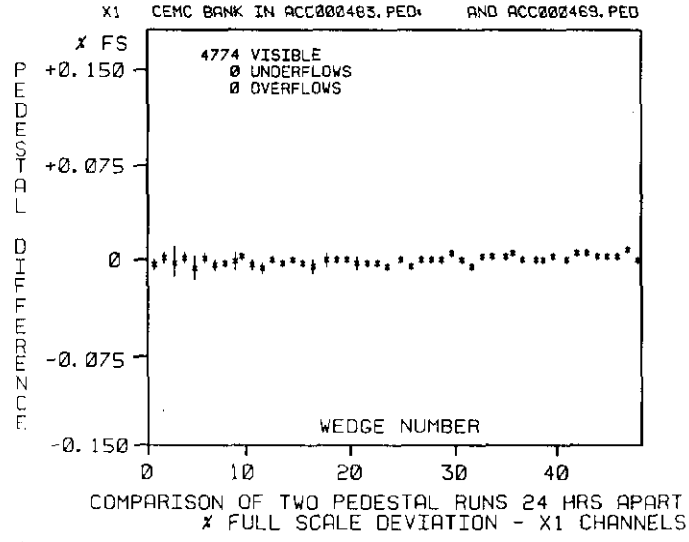

Figure 4. Pedestal 24 hour drift run with channels grouped by wedge (detector sub segment).

Figure 3. is a pedestal drift run taken over a 24 hour interval. Individual channel drifts can be directly correlated with temperature and are typically 30 parts per million per degree C. Figure 4. shows the pedestal differences averaged over each detector wedge segment. This type of plot is useful for locating drifting channels. Because of the difference method used, an individual channel can drift either direction with temperature. The data is consistent with a two degree temperature change in the collision hall, and the measured 30 part per million of full scale per degree C pedestal drift.

A Comment on Redundancy

Without redundancy there would be about 780 power supply channels in the collision hall, where a multi-output supply is counted once for each voltage. From Fermilab's equipment pool records, a failure rate of one per 50,000 channel hours is estimated for supplies in the high energy physics environment. Using this data to estimate the CDF failure rate, one expects a mean time to failure of 64 hours. Since periods between access are about 150 hours, it is very likely that a supply will fail every time the detector is closed up. The rigorous argument is even less favorable since the first failure is likely to occur before the mean time. With parallel supplies, it is expected that the mean time for the first crate loss due to supply failure is at least ten days. In practice, other failure modes may become more important. We continually discover new ways the intended redundancy is defeated. The power supplies are powered from two separate circuits all the way back to the control room, but random electricians can decide to turn off every switch in sight. A blown fuse on a card could, in the original design, cause both buses to be pulled to ground. This failure mode was discovered and circumvented, but in a complex system it is unlikely that true redundancy can be achieved. Many items, i.e. the clock, cannot be made redundant without introducing more problems than the redundancy solves. The attempt made was to reduce the number of items which could take down a large portion of the system.

One reason for designing a new system was the desire to make the bus structure redundant. Experience with CAMAC indicated that the most troublesome failures were those which caused a bus problem. There was little way to clear a problem without removing all the modules one at a time hoping for the trouble to clear on an identifiable module. As often as not, shuffling modules introduces more problems than it cures.

The bus was designed to be as simple as possible and has been implemented using only 10 standard integrated circuits and 10 square inches of board space for each combined analog and digital bus.

With two buses it is often possible to use one bus path to diagnose the other. In most cases it is possible to identify the failing device without removing any module. This should be particularly useful when access is limited, because the problem can be thoroughly diagnosed before entry into the radiation area for repair.

A redundant system is of little value without a test program. The BAT's have been designed, for example, so that they measure both sets of power supply voltages before the card diode OR. It will be important to actually measure the supplies periodically so that faulty ones can be replaced before their now heavily loaded partner fails also. The reality of High Energy Physics is such that preventative maintenance programs of this kind

are boring and often the last feature to be implemented.

System Diagnostics

There are many diagnostic features built into this design. One concern was that digitizing the signals at the detector would result in noisy or failing channels being discovered only after computer analysis of many events could reveal abnormally wide pedestal distributions or abnormally infrequent channel occurrence in the data buffers. A multiplexing scheme was therefore designed as part of the standard card design whereby it is possible to connect the analog output of each front end amplifier directly to a cable to the control room. This has already proven to be useful for detecting problems such as high voltage breakdown in phototube bases.

The PROM identification proved to be very helpful during checkout. It was very comforting to plug in a new set of cards and have four layers of computer operating system report back the ID's of the cards which had just been inserted.

The many voltage and time monitors were also useful during checkout. By the time all the test signals had been read, a thorough test of the system had been made.

Production Costs

The redundant features do not add significantly to the cost. A typical card containing 36 data channels costs about $500 to produce in 100 quantities. This is broken down to $25 Board, $50 Assembly, $300 Parts, and $125 technician time for testing. Of this cost, about 10% could be attributed to the second bus and multiplexers associated with reading every channel by two paths.

The above costs do not include the MX processors, crates, digitizers, power supplies, etc.. One way to give a better estimate of true cost is to divide the project total budget by the number of channels in production. This includes some, but not all of the engineering cost and is presently expected to be $40 per channel. There is an average of about 30 parts per channel for the entire system.

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