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DATA PROCESSING IN AGS EXPERIMENT 780

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Experiment 780 is a search for the rare K decays $K^0_L \to \mu e$ and $K^0_L \to e^+e^-$. We will be sensitive to these decays if the branching ratio is above 10^{-10}. To achieve this in a 1000 hr. experiment will require an intense beam with about 2×10^5 K decays/sec in the three meter decay region and over 10^7 counts/m^2/sec in the apparatus. We will need a multilevel event selection sequence which will accept good events with high efficiency but quickly reject most of the background events.

THE FAST TRIGGER

A schematic representation of the E780 detector is shown in Fig. 1. Drift chamber modules (xx'yy') are placed upstream and downstream of the 72D18 spectrometer magnet with a transverse momentum kick of 220 MeV/c. The four modules are labeled A-D. Electrons are identified in the lead glass and hydrogen Cerenkov chamber. Muons are required to penetrate into the range stack. Scintillation counter arrays are labeled E, G, H, and I. The fast trigger is implemented using 100K ECL logic. The risetime, transit time, and transit time dispersion are about 800 psec. per gate. The fast trigger requires an electron have a coincidence between a quadrant of the Cerenkov counter, an E scintillation counter in that quadrant, and at least 1.2 GeV pulse height in the appropriate lead glass quadrant with no hit in that H quadrant. The e^+e^- fast trigger then requires two such quadrants on opposite sides of the beam, with only two E counters hit. The muon requirement is an E, G, H, and I quadrant in coincidence, with no Cerenkov hit in that quadrant, and less than 1.2 GeV in that lead glass quadrant. The pion requirement is an E and G quadrant in coincidence with no Cerenkov hit or H hit in that quadrant. The four trigger types are $\pi\pi$, $\mu\mu$, μe, and ee. All types require exactly two hits in the E array. The $\mu\mu$ trigger further requires only two hits in the I array.

Drift chamber information from the ORs of the outputs of four drift chamber discriminators is used in the trigger. We require at least one hit on either side of the beam in the A and B chambers (x and x' planes) and rough parallelism ($\pm$ 25 mrad), after the spectrometer magnet in the C and D chambers. This part of the trigger is implemented in 10K ECL logic with about 2 nsec. transit time per gate. The risetime and transit time dispersion are also about 2 nsec.

BROOKHAVEN FASTBUS

This is the third experiment in which we have used Brookhaven Fastbus [1]. A schematic representation of the E780 seven segment Brookhaven Fastbus system is shown in Fig. 2. The segment interconnect modules contain the arbitration logic for the lower segment and the broadcast register besides connecting cable and crate segments. All slaves can be read out in under 100 nsec per dataword. The lead glass ADC modules and the drift chamber TDC modules store their encoded data in an onboard FIFO memory. The ADC modules subtract pedestals and only present hits above a settable threshold. The Fastbus List Processor (FLIP) reads out the slaves and stores the data in the two megabyte Fastbus memory. This memory is large enough to contain all the events from one AGS spill. The host computer therefore analyzes events over the full AGS cycle. The FLIP takes about 200 nsec to read a data word from a slave and store the data in memory. This memory is two-headed - the FIFO write port is on the crate segment while the FIFO read port is on the cable segment. There is an additional address on the cable segment which causes the FIFO read counter to advance to the beginning of the next event when addressed. Thus the computer may quickly end processing one event and jump to the beginning of the next event.

The TDC spy resides on the lower cable segment. It examines the TDC data as the FLIP reads the TDC modules and signals the FLIP via a coaxial cable if there are less than two hits per horizontal plane or less than one hit per vertical half-plane or too many hits in the chambers. The FLIP then writes the abort word to the segment interconnect broadcast register, which issues a global abort broadcast. This clears the slave modules and the FIFO read pointer is reset to the beginning of the event. The spy also prevents TDC data with drift times outside of a programmable range from being written into memory and requires hits in the vernier (say x') plane to have contiguous hits in the upstream (say x) plane to be recorded. We are now building a DEC Q bus to Fastbus cable segment interface which will allow us to put a J11 processor on the upper cable segment to preprocess the data.

CONCLUSION

We are preparing a seven segment Brookhaven Fastbus system for AGS experiment 780. The data is filtered and buffered in a two megabyte Fastbus memory. Parallel processing will occur in the TDC spy, Fastbus list processor, J11 processor and PDP 11/44 host computer. We will take data in spring 1986.

REFERENCES

[1] L.B. Leipuner, et al., IEEE NS-30, No. 5, 3773 (1983); G. Benenson, et al., ibid, 3958 (1983); W.M. Morse, et al., ibid, 3964 (1983).

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