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PROTOTYPE VME DATA ACQUISITION CARD FOR THE ZEUS CALORIMETER

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ABSTRACT

This paper discusses the design of a prototype data acquisition (DAQ) card for the ZEUS calorimeter. The card accepts two multiplexed analog data streams at a 1 MHz rate, and digitizes and stores the data for subsequent transfer through VME to a host computer. The data is buffered by a high-speed asynchronous FIFO following the A/D converters, and written into Data Memory on the card, either directly or after processing by an on-board digital signal processor (DSP). Each card has a 16-bit control-status register (CSR), the bits of which configure the hardware and define the hardware options. The 1/4 Mbyte of high speed CMOS static RAM appears either as a FIFO, or mapped memory depending upon a bit in the CSR. The card is designed to make use of the 32-bit data and address buses supported by VME, and accordingly can be most efficiently utilized in conjunction with a processor in the VME environment such as the 68020, which supports longword transfers in a 32-bit address space. The card is constructed on a ten layer printed circuit, with almost all components being surface-mount devices. All logic is implemented in PLD's.

INTRODUCTION

The High Energy Physics Division of Argonne National Laboratory is a member of the U.S. participation in a multinational collaboration to build the ZEUS detector[1]. The U.S. group will design and build the barrel calorimeter for the detector, and provide the electronics used for data acquisition with the calorimeter. The calorimeter is composed of layers of depleted uranium and plastic scintillator, which is coupled optically to photomultiplier tubes by waveshifter bars[2]. The output of the photomultipliers is carried to electronics resident within the calorimeter modules. This electronics consists of linear shaping filters, analog storage devices, and analog buffering and multiplexing devices[3].

When conditions which constitute a first level trigger (an event) are detected by the trigger logic, the front-end logic causes the analog storage devices to stop commutating. The stored analog quantities corresponding to the event which created the first level trigger condition are then transferred to an analog buffer. These buffered quantities are then multiplexed over 40-meter twisted pair cables to the data acquisition electronics which resides in a VME environment in an adjacent facility. This "front-end electronics" is located in the calorimeter modules themselves, and is subject to the radiation and thermal environments of the modules.

This document describes the design of a prototype version of the data acquisition card which acquires these streams of multiplexed analog data from the front-end electronics. A high and low gain stream of data are input into two 1 MHz 12-bit A/D converters on each DAQ card within the multi-crate VME environment, and are processed for subsequent transfer to a host computer. Figure 1 shows a version of this multi-crate environment. The digitized data is buffered by a high-speed asynchronous FIFO, and subsequently written into on-card Data Memory (256 Kbytes), either directly, or through a DSP[4]. The Data Memory is accessible at any time to the VME bus.

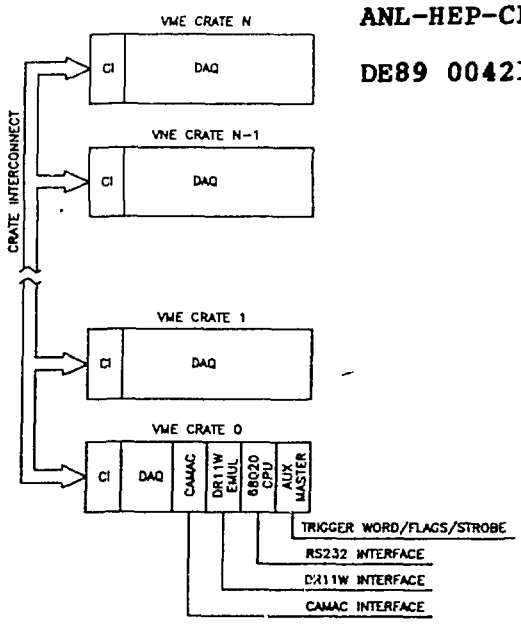

Fig. 1. A configuration of a multi-crate VME environment in which the DAQ cards reside.

Digitized/DSP'd data can either be written into Data Memory as if the memory were a FIFO, written into sequential addresses with addresses supplied by the on-board address register, or written into "pages", such that each event begins at a 256 longword page boundary. The DAQ card is designed to make use of the 32-bit data and address buses supported by VME, and accordingly can be most efficiently utilized in conjunction with a local processor such as the 68020, which supports longword transfers in a 32-bit address space.

CONCEPTUAL DESIGN

This data acquisition card is intended to be a prototype for the card which will actually be produced to acquire data in the final ZEUS detector. For this reason, an attempt was made to include a large range of capabilities and features on this card. Some subset of these features which had been found not particularly useful would then subsequently be deleted when the design was revised for the production cards.

The following is a partial listing of guidelines followed in the design of this card:

1. All logic, decoding, etc. is implemented in PLD's. Address and data buses carry 32 bits. All hardware is surface mount.

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2. All memory and registers can be written/read from VME.

3. Hardware supports VME block transfer protocol.

4. Hardware supports global broadcasts on VME.

5. Rows a and c on J2/P2 are not used so that a parallel bus protocol such as VSB may be implemented to facilitate the second level trigger.

6. VME address space allocated to the DAQ cards begins at 140000H.

7. Each DAQ card uses 40000H address space. Data Memory address space across all the DAQ cards as seen by the 68020 is contiguous.

8. All data transfers to Data Memory are longwords. All data transfers to DSP Memory and registers are word transfers.

9. Logic allows fast asynchronous FIFO buffers to accumulate data while VME is interacting with Data Memory.

10. Bits of the CSR convey information regarding status or configuration of a card. The CSR may be written/read from VME at any time. A subset of CSR bits is OR'ed to drive jumper selectable IRQ line in VME.

12. DAQ cards are organized so that inclusion of a DSP is optional. Buffer output writes directly into FIFO/RAM if DSP is not present.

CARD TOPOLOGY

Figure 2 shows a block diagram of the hardware on the DAQ card. Analog data entering the card is digitized by two AD9003 12-bit A/D's on 1 μsec clock edges received by the card through the serial clock (SERCLK) VME line. The clock signal is provided by the front-end electronics, since clearly the A/D's must be synchronous with the front-end multiplexer. The two 12-bit data streams are packed into the high and low words of a 1K longword deep asynchronous fast FIFO, which buffers the on-card logic from the time structure of the events.

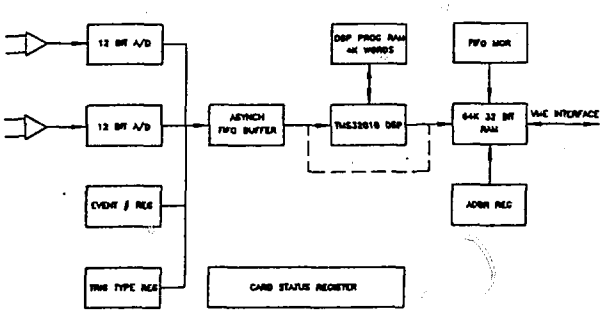

Fig. 2. A block diagram of the DAQ card.

Data from the fast FIFO can be processed by a TMS32010 DSP or written directly into Data Memory. Data Memory is organized as longwords (32 bits wide), 64K longwords deep, and can be configured either as a FIFO or as memory-mapped RAM. If the user chooses not to preprocess the digitized data with the DSP, the fast FIFO data will then be automatically written directly into Data Memory. If the user chooses to enable DSP processing, the BIO flag will be raised when data exists at the output of the fast FIFO, and the DSP can subsequently process the available data and then write the processed data into Data Memory.

Registers

The user configures the hardware and defines the operating conditions of the DAQ cards by writing a series of registers through VME. These writes may, of course, be done as global broadcasts. Each card has the following 16-bit registers which define and control the operating conditions:

- Control/Status Register (CSR)
- Address Register
- Trigger Type Register
- Event Number Register
- Word Count Register
- Global VME End of Event Register
- Max Word Count Table (16 Maximum Word Count Registers)

The CSR defines the specific logic configuration. The function of the particular bits of the CSR are given in Table 1. Notice that one of the bits of the CSR defines whether or not data will be processed by the DSP.

TABLE 1 - STATUS REGISTER (CSR) PARAMETERS

BIT	FUNCTION
SR0	VME/$\overline{\text{VME}}$
SR1	FIFO/$\overline{\text{FIFO}}$ (*)
SR2	DSP/$\overline{\text{DSP}}$ (**)
SR3	$\overline{\text{RST FIFO}}$ (*)
SR4	$\overline{\text{ADDR FROM VME}}$ (*)
SR5	$\overline{\text{RST FAST FIFO}}$
SR6	---
SR7	DAQ
SR8	AUTO TIMEOUT EEV
SR9	EVENT BOUND INIT
SR10	HEADER WRD
SR11	TRAILER WRD
SR12	AUTO WORDCOUNT EEV
SR13	DATA FIFO EMPTY INT MASK
SR14	DATA FIFO FULL INT MASK
SR15	FAST FIFO FULL INT MASK

* SR1=1 -> SR3=SR4=1

** Bit SR2 = 0 in order to do I/O with the DSP's 4K word memory.

Bit #	Operational Description
0	=1 VME has access to DAQ registers and/or Data Memory. VME can always access the CSR.
1	=1 Data Memory address is FIFO managed. SR3 and SR4 must =1 also. =0 Data Memory addressed via (a) VME(SR4=0) or (b) Address Register (SR4=1).
2	=1 Fast FIFO data will be presented to the DSP for processing. =0 Fast FIFO is placed directly in Data Memory

3	=0 FIFO Data Memory will be held in reset until this bit is set. =1 FIFO Data Memory can accumulate data.
4	=0 Data Memory address is specified by VME. =1 Data Memory address by (a) FIFO hardware (SR1=1), (b) Address Register (SR1=0).
5	=0 Fast FIFO will be held in reset until this bit is set. =1 Fast FIFO can accumulate events.
6	No definition.
7	=1 Enable DAQ card to take data.
8	=1 End Event if SERCLK times out (3 μsec).
9	=1 Begin Events on 256 longword boundaries.
10	=1 Enable Header words in data stream.
11	=1 Enable Trailer words in data stream.
12	=1 End Event if Word Count Register = Max Word Count Register.

The address of the CSR on each DAQ card is selected via on-board jumpers. Data Memory for this card also starts at this address, but is distinguished from the registers by requiring longword read/writes.

As a general rule, all registers may be written/read with word transfers from VME or may be written from VME with global word transfers. Table 2 shows the offsets of the registers and DSP memory.

TABLE 2 - REGISTER ADDRESS OFFSET

DESCRIPTION	ADDRESS OFFSET (HEX)
STATUS REGISTER	00000
ADDRESS REGISTER (VME <-> high byte)	00002
TRIGGER TYPE REGISTER	00004
EVENT NUMBER REGISTER (VME <-> lo byte)	00006
WORD COUNTER (VME <-> lo byte)	00008
GLOBAL VME EEV (solely a valid address)	0000A
MAX WORD COUNT TABLE (VME <-> lo byte)	00020 - 0003E
PAGE INCREMENT LOCATION (R/O)	00040
STATUS LINES REGISTER (R/O)	00042
DSP 4K MEMORY AREA	2000 - 03FFE

The CSR may be written/read from VME at any time, although this is not generally true of the other registers. A description of these registers is as follows:

1. **CSR**
   Each card has a 16-bit status register, the bits of which serve primarily to configure the hardware on the card. The function of the CSR bits is given in Table 1. The CSR can be accessed via VME at any time. This feature allows control of the events into the DAQ card.

2. **Address Register**
   When the Data Memory is configured as memory mapped RAM, the address register is used to provide an address to Data Memory. The address register may be initialized from VME, however only the high byte can be read. Every VME WRITE to the Address Register resets the low byte to zero, and furthermore a READ of the Address Register only indicates at which page of memory the register is pointing. Each time the user does a VME READ or WRITE to any location in Data Memory, the Address Register is incremented, and any subsequent VME READ or WRITE to any location will access the next location of Data Memory.

   For example, if we want to write 100 words to the third page of a card with CSR address set to 180000, and then read the data back, we have the following prescription:

   - CSR bits set such that SR1=0, SR4=1
   - write Address Register=03FF
   - DMAwrite(loc=180000,longword,data,100 words)
   - write Address Register=03FF
   - DMAread (loc=180000,longword,data,100 words)

3. **Trigger Type Register**
   The Trigger Type Register receives the trigger word in a VME global broadcast to begin an event. Typically this trigger word resides in the Trigger Type Register throughout the event, and is written into the data stream in the header word. The first 4 bits of the trigger type may be used as the pointer to the respective entry in the Max Word Count Table, specifying the number of words in the event.

4. **Event Number Register**
   There is an Event Number Register which may be initialized from VME, and will subsequently be incremented on each event. Only the low byte can be written. The event number is typically included in the header word in the data stream.

5. **Word Count Register**
   The Word Count Register is cleared automatically at the beginning of an event, and is subsequently incremented as each data word is written to fast FIFO. The value of the Word Count Register is written in the trailer word. Only the low byte of this register can be written.

6. **Global VME End of Event "Register"**
   The event may be ended by a VME global broadcast to this location. There is no memory or register at this location.

7. **Max Word Count Table** (16 Maximum Word Count Registers)
   Each of the trigger types can have an entry into this table. If the actual word count for a specific trigger type reaches the limit specified by the entry in the table, then the event will end, if the CSR was set to so allow ending in this fashion.

8. **Status Lines Register**
   Table 3 shows the contents of the status lines register.

TABLE 3 - STATUS LINES REGISTER

BIT	STATUS INDICATION
0(lsb)	data FIFO full
1	data FIFO empty
2	data FIFO half full
3	data FIFO almost full
4	low-gain fast FIFO empty
5	high-gain fast FIFO empty
6	low-gain fast FIFO full
7(msb)	high-gain fast FIFO full

Higher order bits are not currently connected.

Memories and Internal Buses

The Data Memory is a block of fast CMOS static RAM. Depending on the value of the CSR this memory may be configured either as FIFO, 64K words deep by 32 bits wide, or as a 64K block of long word addressable RAM. This memory may be written/read from VME as a FIFO, with address supplied from the on-board address register, or addressed directly from VME. During data acquisition the data is written in long words into the Data Memory either from the fast asynchronous FIFO or from the DSP. Note that if in FIFO mode, Data Memory can only be read once after a WRITE cycle.

There is an 8 Kbyte memory for the DSP instruction storage and data, which is organized as 4K 16-bit words. This memory may be written/read from VME only while the DSP is held reset by the appropriate value of the CSR.

The DAQ card local data bus is connected to the VME data bus via four 74LS645-1's. These devices guarantee the VMEbus 48 ma current specs. These transceivers are enabled whenever the card is selected. A memory data bus connected to the Data Memory connects to the local data bus whenever the card is selected and a LONGWORD transfer is occurring. A DSP data bus connects the DSP and the fast FIFO's. Finally, there is a fast FIFO input data bus, which connects the fast FIFOs, the A/D converters, and the registers which are written into the fast FIFOs.

The address presented by the VME address bus is latched into the local address bus by the logic which says the card has been addressed. The memory address bus connects to the address lines on the Data Memory, as well as to either one of the local address bus, the address registers, or the FIFO manager address lines. There is also a DSP address bus which connects the DSP to the DSP memory.

Transfers With the VME Bus

The CSR may be written/read from VME at any time. If bit SR0 of the CSR is set, then VME can initiate data transfers with any of the on-board registers or memory. If VME initiates a longword transfer, the transfer takes place with the Data Memory. The Data Memory may have several different configurations during these transfers, however, depending upon the contents of the CSR.

Word transfers with VME take place only with the registers, DSP memory, or the Max Word Count Table.

Non-VME Transfers to Memory

Data which is written to on-board Data Memory may come either directly from the fast FIFO, or from the DSP, and will be written with Data Memory having a configuration defined by the CSR. Data coming through the fast asynchronous FIFO is in a long word format and is written directly into Data Memory. The DSP, however, has a 16-bit data bus, so it is necessary to parse the data words before they are input to the DSP, and concatenate them again when they are output prior to being written into Data Memory.

SEQUENCE OF OPERATION DURING DATA ACQUISITION

An event begins with a global broadcast to the Trigger Type Registers. There are a number of different types of events, such as calibration events, uranium events, data events, etc., and the logic allows for 16 different trigger types, each having a maximum number of data words in the stream defined in the respective entry of the Max Word Count Table. Immediately thereafter a header word is written to the fast asynchronous FIFO containing the contents of the Trigger Type Register, the event number, and digital input flag bits. The ADC data then follows in synch with SERCLK, and at the conclusion of the data stream, defined either by

(a) timeout (3 μsec),
(b) maximum word count reached, or
(c) a global broadcast to the Global VME End of Event Register,

a trailer word is written to the fast FIFO which includes digital input flag bits and the word count for the event. The data will ultimately be written into the on-card Data Memory for subsequent acquisition through VME. The bit structure of the header, data, and trailer words is given in Figure 3.

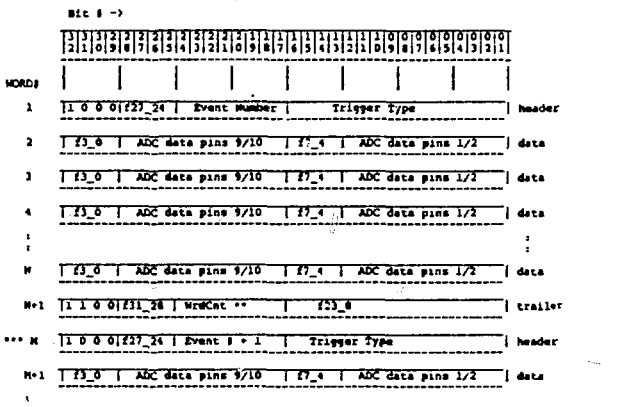

Fig. 3. Bit structure of data in DAQ card Data Memory.

Prior to the initiation of an event, the registers have been initialized. This may be done by global broadcast WRITEs to any registers which the processor in VME wishes to initialize. The Max Word Count Table may also be written with global broadcast WRITEs.

• An event BEGINs when a trigger is generated in the analog front-end electronics. A trigger word is strobed to an auxiliary master in the VME environment which immediately takes the VME bus using prioritized arbitration. The auxiliary master writes a global broadcast to all DAQ card Trigger Type Registers initializing the trigger word. The event is now live and each DAQ card responds by writing a header word to the fast asynchronous FIFO buffer. The header word typically includes the trigger word, event number, and flag bits.

A 1 MHz clock is generated in the front-end electronics and is distributed to all DAQ cards by VME (SERCLK). The A/D's hold and digitize on clock edges. Data words are written to the fast asynchronous FIFO buffer in a stream as they are clocked out of the A/D's. The data stream is 32 bits wide, the lower 12 bits of each word is the data from one A/D. The event continues in this way until it is ended.

Event END may occur in one of three ways as indicated above. VME can end the event with a global broadcast. Two other methods by which the event may be ended can be defined by the CSR. If desired, when the number of data words in the Max Word Count Table (corresponding to the respective trigger type word) is reached, the event will automatically end. Also, if desired, the event will end automatically if after the Trigger Type Register is written to, 3 μsec elapse and no SERCLK is seen. When the event ends, a trailer word will be written into the fast asynchronous FIFO buffer, including such information as tag bits, word count for the event, etc.

Data written into the fast asynchronous FIFO buffer will be written in FIFO/RAM or be available for input to the DSP depending on the value of the CSR. If the card is configured to have a DSP, the $\overline{\text{BIO}}$ flag will be raised allowing the DSP to acquire the data with IN instructions. The DSP can write to Data Memory with OUT instructions, but it has no ability to alter the memory configuration.

At the conclusion of an event, the system may be reinitialized via global broadcast WRITEs for the next event. This is not really necessary, however, if the default values are acceptable.

Ultimately, at some point the 68020 CPU may begin data transfer from Data Memory of the DAQ cards to the host computer through an acceptable interface such as DR11W link or a CAMAC interface[5].

PRODUCTION OF THE DAQ CARDS

At the conclusion of the circuit design and simulation phase, the CAD work for this card was done on the TELESIS system at Argonne National Laboratory. The card was laid out on a 220 mm 6U VME format, observing the VME layout specifications as closely as possible. The design rules included a 12-mil linewidth and 8-mil vias. Routing the card required 10 layers. Figure 4 shows the completed DAQ card.

A prototype production run of six of the DAQ cards was made using standard surface mount placing procedures and vapor phase soldering of the cards. A set of diagnostic software employing very comprehensive procedures had been written for testing the cards, and was used to assure that the cards were functioning properly. These cards were then run in a test beam at CERN in conjunction with a prototype FCAL module. Data were taken for electrons, with a resulting calorimeter resolution in line with calculations. At the conclusion of the test beam running at CERN, the cards were brought back to Argonne to instrument the cosmic ray test stand currently under construction. Some minor problems which had been seen in the cards were corrected, and a new prototype production run of 20 cards was started.

Four of the DAQ cards have been in constant use at Argonne for several months, monitoring phototube response, with no problems or component failures.

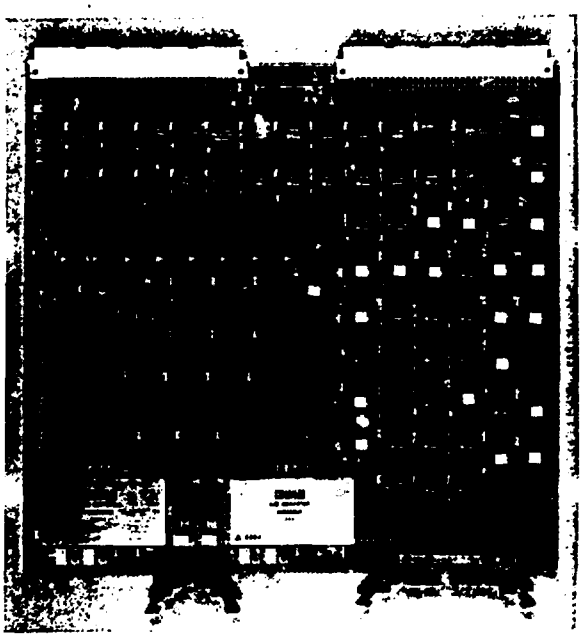

Fig. 4. Photo of the completed prototype DAQ card.

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