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Studies of the LBL CMOS Integrated Amplifier/Discriminator for Randomly Timed Inputs from Fixed Target Experiments*

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STUDIES OF THE LBL CMOS INTEGRATED AMPLIFIER/DISCRIMINATOR FOR RANDOMLY TIMED INPUTS FROM FIXED TARGET EXPERIMENTS

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A group at Lawrence Berkeley Laboratory has reported an elegant CMOS VLSI circuit for amplifying, discriminating, and encoding the signals from highly-segmented charge output devices, e.g., silicon strip detectors or pad readout structures in gaseous detectors.[7] The design exploits switched capacitor circuits and the well-known time structure of data acquisition in colliding beam accelerators to cancel leakage effects and switching noise. For random inputs, these methods are not directly applicable. However, the high speed of the reset switches makes possible a mode of operation for fixed target experiments that uses fast resets to erase unwanted data from random triggers. Data acquisition in this mode has been performed. Details of operation and measurements of noise and rate capability will be presented.

I. Introduction

The introduction of silicon strip detectors to the repertoire of high energy physics instrumentation has had a revolutionary effect on the kinds of experiments now considered routine.[1] The small feature size possible on silicon strip detectors makes possible compact detectors with superb spatial and consequently angular resolution. Detectors with 20 um pitch are now available commercially, and some detectors of 10 um pitch are being tested.[2] Charge is liberated due to ionization from the incoming particle's electric field in a statistical process. This gives a skew distribution, with a sharp low charge cutoff and a long high charge tail. Figure 1 shows the charge deposited in a 300 um silicon detector by one, two, three, or four minimum ionizing particles produced by 10 GeV/c pions in a thin target.[3] Typically, one has around 3.8 fC, or 24000

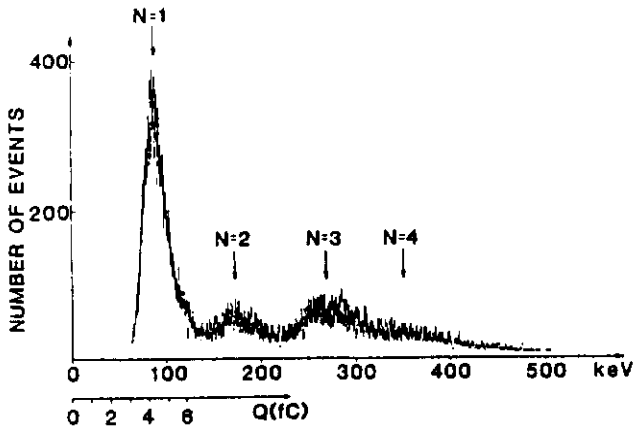

Figure 1. Charge distribution for 1, 2, 3, or 4 minimum ionizing particles traversing a 300 um thick silicon diode detector. For N=1, the peak charge corresponds to 4 fc.

electrons. As seen from figure 1, the minimum charge is approximately 3 fC. If a particle hits the detector at the boundary between adjacent readout strips, this charge is shared proportional to the mutual capacitance (or in some special cases to the resistance of an external line of amorphous silicon [4]). Thus, one must set a charge threshold of 1.5 fC or less to operate with nearly 100% detection efficiency.

In present silicon strip detector systems, the readout cycle is externally controlled. Each channel is checked either for a digital response (fast scan) or for a charge signal above the noise pedestal level for that channel. The latter mode is slower, but it allows one to interpolate the charge centroid on adjacent strips to improve the position accuracy of the tracking. [5] In either case the experiment design is complicated by the need to provide costly low-noise preamplifiers and subsequent analog circuitry for each readout channel. In these systems the readout speed is limited by the information transfer between the silicon strip detector preamplifier and the outside system. For systems requiring fast detector operating rates, analog storage techniques like delay lines can be used. In those cases, the data acquisition system must synchronize the analog data stream with the event selection logic from external sources. Present techniques are pushing toward operation at input fluxes of 50 MHz.[6] The fraction of active channels which have data on any given event is normally small, perhaps several hundred out of a 10,000 channel system. Assigning an expensive analog readout system to a predominantly empty set of channels is not a cost-effective approach to system design.

It is attractive to apply the cost reduction possible with VLSI techniques to this problem, combining the analog front end amplifier with sparse data scanning. This requires an internal editing method to suppress readout channels in which the charge input does not exceed a preset threshold. A CMOS 128-channel circuit with these features was reported at this meeting last year. [7] The aim of the original circuit design was to produce a high quality preamplifier/amplifier/discriminator/sparsifier system compatible with industrial CMOS fabrication methods. This will lower the cost per channel to very modest levels and allow the design of systems with 100,000 or more readout channels - a trend indicated by modern 4(pi) spectrometers like the Colliding Detector Facility (CDF) at Fermilab, for which this specific design effort was initiated. In present collider operation the beams are bunched, so that interactions can occur for only a short interval, separated by a much longer inter-bunch gap. In these applications one has a well defined time at which the system must be "armed", ready to accept a possible event. This timing sequence permits synchronization of steps in the calibration and readout cycle which is very advantageous for cancellation of offsets generated by detector leakage currents. Also, the relatively slow repetition rate means that bandwidth limiting can be employed for noise reduction. This application of the chip was discussed in ref. [7] and by S. Kleinfelder in his talk at these proceedings.

In fixed target experiments the time interval between successive events is random, and the incoming particle flux is high, 1-10 MHz. Such a situation demands a system in which information can be captured quickly and then rejected if subsequent logic indicates that

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the current event is of no interest. This paper studies the application of the VLSI chip designed for the CDF problem, hereafter referenced as "SVX chip", to the needs of the fixed target experimenters.

II. Fixed Target Operation

In fixed target mode one has a beam of incoming particles collimated to be essentially parallel and have small cross section. Some beam particles interact in a target. Trigger devices, e.g., scintillation counters, detect the incoming beam particles one by one, determine if they interact in the target (interaction probabilities range from 1% to 20% in typical experiments), and impose other selective criteria to decide if these interactions are "interesting". The rate of "interesting" interactions may be 1-30% of all interactions, or about .01-5 % of all beam particles. If one summarizes these characteristics from the system point of view, then one sees that fixed target applications demand the following features from the readout:

i) Good data rejection capability, e.g., fast clear features

ii) Operating stability for random intervals between valid inputs

iii) Fast readout times to reduce system deadtime. The experiment cannot proceed with data acquisition after any given event ofinterest until the information has been moved to some other storage device.

In order to see how the SVX characteristics feed into the experiments, consider a typical timing diagram in figure 2. Every beam particle drives charge into the

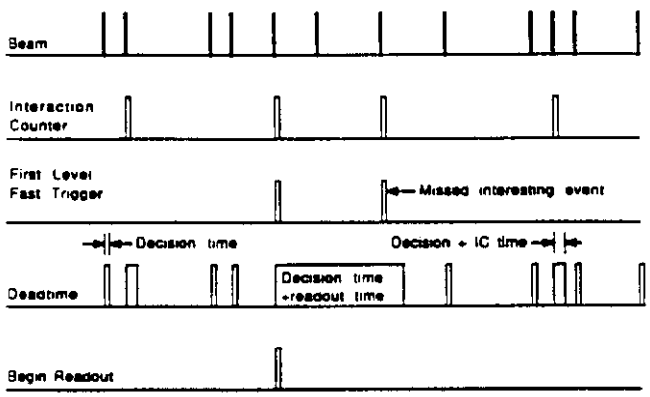

Figure 2. Typical trigger and timing considerations in fixed target experiments. Note that different deadtimes are required to respond to different trigger conditions.

amplifier channels connected to strips through which the particle passes. A RESET would be required to erase that charge, but that would be useful only if it were fast enough to avoid excessive deadtime losses. There are three different deadtime situations to be considered. First, there is the case where a beam particle is detected, but no interaction is detected. To maintain a proper record of experiment sensitivity, a PROMPT DEADTIME signal is generated after each beam particle shown on line 1 of figure 2 which prevents data accumulation during the decision time interval (~50 ns) plus a chip RESET interval. This deadtime should not be a large fraction of the mean time between beam pulses, or the experiment sensitivity will be severely degraded. Second, most experiments include provision to monitor the number of interactions in the target, as well as having additional trigger conditions to limit the overall data rate. These are indicated in lines 2 and 3 of figure 2. If an interaction occurs which does not satisfy the additional trigger logic, then one must RESET the readout devices to erase any hits, taking a longer DEADTIME (100ns+RESET time). The final situation to be noted occurs when a trigger indicates a readout should occur. After a valid interaction one must introduce a READOUT DEADTIME as shown on line 4 of figure 2, again putting a premium on fast readout cycles. In this case, a MASTER RESET pulse ends the readout segment and initializes the system for the next event. In evaluating the SVX chip, one must verify that the amplifier response is fast enough to meet the RESET demands and stable over the random interval between the end of the readout cycle and the next data.

III. Amplifier

The design philosophy of this device, called the "SVX chip" in subsequent references, is given in ref. [7]. A schematic is shown in figure 3. It consists of an

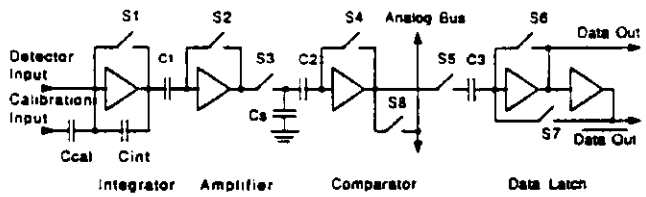

Figure 3. Simplified schematic diagram of the SVX analog section

input charge integrator with an externally controlled NMOS reset switch, a bandwidth-limited amplifier stage with reset switch, a threshold storage capacitor C2, and a sample and hold capacitor Cs for data storage.

It is instructive to look at the SVX clocking pattern in a collider system to understand device operations and architecture. Clocking patterns for fixed target use then become more evident. In a collider system a cycle is initiated by closing S1, S2, S3, and S4 to remove stored charge in the device. Next S1 is opened, followed by S2, storing the interstage voltage on C1. The front end is then ready to integrate and amplify charge. A threshold is imposed by injecting a known charge through Ccal and then opening S4, after allowing sufficient time for the amplifier output to rise. This sets the threshold voltage on C2. The amplifier is then quickly reset to discharge Cs and arm the system for data arrival. The data comes in at a well known time and is sampled by opening S3 after allowing an amplifier rise time interval similar to that used in the calibration step. The comparator buffers the difference between the voltages stored on Cs and C2. The data latch is set if this difference is positive, i.e., if Qin exceeds Qthresh.

This scheme has been loosely termed "quad correlated sampling", since S2 has been opened twice (sampling the interstage voltage on C1) and S3 and S4 have each been opened once, storing sampled voltages on Cs and C2, respectively. This method has the advantage of cancelling detector leakage current charges, since the threshold and input signal time windows integrate the same current for the same time interval. It also cancels the charge injected by opening S2 via the "correlation" of the sampling. The main contribution to noise in such a scheme is the variation in samples

on C1 due to integrator noise. The noise stored on C2 and Cs is smaller due to bandwidth limiting in the amplifier.

For fixed target applications a randomly timed input must be accepted. Periodic resets must be done to remove unwanted interactions and charge from leakage currents. These resets should be as short as possible in order to minimize deadtime. External logic in the experiment makes the decision whether an interesting interaction occured within a short time (50-100 ns) after the event. Thus, the interaction characteristics determine whether hit information should be stored on Cs. Leakage current effects can be eliminated by AC coupling the detector strips [8] or by ramping the calibration voltage if the leakage is sufficiently uniform for all strips feeding a given SVX chip (128 channels). If neither of these conditions is met, then the system must be reset often enough that the charge buildup due to leakage currents is not large compared to the threshold. If a constant calibration voltage can be used, it can be introduced during the MASTER RESET part of the cycle after a good event readout. If a ramped voltage is needed, it can be injected soon after the data signal arrives in response to external trigger logic so that it subtracts from the data.

With these considerations in mind, a fixed target pattern was generated to issue short reset pulses, which begin simultaneously, to switches S1, S2, and S4 while S3 remains closed. Durations of 100, 150 and 200 ns respectively were found to optimize the speed-performance product. Due to the slow response of the amplifier, a good event can be accepted any time after the opening of S2, even though S4 is still closed for a short time after S2 opens. After a good event occurs, the calibration voltage is injected to set the threshold and S3 is opened after the amplifier signal has risen. The SVX chip operates with a good signal/noise ratio under these conditions, but there are some problems with this pattern. If the integrator output is not completely settled when S2 is opened, there is an offset that appears as a signal at the output. Also, when S4 is opened so soon after opening S2, the voltage stored on C2 is not correlated to the voltage stored on Cs due to the slow amplifier risetime. Thus, charge injection is not cancelled.

Another fixed target pattern was developed which circumvents some of these problems. The integrator has a linear response for bipolar charge inputs of up to +/-200 fC. Hence, one can consider a scheme which resets only the amplifier section, while the integrator is reset periodically by the MASTER RESET. This pattern is shown in figure 4. To minimize deadtime, the fastest possible amplifier reset is desired. Since the amplifier bandwidth is proportional to its output capacitance, leaving S3 open will result in the fastest mode of operation, which allows amplifier resets on the order of 200ns. In fact, as shown in figure 4, S3 can be left open until the trigger logic indicates a VALID INTERACTION. Delays up to 200 ns cause no change in the output. At that time it is closed just long enough for the amplifier output to rise. A closure of 1us brings the amplifier output to 90% of its final value.

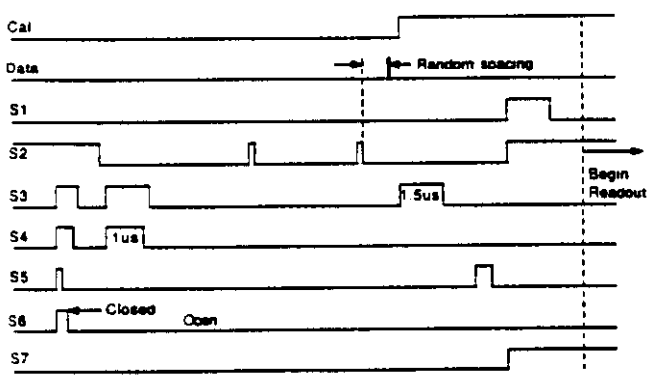

Figure 4. Switching pattern used for quad correlated sample operation with SVX chip in fixed target mode. For switch designations refer to figure 2.

The MASTER RESET, performed at specified intervals or after the completion of event readout, depending on experimental conditions, has the function of clearing the integrator and resetting the level on C2. In figure 4 the integrator reset is shown to occur just before readout, to allow maximum settling time. To cancel charge injection effects from S2, the amplifier output voltage is sampled on C2 about 1us after the amplifier reset is released.

The digital section of the SVX chip provides the editing functions needed to suppress empty channels and produce an ordered list of those channel addresses for which the input charge exceeded the threshold. Because this editing is on-chip, it sees very little capacitance and proceeds rapidly. The 128 channels are ready to begin readout within 1-2 us after an event, including amplifier risetime delays. The readout rate from on-chip storage to external data lines depends on the readout conditions. The chip will provide digital and analog information, if desired. For purely digital readout, the effective clock rate depends on the interval between successive hit channel numbers and ranges from 2-10 MHz. If analog information is also required, then the risetime of the signal on the analog bus limits the rate to about 2 MHz. Optional controls, available at system initialization time, permit the user to read out the left and right neighbors of strips whose charge exceeds threshold (a means to improve position resolution by interpolation). Also, one can force readout of all channels. This READ ALL mode is extremely useful in test and debug stages. Most of the work reported here was done in this mode.

IV. Test Conditions

As part of the evaluation program for the SVX chip the performance of the different stages of the analog section was measured on a probe station. The tests used a multichannel waveform generator connected to an IBM PC to drive the control lines. Data input signals were generated by a pair of HP 8082A pulse generators, driven from the multichannel board. This system gave

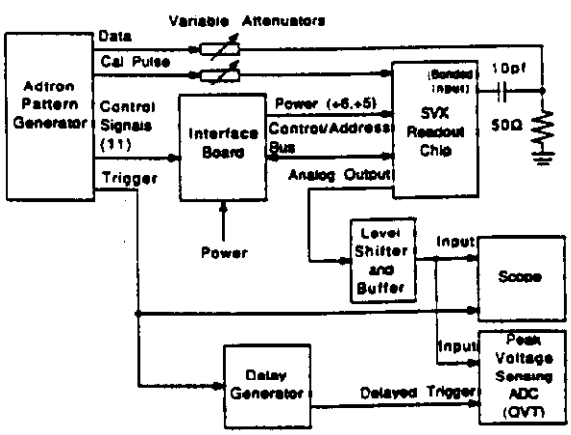

Figure 5. SVX readout chip test set-up

a very flexible control setup, with which any timing changes desired were readily implemented. A diagram is shown in figure 5.

Two different versions of the SVX chip have been studied. The B' version, an early development, has a higher bandwidth and hence more noise than the C'' version developed later. The latter version is aimed at production for CDF and is the focus of this work.

In order to simulate the fixed target conditions, the signal input was injected through a 10 pF input capacitor (surface mount) attached to a particular channel of the SVX chip. 10 pF is typical of the total input capacitance seen by a preamplifier bonded directly onto a detector wafer, so the noise environment of the test is a realistic simulation of the noise in a full system. The SVX analog stages are symmetric, so that bipolar inputs can be accepted. The signal input was positive, the calibration input negative. Amplifier linearity was studied over the range from 0 to 10 fC of input charge of each sign. No deviations could be seen at the 3% accuracy of the test measurements. For these measurements the chip was operated in the READ ALL mode, in which all channels were read regardless of threshold. Signals were fed to a LRS 3001 qVt voltage sensing ADC for measurement.

For the quad sampling pattern shown in figure 4 and discussed in section III, the test procedure was aimed at simulating the fixed target conditions of randomly timed valid and invalid inputs. Most readout channels in a system will not contain any charge, even in the case of an interaction. Some channels, however, will contain charge. Therefore, one must measure any shifts in response due to resetting channels with data relative to those without data. To simulate a typical event, a data pulse was injected on the data line 100ns before the reset pulse on S2. This data pulse was then removed to also study the clearing response of empty channels. Another test was done which studied the timing of the extra S2 resets relative to the MASTER RESET conditions (which correspond to the end of the previous readout cycle) and relative to the VALID DATA conditions (dark pulse on the DATA line in figure 5 and subsequent control pulses). S2 reset times relative to each of these conditions were varied over a range of 0 to 3 us. Excellent stability was observed with a reset pulse on S2 of 200 ns. No charge offset is needed from the CALIBRATE pulse to cancel an unwanted output offset. The variation of system performance for varying intervals between a RESET and the VALID DATA state corresponded to a charge fluctuation of less than 0.1 fC, independent of whether the channel was empty or held data. There was no dependence on how many RESET pulses were issued or their time separation. For interactions without a LEVEL 1 trigger (INVALID INTERACTIONS) the DEADTIME for reset operations is 300 ns, 100 ns of which is the trigger time delay necessary to form the LEVEL 1 trigger as indicated in figure 2. Most of the time there is a beam hit with no interaction. If the beam track charge is to be erased each time, then the deadtime is 250ns (50 ns due to the decision time and 200 ns for the reset).

Deadtime can be reduced by at least another 50 ns with very little penalty. Reducing the S2 reset time from 200 ns to 150 ns has no effect on the performance for time delays of up to 1.8 us between the end of a reset of INVALID data and the VALID DATA signal. For time intervals longer than that, one sees a charge buildup of order 0.3 fC/us with this 150 ns pulse length. This kind of effect is not seen for 200 ns resets. One should note that the times when one would push for a shorter reset pulse are precisely when the mean time between events is shorter, so that this onset of charge buildup is not likely to be a serious detriment. The SVX chip performs well for either 150 or 200 ns reset times for S2. The user should choose the duration to optimize his/her experimental performance. The signal/noise performance with this switching pattern is shown in figure 6, which shows the distribution of output pulse heights for input charges of 0, 1.5, 3.0, and 4.5 fC. Refer to fig. 1

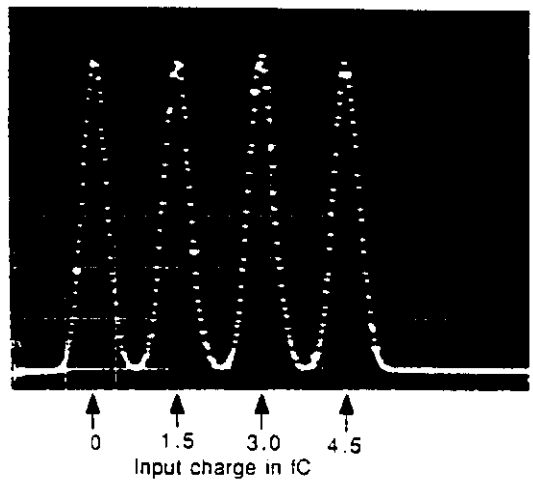

Figure 6. Pulse height distribution on analog output bus for input charge values Qin=0, 1.5, 3.0, and 4.5 fC. Here 0 fC input shows the noise associated with the electronics and the 10 pF input capacitance.

to see the fraction of the charge liberated by a single MIP that each test input represents. From the width of the peaks in figure 6 one can compute the noise in the system. For 10 pF input capacitance the noise seen here is 0.22 fC. Three input channels were checked, moving the same input network to each to minimize error. The gain was the same to within 4%, as one would hope for VLSI circuitry.

V. Conclusions

The electronic tests of the SVX chip in fixed target readout mode indicate that it is a high performance device well suited for many applications in fixed target experiments. In high-resolution silicon vertex detector systems with many readout channels it offers an extremely compact, cost effective way to implement the readout. The on-board sparse data editing feature permits a tremendous simplification in the cable requirements that currently present an enormous difficulty in vertex detector system design. The reset times required (150 ns after the VALID/INVALID trigger decision) are suitable for resets after every noninteracting beam particle in fluxes up to 1 MHz. For fluxes of several MHz, one can choose to reset after every Nth beam particle, with N set by leakage current or other considerations. The cost for doing this periodic reset is that some additional non-interacting beam tracks will be recorded in the SVX system, along with valid event data. Some external means must be provided to filter them out. Because the beam part of the system is usually a small fraction of the total cost, one might consider putting in a small number of additional detectors in the beam system and equipping them with high speed amplifiers of the type described in ref. 6. Because silicon detector efficiencies are generally above 99% for high momentum beam tracks, two or three planes implemented this way would tag the true beam track which initiates an interesting event, even though the SVX system might reset only after every Nth beam track. This would

reduce the system deadtime significantly, at little additional complexity in either hardware or analysis. This is the silicon detector analog of using proportional wire chambers to tag interesting tracks for precision reconstruction in drift chambers, which are slower but higher resolution devices. With this scheme one can expect to handle beam fluxes of several MHz with system deadtimes below 20%.

Further work is now underway to couple these readout chips to working silicon microstrip detectors for investigations in a particle beam.

VI. References

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