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THE ECLINE - DRIVER :
A FLEXIBLE, 20MHz, 256 WORDS ECLine GENERATOR.

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Abstract

The ECLine - Driver is a dual 256x16 - bits words fast ECLine generator fully controlled by CAMAC. Designed to fit requirements of High Energy Physics experiments, its flexibility makes it a general purpose unit.

It is used on the LEP - L3 experiment, at CERN, to implement two applications. In the first one, it generates the "trigger detector" response in order to exercize the different trigger processors under experimental conditions. In the second one, it generates some 10000 synchronisation signals required to drive the level - 1 energy trigger processor. 70 units are installed on the experiment.

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1. Introduction The FCLine bus [ref. 1] is largely used in High Energy Physics experiments. Its low cost, in view of its high speed transfer capability, makes it attractive. However, because of its one – way feature, debugging remains its weak point. To be safe, one has to inject known data on the bus at nominal speed; this can be done with a performant ECLine generator such as the ECLine – Driver

On the L3 experiment, the first level trigger processors are implemented in a CAMAC environment. They are connected to the trigger digitizers via the ECLine bus. In order to check the data transmission through the hardware, ECLine – Driver units are connected to the ECLine – bus between the digitizers and the trigger processors. "Ad – hoc" bit pattern blocks of 256x16 bits datawords, initially downloaded into the internal memory, are sent on the ECL – bus at 20 MHz.

In more refined tests, we check the detailed trigger decision on a set of simulated events. Simulated trigger data are written via CAMAC in ECLine – Driver memories. The total trigger information is splitted over 50 units. Simultaneous transfer on ECL bus, synchronized by front panel signals, reproduces the data taking conditions in its final environment, and allows thus to check the operation of each processor. The LEP experimental beam – crossing rate is reproduced by restarting the transfer of the same data block transfer each 22 microseconds.

In a different application, ECLine – Driver units are integrated in the L3 level – 1 energy trigger [ref. 2] in order to generate its overall clocking sequence. They allow to synchronize any number of channels with a very precise time definition. In the L3 energy trigger, some 10000 strobe signals are synchronized within 1 nanosecond every 22 microseconds. In this application, each bit of each word corresponds to one synchronization signal. So, each unit drives up to 32 clock sequences, each sequence being limited to 256 steps. Synchonization sequences are coded step by step into 2x 16 – bits datawords and downloaded into the internal memories. Perfectly synchronous reshaped signals are delivered at the output bus, and used to clock the fast trigger logic which makes the level – 1 energy trigger decision.

2. Principle of operation A very simplified block diagram of the unit is displayed in Figure 1. The ECLine – Driver supplies two operation modes, respectively named **transparent mode** and **generator mode.**

In **transparent mode,** the 16 – bits differential ECL output is connected to the differential ECL input. Data are transmitted without any modification from input to output. It is the data taking mode of units dedicated to hardware tests.

In **generator mode,** the ECL – output is connected to the 256x16 – bits words memory which is read and written via CAMAC dataway. The data transfer from memory to the ECLine bus is controlled either synchronously or asynchronously by a sequencer. It produces either data and strobe signals (standard ECL mode) or reshaped signals (burstguard mode). Asynchronous transfer is controlled by external front panel signals (allowing variable transfer rate). Synchronous transfer is controlled by internal signals generated at a preselected transfer rate (4 possible values). The data block length, delivered on the ECLine bus is adjustable from 1 to 256 words. Perfectly clean and synchronized output signals are provided by selecting the gated mode, the signal width is then defined with straps on the printed board. This mode allows to clock fast trigger logics.

3. Circuit description. The ECLine – Driver is a double width standard CAMAC unit, providing two independant ECL channels (ports). Its synoptic is displayed in figure 2.
In both channels, the multiplexer selects the operation mode : **transparent** or **generator.**

In **transparent mode**, the ECL data (D0 to D15) and control (RQO – WSO and ADL) differential input signals are regenerated without any change and directly transmitted to the output port. No signal alteration is possible. This default mode is set by one of the next CAMAC functions: Z – C – F9 or F24.

The **generator mode**, activated by F26, connects each ECL output port to its internal memory. Both memories are controlled by the same address counter, and both data banks are transferred in parallel. This feature allows to drive a 32 bits ECL bus by storing half of the word in each 16 bits word of same rank in both memories. Data transfer is controlled by a sequencer which activates options according to the parameters memorized in the control registers namely : "start address register" – "synchronisation mode" – "data shaping" – "transfer frequency".

The "start address register" contents the address of the first data to transfer (0 to 255). The transfer stops after the word 255 has been transferred. At beginning of each transfer the start address is transmitted to the sequencer. It is activated either by front panel signal, or by F25 CAMAC function.

The "synchronisation mode register" defines the source of the synchronization signal delivered to the sequencer. In asynchronous mode it validates the external signal applied on the front panel NIM or ECL connector. In synchronous mode, the clock is internally generated according to the preselected value stored in the frequency register. The sequencer clock frequency is trimmable, in order to adjust transfer frequency from 10 Mhz to 20Mhz. If it is trimmed to 20Mhz, the four preselected transfer frequencies are 2.5, 5, 10 or 20MHz. The "transfer frequency register" contains the selected value.

The "data shaping register" controls the data shaping on both output ports. It acts only when the generator mode is activated. The "standard" option delivers ECL,ine standard data and strobe signals on the output port. The "burstguard" option delivers reshaped signals on the data output port. Delay and width of signals are selected by on – board straps with a precision better than 1 ns. No parasitic signal is generated during transient time. Output signals are clean enough to be directly used to synchronize a fast trigger logic.

Figure 3 displays a timing sequence of the ECL transfer. Output signals are displayed in both options :"standard" and "burstguard".

4. Unit Operation In **transparent** mode, the operation is trivial. In **generator** mode, the unit provides a lot of options, but the user has only to care about options and parameters used for its application. The operation is split into 2 main steps. In the first step, one writes data into the internal memory associated to each channel by CAMAC F16 function. In the second step, datawords are transferred onto the ECL bus according to option parameters stored into control registers, as previously described. Transfer has to be started by F25 or by front panel signal. When started, all CAMAC functions are inhibited up to the end of transfer.

If asynchronous transfer is selected, only the signals delivered on front panel connectors will clock the unit. If synchronous mode is selected, only the signals generated by the sequencer at preselected frequency will clock the unit. A further transfer requires a new start of transfer, i.e a clock excess cannot restart the transfer.

Read/write in the internal memory is allowed while the unit transfers data in transparent mode. This feature reduces the writing time overhead when generator and transparent mode are interleaved.

On each valid CAMAC function, the unit generates X and Q responses. Implemented functions are F0, F1, F9 (Z or C), F16, F17, F24, F25 and F26. F0 reads one 16 bits dataword at the address given by the address counter. F1 reads the address counter and some control registers. F9 or Z or C initializes the unit. F16 writes one 16 – bits dataword at the memory location addressed by the address

counter. F17 writes the control registers. F24 selects the transparent mode. F25 starts transfer on both channels. F26 selects generator mode.

The internal memory associated to each channel is selected via subaddress (A0/A1). During data transfer on the ECL bus, all CAMAC functions are inhibited (Q = 0) except F9.

5. Conclusion The FCLine Driver is a general purpose fast ECLine datawords generator designed to drive applications encountered in large High Energy Physics experiments. All parameters are controlled by computer via the CAMAC dataway. Its burstguarded output makes it a versatile and fast synchronous or asynchronous sequencer (256 steps of 32 bits). Characteristics of the output signals are tuned by the user depending on the application. It drives 32 bit words with a maximum transfer rate of 20 MHz.

The transparent/generator option allows its easy integration on any ECL bus. Activated on request, it allows "in situ" test of sophisticated ECLine fast processors. Up to 256 words can be delivered on each port, synchronously or asynchronously at the maximum rate of 1 word each 50 ns.

More than 70 units (140 ports), produced by SCAIME company [ref. 3], are now installed in the L3 experiment.

Acknowledgement We thank R.Morand for helpful discussions and critical reading of the manuscript.

References

[1] ECL = Emitter Coupled Logic *developped in High Energy Physics by LeCroy Corporation.*
[2] L3 level – 1 Energy Trigger – L3 note # 449 – October 1986.
[3] SCAIME *B.P 501, zone industrielle de Juvigny 74105 Annemasse Cedex (France).*

Figure Captions

Figure 1 Represents a simplified block diagram of the unit. The ECL output port is connected either to the ECL input port, either to its 256x16 – bits words internal memory.

Figure 2 Displays a synoptic scheme of the circuit.

Figure 3 Displays a timing sequence, as observed on the ECL output port in a 20Mhz transfer in both options respectively "standard" and "burstguard".

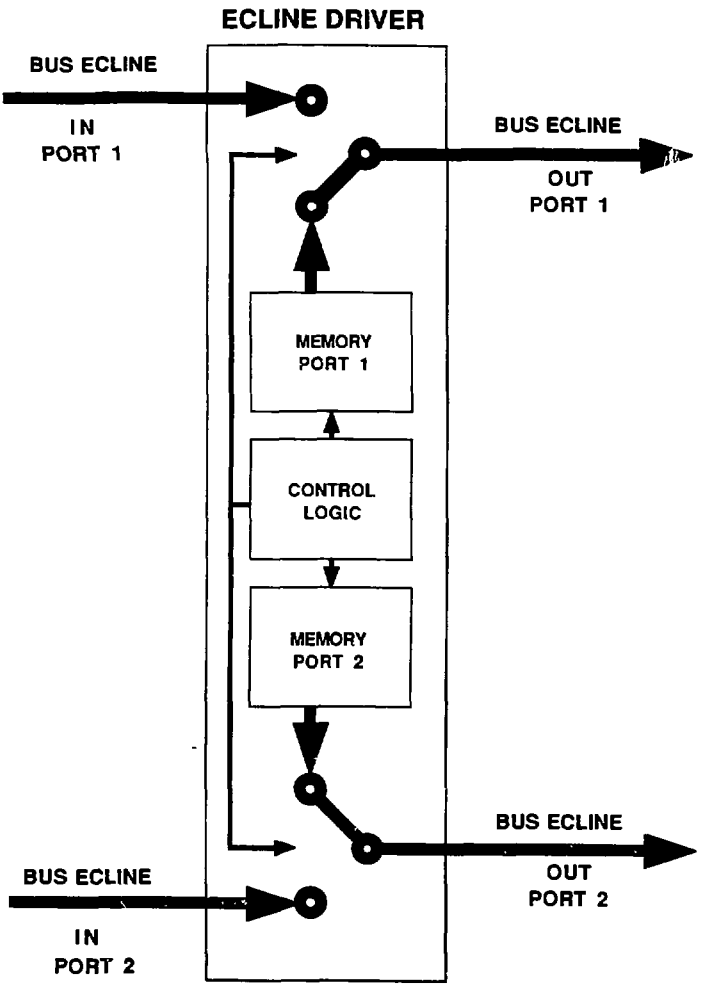
ECLINE DRIVER
BUS ECLINE
IN
PORT 1
BUS ECLINE
OUT
PORT 1
MEMORY
PORT 1
CONTROL
LOGIC
MEMORY
PORT 2
BUS ECLINE
OUT
PORT 2
BUS ECLINE
IN
PORT 2

Figure 1

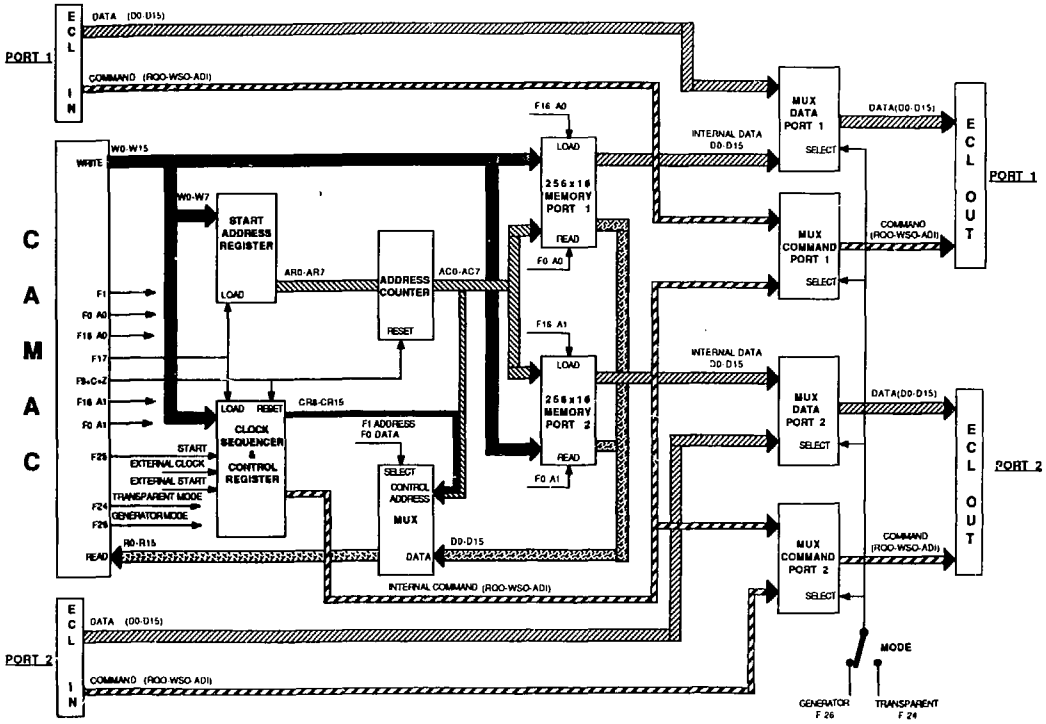
PORT 1
ECL IN
DATA (D0-D15)
COMMAND (R00-W50-AD1)
CAMAC
WRITE
W0-W15
W0-W7
START ADDRESS REGISTER
LOAD
AR0-AR7
ADDRESS COUNTER
AC0-AC7
RESET
F1
F0 A0
F16 A0
F17
F8-C+Z
F16 A1
F0 A1
F28
START
EXTERNAL CLOCK
EXTERNAL START
TRANSPARENT MODE
F24
GENERATOR MODE
F26
LOAD
RESET
CR8-CR15
CLOCK SEQUENCER & CONTROL REGISTER
F1 ADDRESS
F0 DATA
SELECT
CONTROL ADDRESS
MUX
DATA
D0-D15
R0-R15
READ
INTERNAL COMMAND (R00-W50-AD1)
F16 A0
LOAD
256x16 MEMORY PORT 1
READ
F0 A0
F16 A1
LOAD
256x16 MEMORY PORT 2
READ
F0 A1
INTERNAL DATA D0-D15
MUX DATA PORT 1
SELECT
MUX COMMAND PORT 1
SELECT
INTERNAL DATA D0-D15
MUX DATA PORT 2
SELECT
MUX COMMAND PORT 2
SELECT
DATA(D0-D15)
COMMAND (R00-W50-AD1)
ECL OUT
PORT 1
DATA(D0-D15)
COMMAND (R00-W50-AD1)
ECL OUT
PORT 2
PORT 2
ECL IN
DATA (D0-D15)
COMMAND (R00-W50-AD1)
MODE
GENERATOR F 26
TRANSPARENT F 24

Figure 2

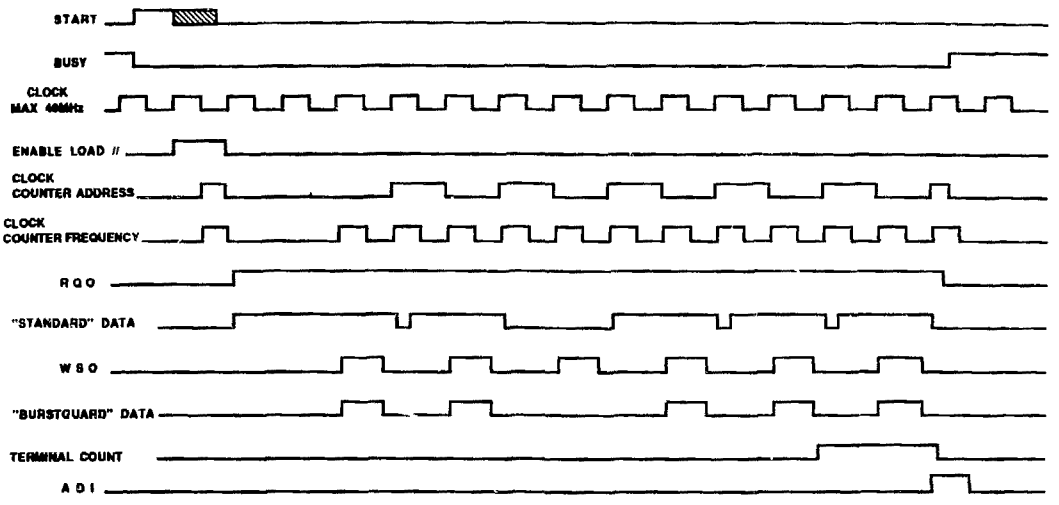
START
BUSY
CLOCK
MAX 40MHz
ENABLE LOAD //
CLOCK
COUNTER ADDRESS
CLOCK
COUNTER FREQUENCY
RQO
"STANDARD" DATA
WSO
"BURSTGUARD" DATA
TERMINAL COUNT
ADI

Figure 3