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ASIC Design at Fermilab

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ABSTRACT

In the past few years, ASIC (Application Specific Integrated Circuit) design has become important at Fermilab. The purpose of this paper is to present an overview of the in-house ASIC design activity which has taken place. This design effort has added much value to the high energy physics program and physics capability at Fermilab. The two approaches to ASIC development being pursued at Fermilab are examined by looking at some of the types of projects where ASICs are being used or contemplated. To help estimate the cost of future designs, a cost comparison is given to show the relative development and production expenses for these two ASIC approaches.

I. INTRODUCTION

There are several reasons for the increased use of in-house designed ASICs at Fermilab. First is the need for increased density in many of our designs. By combining more circuitry into a given package, fewer cards, crates, and associated hardware are needed to satisfy a given function. Also, in many cases, the circuits need to be reduced in mass as well as size since the circuits reside deep within a detector where secondary interactions with the electronics could corrupt measurements in outer layer detectors. A second reason is to achieve higher performance due to the reduced parasitic capacitance and inductance which are often limiting factors with discrete component designs. Finally, lower cost per channel can be achieved. However, cost savings is highly dependent on the quantity of chips or channels of electronics which need to be fabricated, due to the relatively high non-recurring engineering charges associated with ASIC design.

Of course, ASICs can be designed in-house or specified for design and fabrication by outside vendors. By doing the engineering design in-house, a closer relationship between the designer and user is maintained, resulting in (hopefully) a shorter design cycle and a product better tailored to the project's requirements. For these reasons, in-house ASIC design has become important at Fermilab. Only the in-house design work is discussed in the remainder of this paper.

Projects at Fermilab that use ASICs fall into two general categories. First, there are fixed target experiments in which interactions may occur as often as every 19 ns. These experiments are of general interest since the time between interaction is very close to the time between bunch crossings in detectors at the SSC. The second category is collider experiments. The collider experiments (CDF, D0, BCD) at Fermilab will all operate at a 400 ns crossing rate once the Fermilab III upgrades are complete. Fermilab designs for the SDC (Solenoidal Detector Collaboration) at the SSC must all operate at a 16 ns crossing rate.

Two different ASIC technologies are currently being used at Fermilab to assist with the physics program. One is a semicustom bipolar process which is characterized by NPN transistors with an fT = 6 GHz. These designs are all done using Tektronix Quickchip linear arrays. Designs using these arrays have been very effective for many Fermilab projects. The other technology is full custom CMOS with a 1.2 or 2.0 micron minimum feature size. Full custom design is generally used where high density, greater functionality, or low power is needed.

II. SEMICUSTOM BIPOLAR DESIGNS

Numerous bipolar designs have been completed using Tektronix Quickchip linear arrays. The arrays have two layers of metal available for routing. Precision laser trimmed nichrome resistors are

available if desired. As can be seen in the following table, bipolar designs have been completed for four different experiments at Fermilab. There are 3 different preamplifier designs, two different discriminator chips, and two chips which are a combination of logic and analog functions.

Device

Name	Function	Experiments
QPA02	Quad Preamp	E771,789, + others
QPA03	Quad Preamp	E665,771
VTX	Hex Preamp	CDF
IC01	Discriminator	E771
IC05	Discriminator	E771
IC02	Logic+analog	E771
IC04	Logic+analog	E771

Table 1 - Semicustom bipolar designs

Detailed descriptions are not given for the circuits described in this paper. Most of the circuits have been discussed at other conferences. What is described however, is the manner in which these ASIC circuits evolved.

A. QPA02

The QPA02 preamplifier is examined first because it helped to influence the design of several other chips.

Two experiments, E-771/789, needed preamplifiers for their silicon strip detectors. The preamplifiers were intended to provide single bucket resolution in a fixed target experiment with 19 ns between interactions. The preamplifiers needed to have low noise along with the high speed. Direct wire bonding of the preamplifiers to the detectors was not wanted for maintenance reasons.

A bipolar approach was decided upon to meet the speed requirement. Full custom design seemed unnecessarily expensive and time consuming. Therefore a semicustom bipolar design was selected due to the high probability of success and shorter design time. Tektronix was the vendor selected for the design.

The design which was implemented is a two stage amplifier called the QPA02. The first stage is a transimpedance amplifier and the second stage is a combined amplifier-shaper-line driver. The chip was

built using the Tektronix Quickchip 2S linear array. A key feature of the design was that it used trimmed nichrome resistors to correct for process variations and give uniform output response. The chip had high gain and differential outputs capable of directly driving long cables. There are four complete circuits on a 0.08" x 0.10" die. A schematic of one channel is shown in Figure 1. A few of the pertinent specifications are shown in Table 2.

Impulse gain	17 mv/fc
Crosstalk	<1%
Input noise	1600 e rms @ 20 pf
Risetime	6 ns
Falltime	12 ns
Power	42 mw/channel

Table 2 - Selected QPA02 specifications

Figure 2 shows the amplifier response to a small impulse of charge for different values of input capacitance.

Two QPA02 preamplifier chips were packaged in an inexpensive custom chip carrier as shown in Figure 3. These devices were encapsulated and mounted on a compact 128 channel preamplifier board as shown in Figure 4. Construction of a compact preamp board with 128 channels drove the packaging of the following comparator board. The logical design of the comparator board had 128 channels to match the preamp board. In order to fit 128 channels on a reasonable size (FASTBUS) board, much of the remaining circuitry was also implemented in ASICs.

B. IC01, IC02, IC04

The key circuit on the comparator board is the discriminator circuit. Each of the discriminator circuits has several special features. Each discriminator circuit must have 1) a provision for a separate threshold setting, 2) a transparent output latch, 3) a two channel analog summing circuit, 4) an analog buffer, and 5) low power dissipation. A great savings in space was realized by combining all these features into a single multichannel chip called IC01. In this case, the Tektronix Quickchip 2K-130 linear array was chosen for the layout. Figure 5 is a schematic for IC01. The analog sum circuit adds two signals from adjacent detector channels (to take into account charge sharing) and discriminates on that signal. Also, each individual detector channel is

routed to its own separate discriminator. A few of the specifications for IC01 are given in Table 3.

Differential input range	90 mv
Hysteresis	10 mv
Common mode input	+/- 1V
Differential output swing	710 mv
Propagation delay	5 ns
Crosstalk	1% max
Power	400 mw

Table 3 - Selected IC01 specifications

IC01 saved a great deal of space. However, the design of the discriminator board also required other high density circuits. A decision was made to split the remaining repetitive logic and analog functions into two semicustom chips called IC02 and IC04 which are shown in Figure 6. The logic shown also provides level shifting for the input signals coming from the discriminator chip. The quad analog sum circuit provides an analog sum of the signals from 8 adjacent detector channels while the NHit circuit provides a digital sum from 8 adjacent channels for trigger formation. IC01, 02, and 04 are mounted on the comparator board shown in Figure 7. (Also shown on Figure 7 is IC03, a multichannel D/A converter with A/D readback, that is used to set the discriminator thresholds. This chip was specified by Fermilab but designed by an outside vendor).

C. Wire Chamber Designs

The previous designs were all for a silicon detector readout system. Other designs quickly evolved from those designs to give circuits for readout from proportional wire chambers.

The first was a quad preamplifier chip called QPA03. This device is similar to QPA02 except for a few characteristics. The input impedance of the QPA03 is lower (90 ohms) and non-inductive. (The inductive component of the QPA02 input impedance made it unusable with a wire chamber.) The gain of the QPA03 can be trimmed to 10 or 20 mv/fc. The speed can be trimmed to as fast as 15 ns baseline to baseline.

Another chip is a discriminator chip called IC05 which is similar to IC01. For IC05, some of the features of IC01 were removed leaving only the four independent discriminators with independent thresholds and output latches. Thus IC05 may be a somewhat more general purpose device than IC01.

The interesting fact about these last two chip designs was that prototype runs were not made. The designs went directly into production showing confidence in the simulations and design review.

D. VTX

The latest device designed using a Tektronix bipolar array is a new preamplifier for the Fermilab Colliding Detector Facility VTPC upgrade. The new design is to replace the existing Fujitsu MB43458 four channel device. Four major changes were requested: 1) the preamplifier needed higher gain so that the wire chamber could run at a lower voltage, 2) the power had to be lower to reduce heating and improve dimensional stability of the detector, 3) the noise had to be lower, and 4) the mass of the packaged assembly had to be reduced to minimize secondary interactions with the electronics.

Based on the previous experience with Tektronix, the preamplifier was designed on a Quickchip 2S linear array. A performance comparison is given in Table 4.

	MB43458	VTX
Inpulse gain	0.3 mv/fc	1.0 mv/fc
Noise @ Cin		
= 25 pf	3400 e rms	1850 e rms
Power	25/mw channel	10 mw/channel
Mass (size)	1.0	<0.5
Risetime	----	6 ns
Falltime	----	15 ns
Channels	4	6

Table 4 - VTX performance comparison

As can be seen, all of the performance requests were met. As an additional advantage, six channels of the preamplifier instead of four were placed on a 2S die with a proportional reduction in cost per channel. The 6 channel VTX die is shown in Figure 8. To reduce the mass, the dice were direct bonded onto a thin substrate as shown in Figure 9. Coating has been placed over 2 of the dice to protect the wire bonds.

Although the design of this chip was quite different than previous designs, again no prototype devices were made. Over 16000 channels were made in the first production run. The devices worked exactly as expected based on the simulations.

E. Bipolar Summary

All of the devices described above have been produced in production quantities. The totals are summarized in Table 5.

Device	Type	Quantity	Channels
QPA02	Preamplifier	12060	48240
QPA03	Preamplifier	3809	15236
VTX	Preamplifier	2714	16284
IC01	Discriminator	11350	45400
IC02	Analog+Logic	4442	-----
IC04	Analog+Logic	5416	-----
IC05	Discriminator	3252	13008
	TOTAL	43043	

Table 5 - Production quantities of devices produced to date

As can be seen, thousands of devices and tens of thousands of channels of electronics have been made using the semicustom approach.

Semicustom chip design at Fermilab using the Tektronix linear arrays has been very successful. After the initial learning curve, some designs were completed and submitted directly to production indicating a relatively high confidence level at Fermilab in the design proceedure. The success of the semicustom chip design program is attributable to two main factors. One is the high quality of the component models that are provided by Tektronix and which result in accurate simulations. The other is the independent design review performed at Tektronix along with Fermilab personnel to detect errors and suggest layout improvements.

III. SEMICUSTOM BIPOLAR COSTS

Prototype and production costs depend somewhat on the linear array used and greatly on the quantity of chips produced. Approximate costs are given for reference.

A prototype run of one wafer costs $25K including the design review at Tektronix. For that price, the customer receives 25 packaged parts and the balance of the wafer as bare dice. If the design is good, the remaining parts can be also packaged at an additional cost. Production costs of a 4 inch wafer with 2S or 2K130 arrays decrease drastically with increasing quantity.

Wafer Quantity	Total Cost
3	$22500
4	24000
5	25500
6	27000
10	33000
50	93000

Table 6 - Semicustom wafer costs

The initial cost for each of the first wafers is about $7500 each. After the first three, the incremental cost for each additional wafer is only $1500. It is most cost effective to order all parts needed at the same time.

Packaging and testing are extra. For the Fermilab parts, the packaging cost was about $3/die and testing about $1/die. Approximately 900 good dice were received from each of the Quickchip 2S wafers and about 500 good dice from each of the Quickchip 2K-130 wafers.

IV. FULL CUSTOM CMOS DESIGNS

Semicustom circuit design has many merits but also limitations. One of the main limitations is that the circuit density is limited due to the fixed arrays of transistors, resistors and capacitors. Full custom CMOS and BiCMOS design overcomes this limitation and provides the maximum circuit density possible as well as many other advantages.

There are two main ongoing projects under development where full custom CMOS is needed. One is a research and development project to understand how to build the next generation of silicon strip detector high density readout chips. This effort involves designing test chips with various low noise preamplifiers to understand the problems and limitations of current processes. Also, designs of very sensitive analog circuits in close proximity to digital circuits have been completed to study the problem of noise from nonsynchronous operation of the analog and digital sections. Finally, multichannel low power A/D chips have been fabricated for simultaneous digitization of large numbers of analog signals. All of these circuits would ideally be combined into one chip design. The other effort is for the Solenoidal Detector Collaboration (SDC) Scintillating Tile Calorimeter. The SDC effort requires the development of a variety of ASICs which are suited to full custom design.

In the following sections, the SDC effort has been chosen as an example to show the types of circuits which are under development for a full custom process.

A. SDC Scintillating Tile Calorimeter Overview

The Scintillating Tile Calorimeter electronics system is basically a fast PMT (photomultiplier tube) readout system. Signals from each of 40000 PMTs are digitized every 16 ns and placed in a digital pipeline. Those signals are processed to locate and measure electron energy deposited in the PMTs in as few clock ticks as possible. The faster the electron can be located, the shorter the required digital pipeline. A very simplified signal flow diagram is shown in Figure 10.

Light signals are brought to the PMT through a light pipe from a scintillating material. Within the PMT base, the signal is digitized by means of a full custom ASIC and an FADC. That signal is transmitted over a medium length cable along with signals from 31 other PMTs to a card called the Electron Identification and Energy Measurement Board. There are 16 of these cards in a crate and 78 crates distributed over the detector. The EI&EM board has at least 5 different ASICs.

Name	Chip Quantity
1) Gated Integrator/ Digitizer	40000
2) Adder Tree	10000
3) Quad Adder	20000
4) 16 Tower Energy Sum	625
5) Calibration & Delay Chip	40000
6) Electron Sorter	5000

Table 7 - ASICs for the SDC Scintillating Tile Calorimeter

The total quantity and names of the ASICs required for the project are shown in Table 7. These quantities justify the large NRE costs associated with ASIC development.

The first ASIC listed is located within the PMT base. All of the remaining ASICs are located on the EI&EM board. Work is progress on ASICs 1 through 5.

B. Gated Integrator/ Digitizer

The first chip listed, the Gated Integrator/ Digitizer chip, is the key to the scintillating tile calorimeter readout system. This ASIC along with an FADC is placed in each PMT base to digitize the PMT output signal every 16 ns. The two chips are expected to provide 18 bits of dynamic range (1 fC to 1 nC) with 8 bits of accuracy. Eight bits of dynamic range are produced by the FADC and the remaining bits are produced by a 4 bit exponent which is generated by the ASIC. Thus, the output from the PMT is a 12 bit floating point number (8 bit mantissa , 4 bit exponent) which is pipelined through the remainder of the detector electronics.

Figure 11 shows a simplified diagram of the Gated Integrator/Digitizer chip. Due to the unusual nature of the chip, a brief discussion is warranted. In general the circuit toggles between two sets of 10 capacitors each RF bucket. During one 16 ns period, charge from a PMT is integrated on one set of capacitors, while the signals on the other set of capacitors from the previous time bin are being digitized. More specifically, the PMT current passes through a 10 bit binary weighted current splitter which feeds 10 different capacitors. At the same time, voltages stored on the other set of capacitors are feeding a set of comparators whose outputs are latched. Some fraction of the comparators are set, dependent on the amplitude of the input signal. That fraction of comparators is encoded by a 10 to 4 encoder to give a floating point exponent. At the same time, the set latches are examined to determine which capacitor signal should be routed through the analog multiplexer to the output for digitization by the FADC. Currently the FADC is thought to be off chip, but on chip possibilities are being examined.

Initial design work was completed on the binary weighted splitter using Tektronix bipolar devices. However, design of the other sections of the chip appeared better suited to a CMOS design. Since both bipolar and CMOS appeared desirable, the design focus was shifted to the Orbit 2 micron CMOS process which also has NPN bipolar devices. At the present time, a high frequency model of the NPN device has been developed and the design is proceeding. Other BiCMOS processes have also been examined.

C. Adder Tree

The second chip listed above, the Adder Tree chip, is the main building block for determining location of an electron and its energy within the calorimeter. All processing is done synchronously with beam crossing rate of 63 MHz. The Adder Tree ASIC adds digitized PMT signals (4 electron and 4 hadron signals) from 4

adjacent calorimeter towers and then performs two tests to determine if an electron has been found. If an electron is found, the electron energy is computed and sent to the trigger electronics. The signals which are being added are 12 bit floating point numbers (4 bit exponent + 8 bit mantissa). The additions take place in a tree like structure with each floating point addition taking 2 clock ticks of the 63 MHz clock. Figure 12 shows a simple functional diagram of the Adder Tree chip. It should be noted that each input and output line is a 12 bit floating point number, making this chip a high pin count device. A single adder circuit is represented by a circle with two floating point inputs and a single output.

A single adder circuit has been submitted for fabrication in a 1.2 CMOS micron process using custom cells. The layout is shown in Figure 13. The circuit dimensions of 1.7 x 1.7 mm indicates that 10 of these circuits as required by a complete Adder Tree chip will fit on a reasonable size chip. Simulations indicate that a single addition takes 2 clock ticks of less than 16 ns each.

D. Quad Adder and 16 Tower Sum

The quad adder is comprised of four single adder circuits as seen at the input to the Adder Tree circuit. Thus the Quad Adder is actually a subcircuit of the Adder Tree and could be the same device if the outputs of the Quad Adder portion were tri-stated to other pins.

In a similar manner, the 16 Tower Energy Sum circuit is a combination of three single adders as shown in the lower right hand portion of the Adder Tree. The output of the three adder circuits could be tri-stated to outputs rather than the compare circuits.

Thus, these two circuits are developed at the same time as the Adder Tree and may actually be implemented in the same device.

E. Calibration and Delay

The calibration and delay chip performs two main functions. First, there is a calibration Table or associative memory (12 x 4K) which corrects for nonuniformities in the Integrator/Digitizer chip. Second, there is a digital delay (12 X 128) portion which is necessary to store the digitized data while the trigger is being formed.

A delay test chip called SIRO has been fabricated in a 2 micron CMOS process. SIRO stands for serial

input and random output. Data is written to the device sequentially but can be read out in any order. A fixed delay is achieved by maintaining the read and write pointers at a fixed interval. A layout of the SIRO chip is shown in Figure 14.

Test results show that data can be written at 59 MHz, while readout is somewhat slower. This small discrepancy is understood and is easily corrected.

V. CMOS FOUNDRY COSTS

Two different foundry services are used at Fermilab to produce inexpensive prototype chips. The low cost is possible due to multiuser fabrication runs at the foundry. Interestingly, the costs for similar processes at the different vendors are quite different. Table 8 below compares a small and medium die size costs for MOSIS and Orbit in both 1.2 and 2.0 micron processes. It is clear that 2.0 micron prototype devices from MOSIS are cheaper while 1.2 micron devices from Orbit are less expensive. Although the quantities of dice provided by each vendor is different, usually 4 dice will suffice for prototype test chips.

Die Size	MOSIS		Orbit	
	1.2 u	2.0 u	1.2 u	2.0 u
2.4 x 2.4 mm	$6.3K	$550	$1.5K	$1.5K
	(50 die)	(4 die)	(12 die)	(12 die)
7.2 x 7.2 mm	$40.8K	$6.8K	$12K	$12K
	(50 die)	(24 die)	(24 die)	(24 die)

Table 8 - Prototype chip costs

Production costs previously given for the Tektronix process were based on 4 inch wafers. For comparison, costs are also given for a 4 inch CMOS wafer (1.2 micron). In a full custom process the NRE cost is higher since all of the masks instead of just 3 or 4 are need to fabricate the chips. Typical NRE costs are $3.5K for tape conversion and about $30K for masks.

A CMOS prototype run would include 5 wafers but only 25 packaged parts for $25K. Production runs usually begin at a quantity of 25 wafers or more. For 25 wafers, the cost is about $1500 per wafer and for 100

wafers the price may drop to $800 per wafer. Of course, packaging and testing are extra.

One can expect 900 good 2.4 x 2.4 mm dice from a 4 inch wafer. Surprisingly, this is essentially the same yield we received with the same size die (2S) from Tektronix production runs.

VI. SUMMARY

In-house ASIC design has become a significant tool for the high energy physics program at Fermilab. Currently, two different approaches are being pursued.

The first, and the one with which we have had the most experience, is semicustom bipolar design using Tektronix linear arrays. All of the designs have been very successful due in part to the well characterized models which are used and the design review performed by Tektronix. We have found that chip development time can be relatively short. And finally, the cost per channel is reasonable when the number of devices or channels approaches 10,000.

The other approach is full custom CMOS or BiCMOS, where maximum circuit density or low power dissipation is important. With these technologies, the device models are often not as well characterized, particularly for analog design. Small quantity prototyping usually costs less for CMOS devices due to multiuser wafer fabrication. However, the higher NRE costs for production makes the cost of small production runs usually higher than for semicustom designs. A small production run (4 wafers) with Tektronix arrays costs about $50K while the same size run in Full custom CMOS would cost about $65K.

The importance of these technologies, as well as others, can be expected to grow at Fermilab as the channel count for experiments continues to grow and speed and performance issues become more critical.

VII. ACKNOWLEDGEMENTS

VIII. REFERENCES

[1] D. Christian, et. al., "The Development of Two ASICs for a Fast Silicon Strip Detector Readout System", IEEE Transactions on Nuclear Science, vol. 36, pp. 507-511.

[2] T. Zimmerman, "A High speed, Low Noise ASIC Preamplifier for Silicon Strip Detectors," IEEE Transactions on Nuclear Science, vol. 37, no2, pp. 439-443, April 1990.

[3] R. Yarema, et. al., "A High Speed, High Gain Preamplifier System for Silicon Strip Detectors", IEEE Transactions on Nuclear Science, vol. 37, no. 2, pp. 430-433, April 1990.

[4] C. Swoboda, et. al. "A High Rate FASTBUS Silicon Strip Readout System", IEEE Transactions on Nuclear Science, vol. 37, no. 2, pp. 342-346.

[5] R. Yarema, et. al. "A High Performance Multichannel Preamplifier ASIC", To be presented at the 1991 Nuclear Science Symposium.
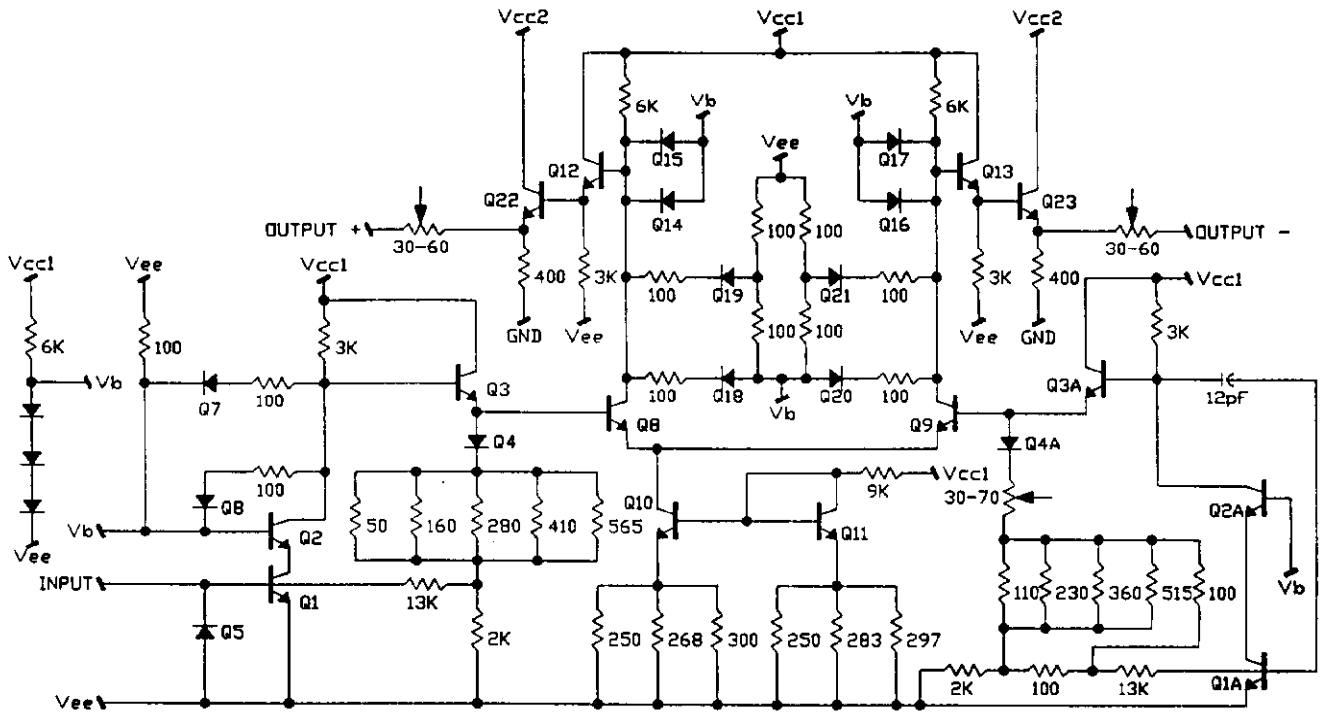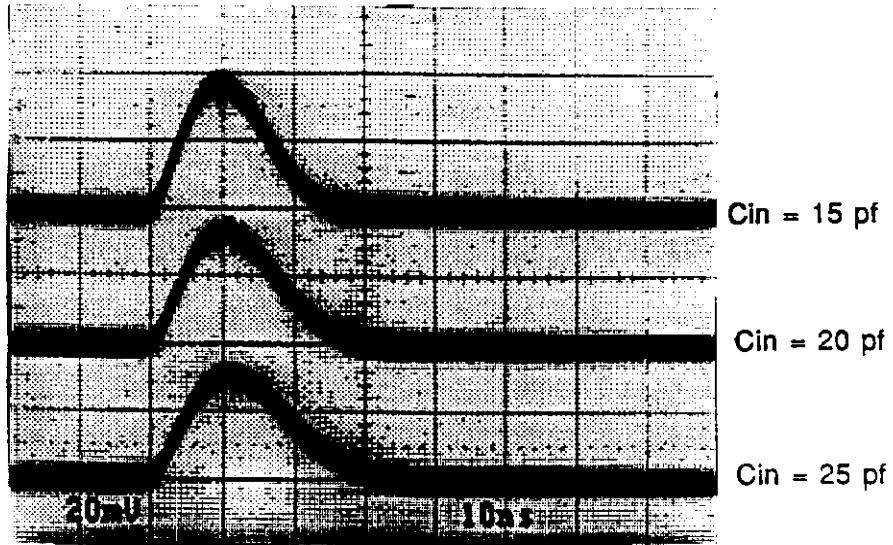
Figure 1 - QPA02 Schematic Diagram
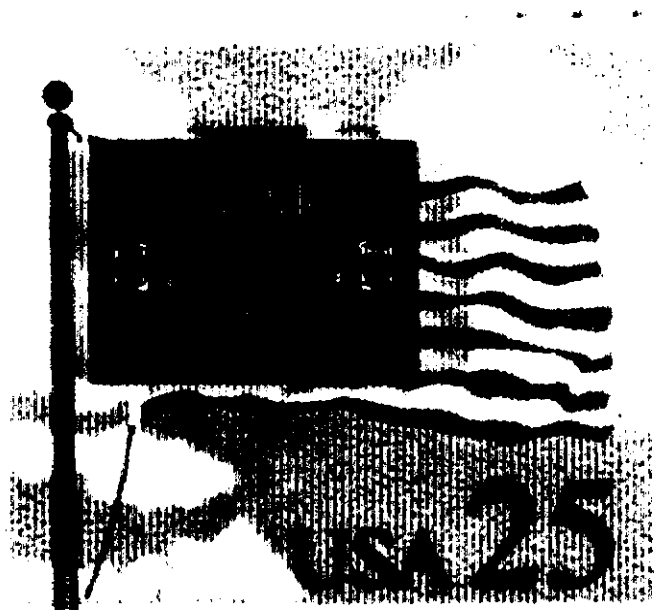
Figure 2 - QPA02 Impulse Response

Figure 3 - Two QPA02 Preamplifier Chips Attached in a
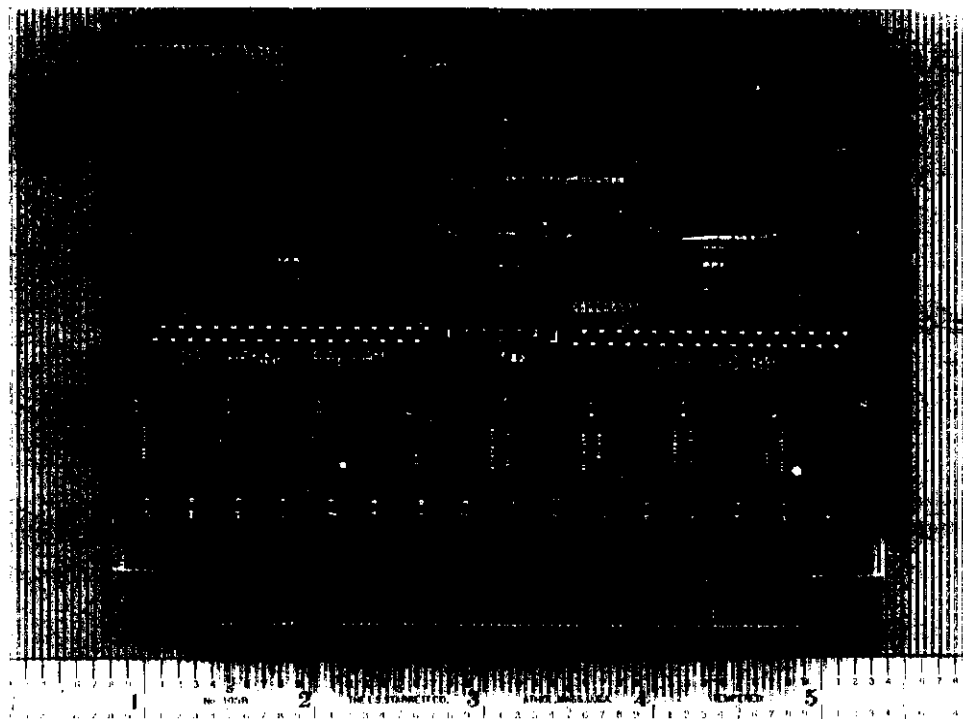Custom Chip Carrier to Form an 8 Channel Assembly

Figure 4 - 128 Channel Preamplifier Board for
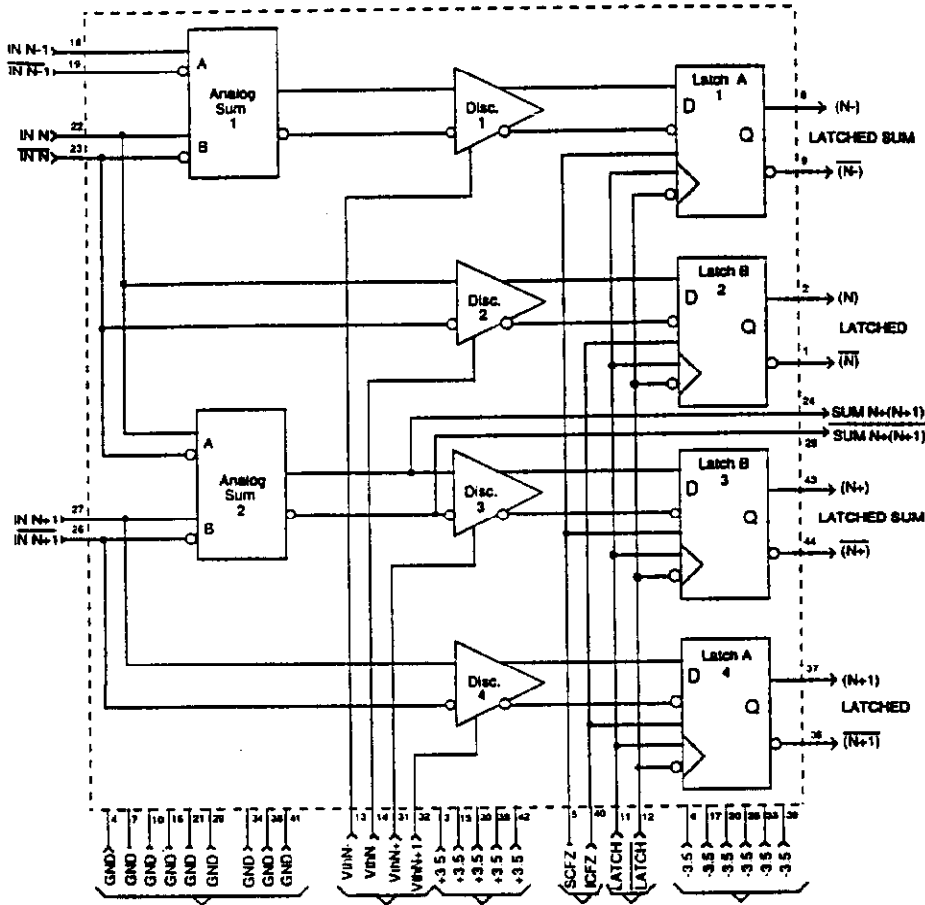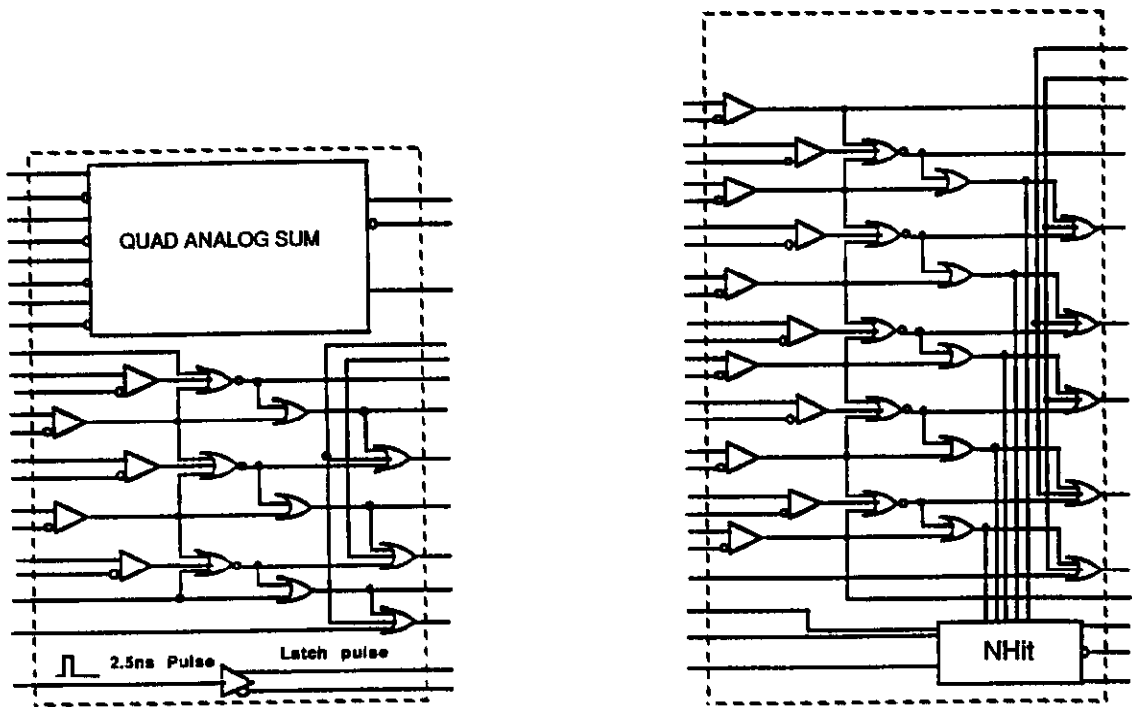Fast Readout of Silicon Strips

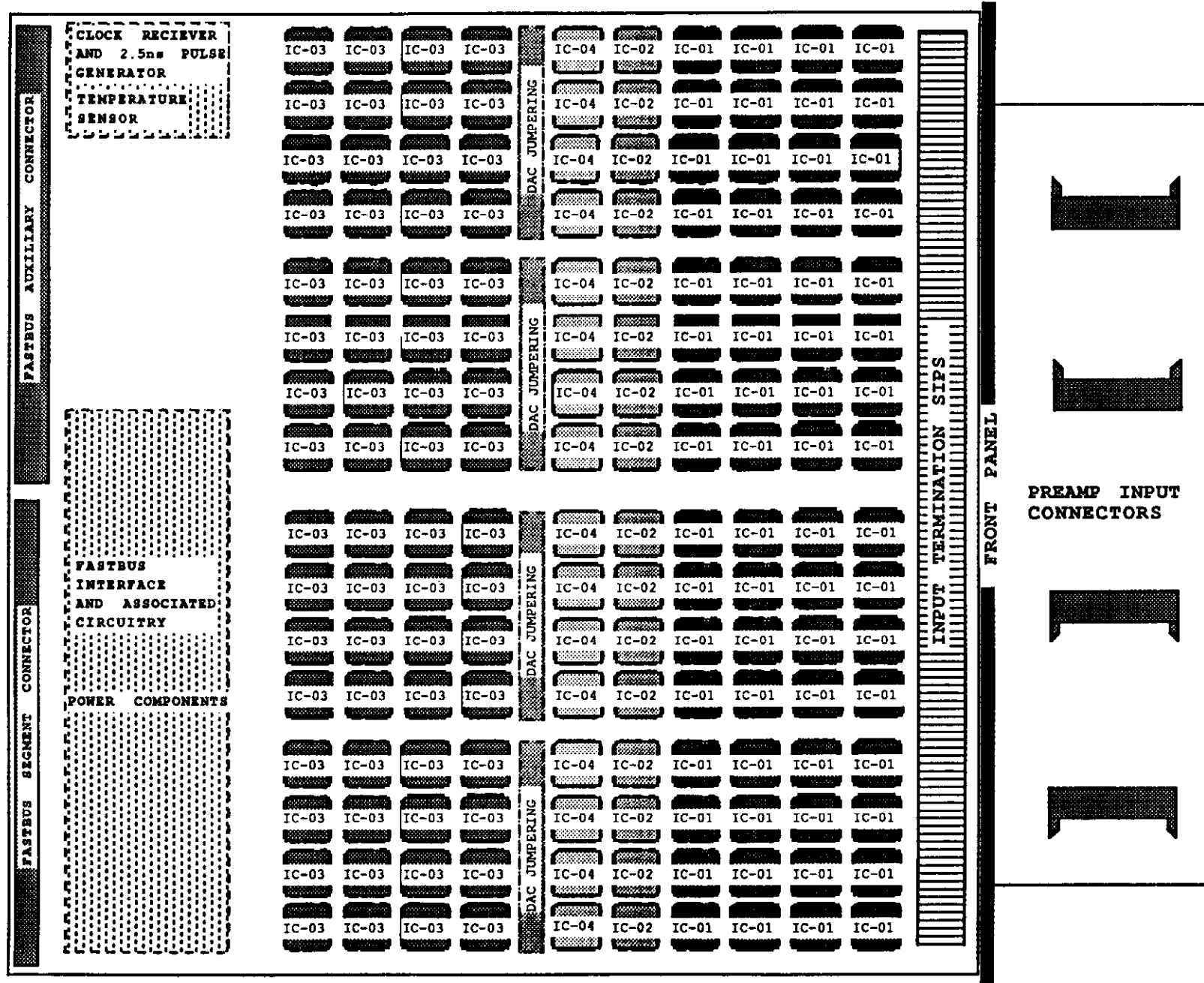Figure 5 - IC01, Multichannel Discriminator with Latch and Sum Circuits

IC-02: Three Channel Logic, Quad Analog Sum & Latch Driver

IC-04: Five Channel Logic and Octal NHIT

Figure 6 - IC02 and IC04, Combined Analog and Logic Circuits

Figure 7 - Custom Integrated Circuits on a FASTBUS (14" x 20") Board

FASTBUS POSTAMP/COMPARATOR MODULE
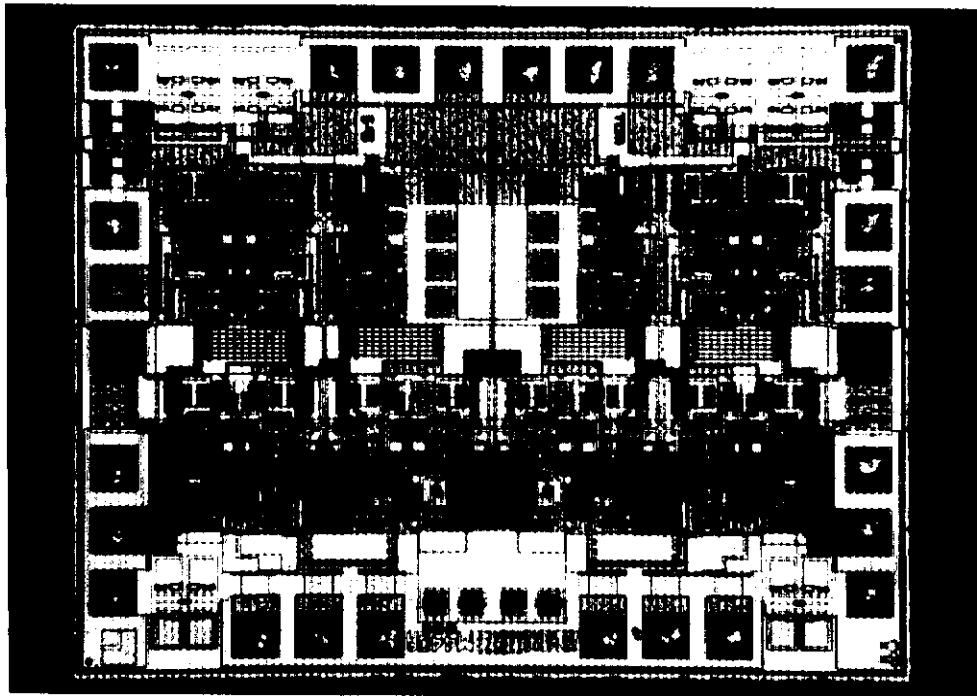
Figure 8 - Six Channel VTX Preamplifier on a Quickchip 2S Die (0.08" x 0.10")
Inputs at the Top, Outputs Along the Bottom
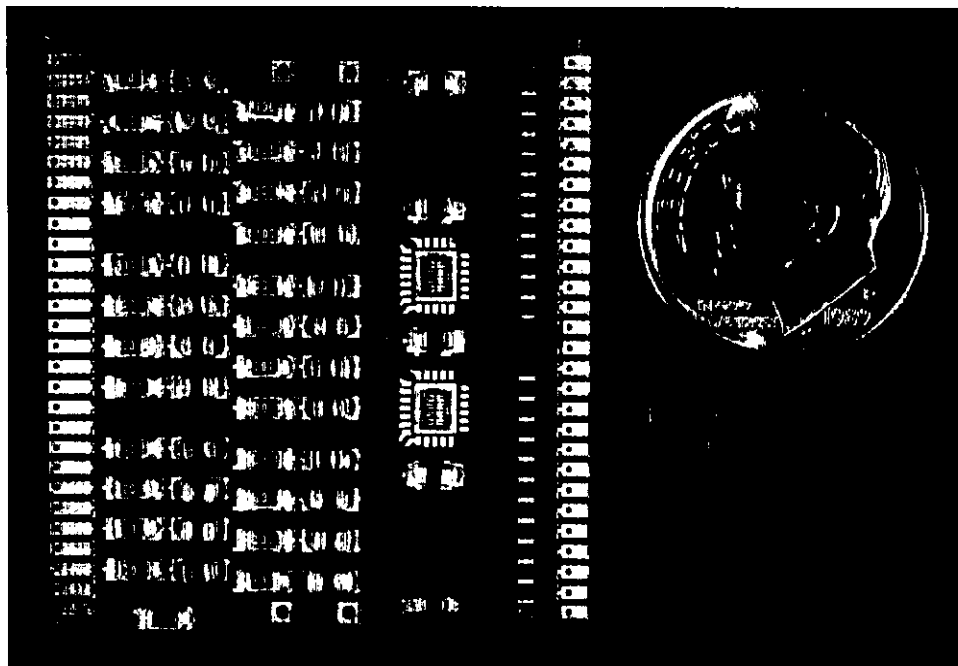
Figure 9 - 24 Channel Preamplifier Assembly Using VTX Chips With COB
(Chip On Board) Attachment. Two chips Are Coated to Protect Bonds.
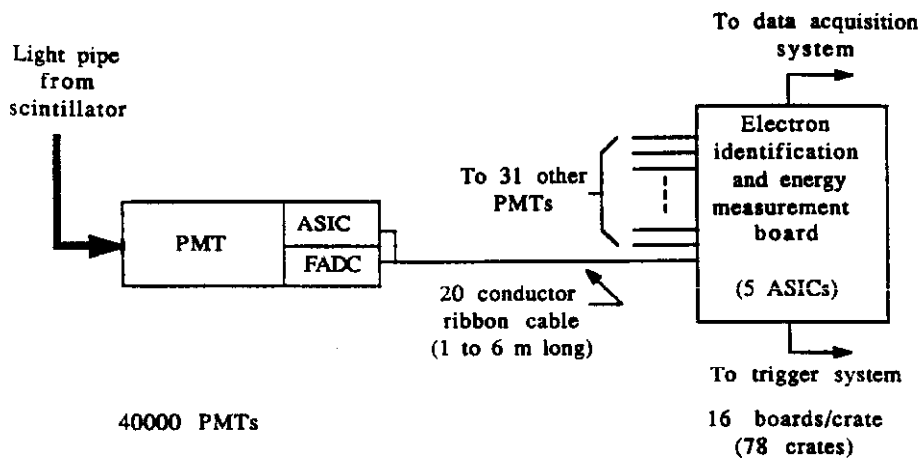
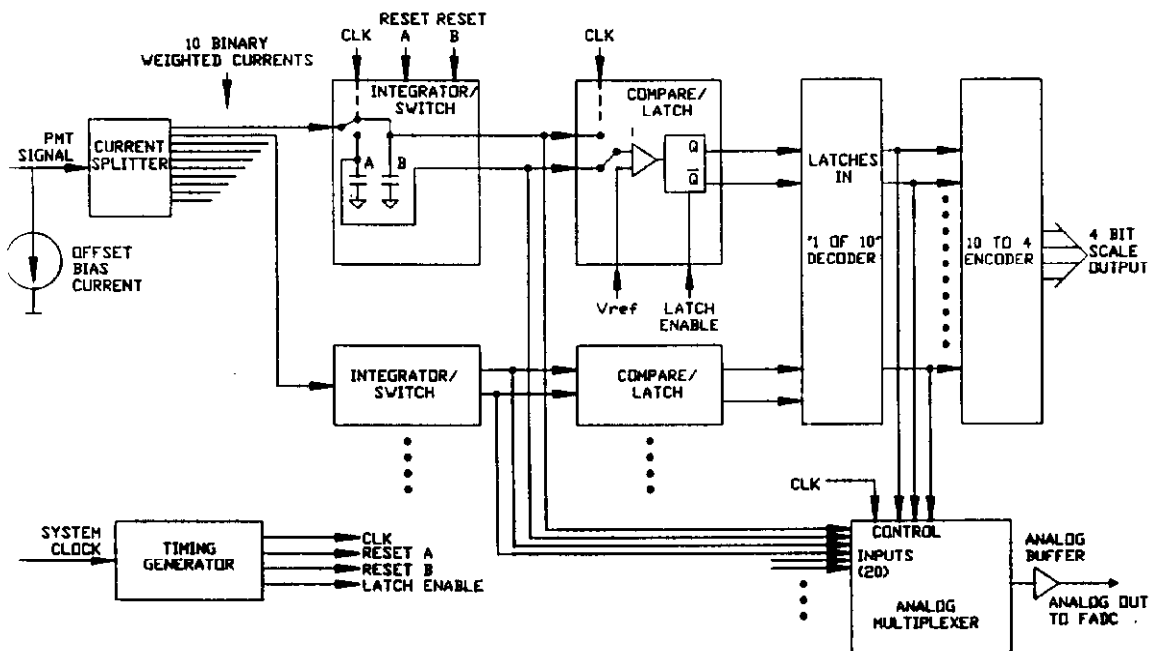**Figure 10 - Simplified SDC Scintillating Tile Calorimeter Signal Flow Diagram**

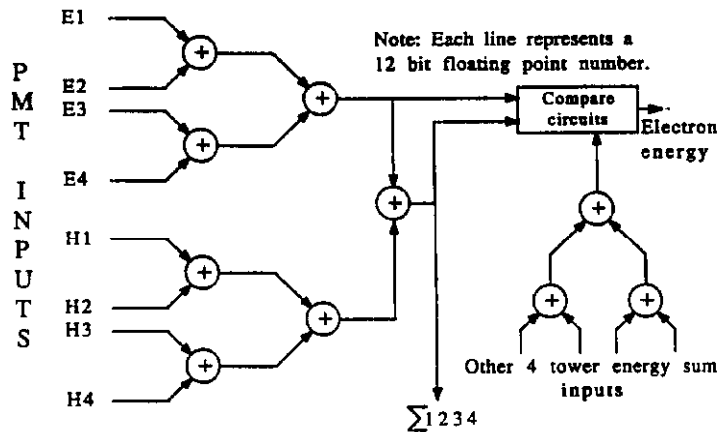**Figure 11 - Photomultiplier Tube Gated Integrator/Digitizer Block Diagram**

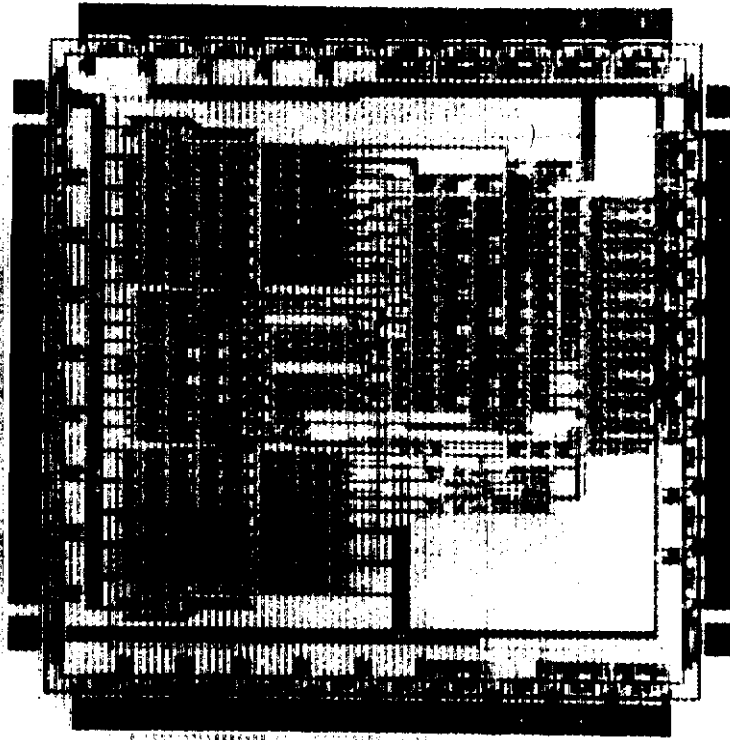**Figure 12 - Adder Tree Chip Functional Diagram**

Figure 13 - Fast Adder Layout for Two 12 Bit Floating Point Numbers.
Inputs on the Left, Outputs on the Right.
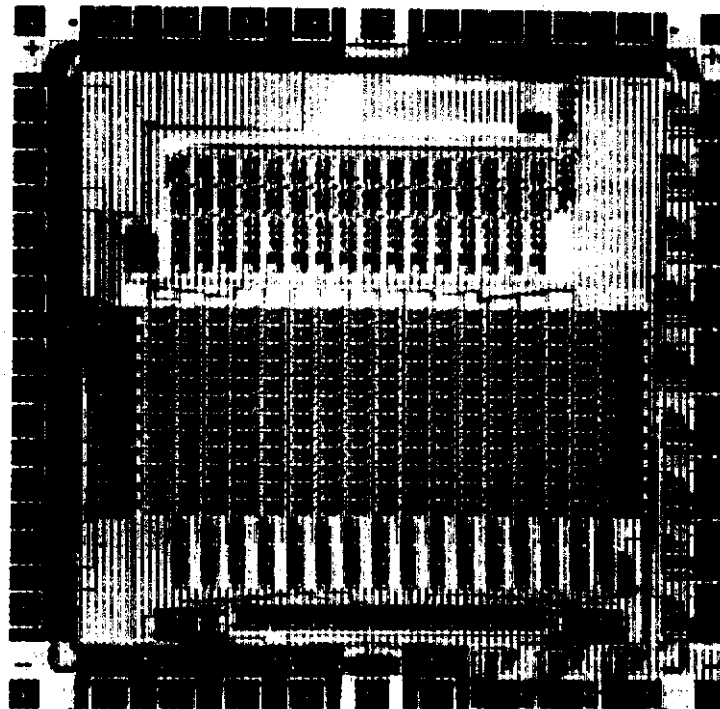(1.7 x 1.7 mm Active Chip Area)

Figure 14 - Serial Input Random Output (SIRO) Delay Chip Layout
(12 Inputs on the Left, Outputs on the Right)