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Gate-Keeper Module
for
TANSY-KM5

by
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The Gate-Keeper Module

Fig.1. The Gate-Keeper Module

The purpose of the Gate-Keeper is the control of the TDCs, the ADCs, and the constant fraction discriminator (Ortec 584). The Gate-Keeper synchronizes the units and ensures that the data taking is clean and not intermixed with other events. There are six Gate-Keepers in the system, one for each proton detector.

The Gate-Keeper has two modes of operation named Amp and Time, see figure 3, "Block Diagram", page 4. The Amp mode is designed for calibrations. Only the ADC is used during this mode. The ADC gate is then always open except at the time of inhibit signals from the linear amplifier.

The Time mode is used for normal measurements. The signal "CF DISCR POS" is branched into and triggers two monostable circuits, t1 and t2. The t1 time width is controlled by an internal potentiometer (P3 in figure 4, "Circuit Diagram for Board TANSY1", page 5). The output proceeds over an OR-gate to an output driver. The output is connected to the constant fraction gate input v ch locks it until the end of the event. The locking dur..g the time the TDC waits for data fetching is done by the TDC DATA READY signal. The TDC data are the last data fetched by the computer during an event fetching cycle. The TDC DATA READY signal is ORed to the t1 output signal. The t1 monostable covers the the time gap caused by the TDC conversion time. The deadtime of the constant fraction discriminator is normally shorter than the TDC conversion time.

The monostables t2 and t3 control the delay and the width of a gate signal for the ADC. The times are controlled by external potentiometers. t3 is only started if there is no pile-up, i.e. no inhibit signal from the linear amplifier. Therefore, a pile-up event will be recorded as an event with an undefined amplitude.

The mode control input has a switch which can be set to the three positions Amp, Time, and Ext. The Amp and the Time positions overrule the external input signal. The external signal used at the switch position Ext. sets the mode Amp if the signal is high and Time if the signal is low. It is coming from the the CTM1 module channel 1.

All input circuits are designed to accept TTL as well as negative NIM signals. However, during the test period negative NIM was used only at the TDC DATA READY input. Therefore, this input is optimized for NIM signals and the other ones for TTL signals. All inputs are high impedance inputs and must be terminated by external terminators. Connectors are provided for termination or by-passing of the signal.

The output is 50 ohm TTL or negative NIM as defined by internal jumpers.

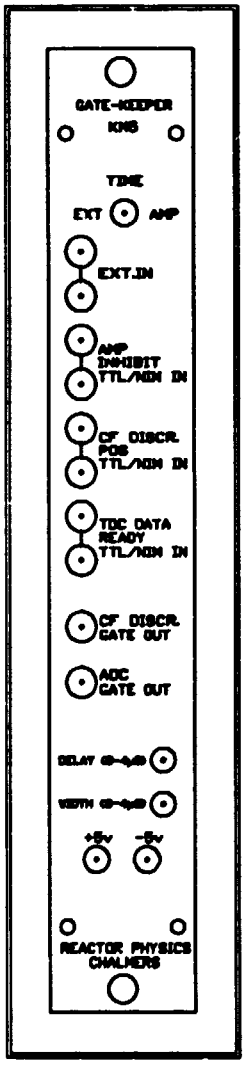

Fig.2. Gate-Keeper Front Panel

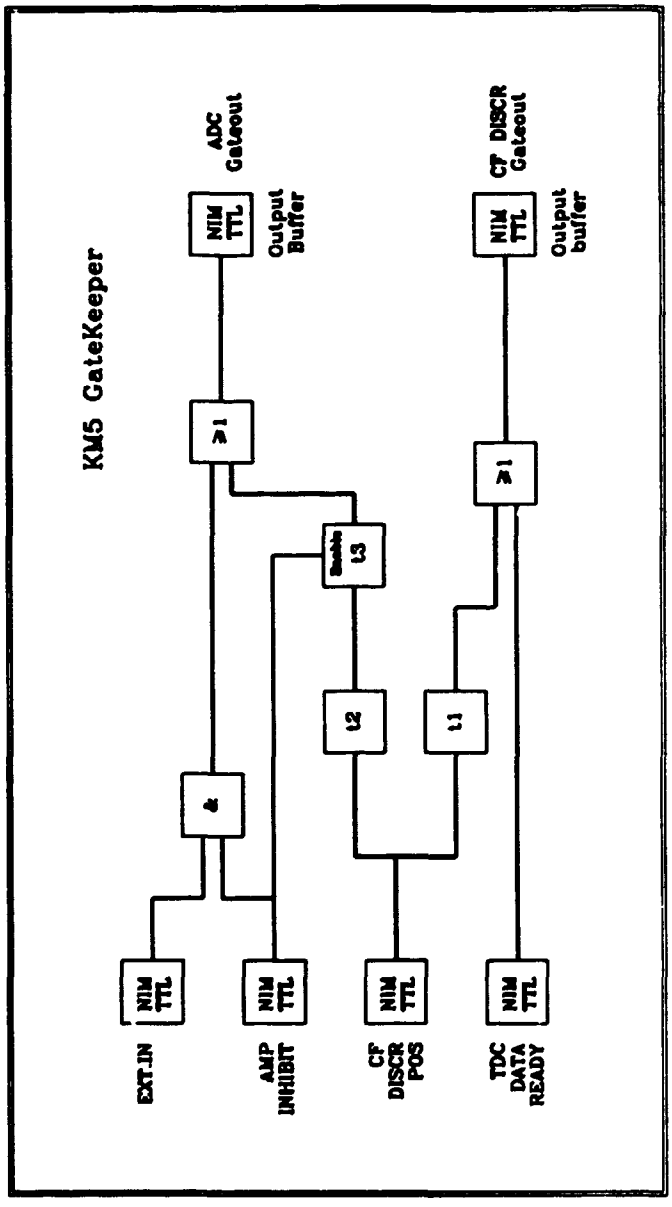

Fig.3. Block Diagram

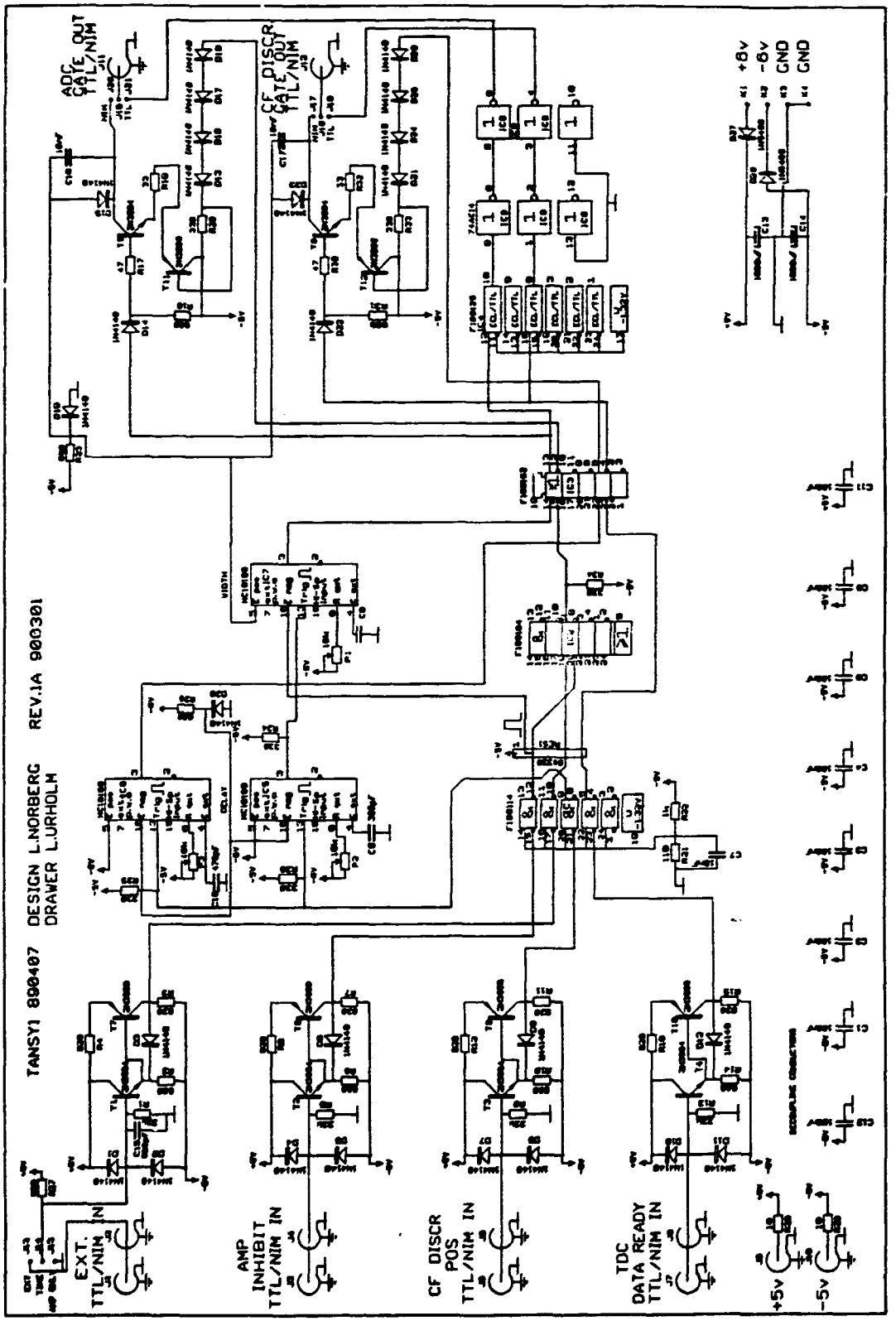

Fig.4. Circuit Diagram for Board TANSY1

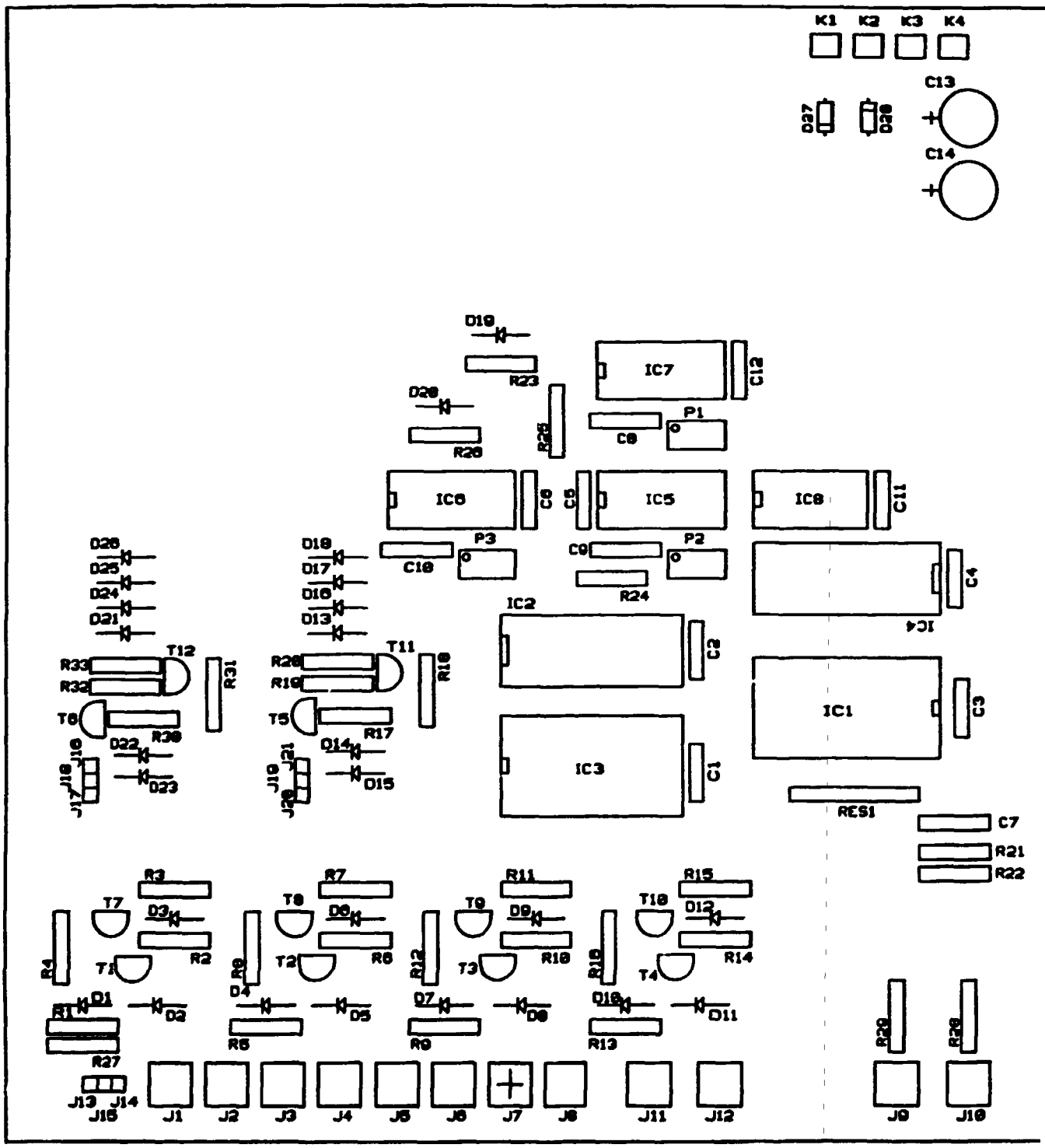

Fig.5. Component Layout at Board TANSY1

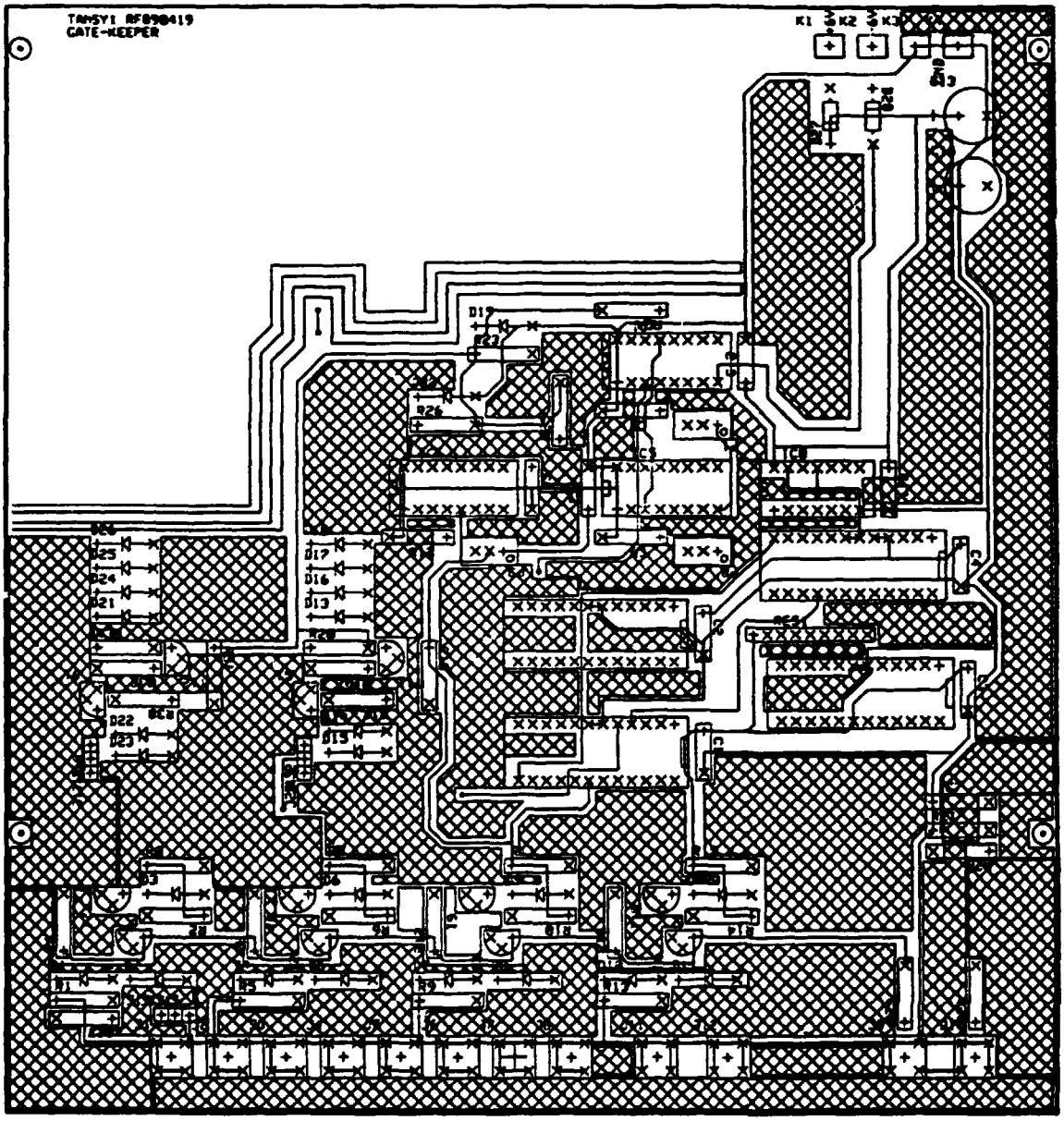

Fig.6. Board TANSY1 Layer1

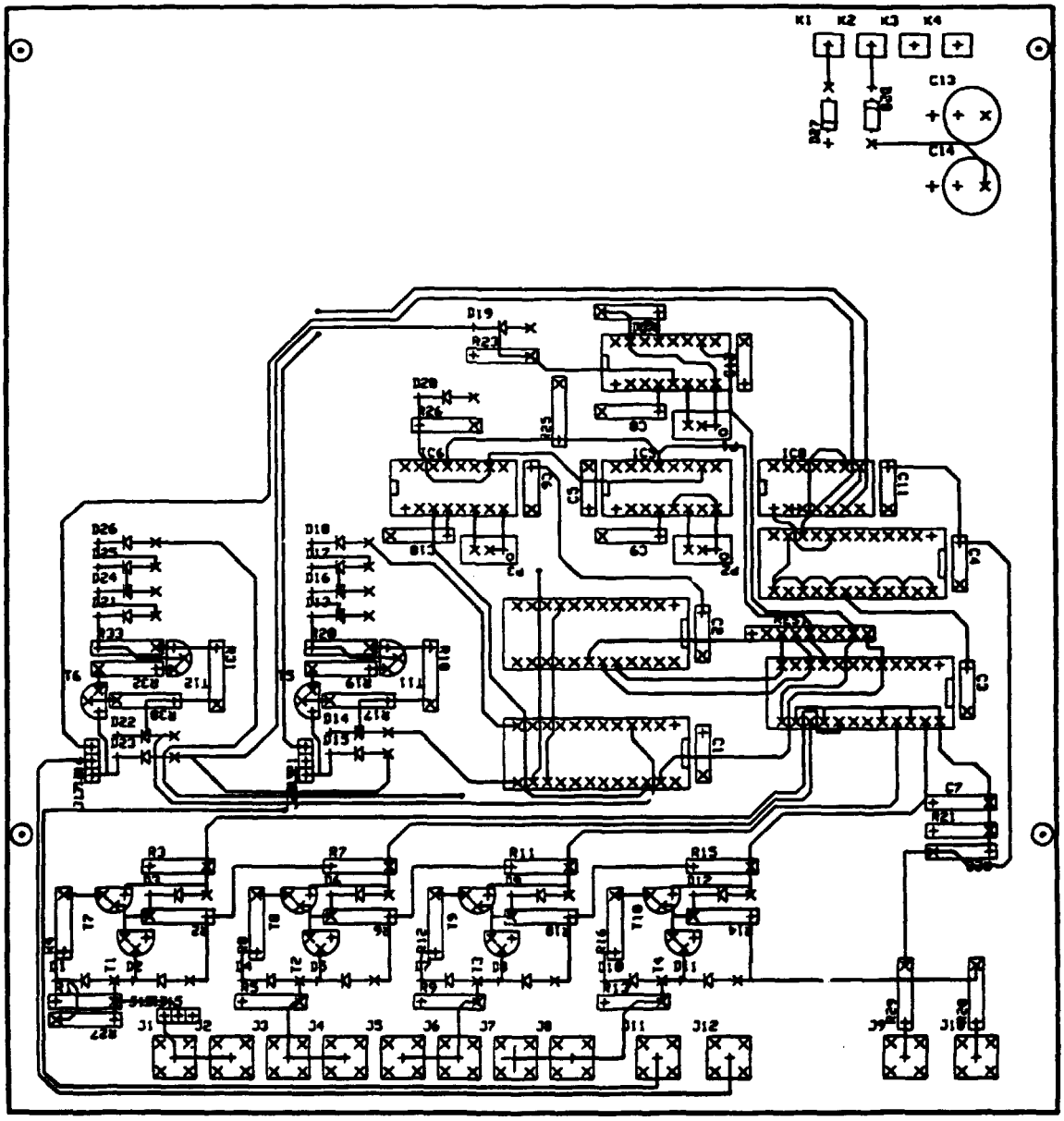

Fig.7. Board TANSY1 Layer2

Table 1. Component List

Comp. #	Type	Value
C1	CF31	100nF
C2	CF31	100nF
C3	CF31	100nF
C4	CF31	100nF
C5	CF31	100nF
C6	CF31	100nF
C7	CF41	10nF
C8	CF41	390pF
C9	CF41	390pF
C10	CF41	470pF
C11	CF41	100nF
C12	CF41	100nF
C13	CES24	1000µF
C14	CES24	1000µF
C15	CF41	680pF
C16	CF41	10nF
C17	CF41	10nF
D1	DIODE4	1N4148
D2	DIODE4	1N4148
D3	DIODE4	1N4148
D4	DIODE4	1N4148
D5	DIODE4	1N4148
D6	DIODE4	1N4148
D7	DIODE4	1N4148
D8	DIODE4	1N4148
D9	DIODE4	1N4148
D10	DIODE4	1N4148
D11	DIODE4	1N4148
D12	DIODE4	1N4148
D13	DIODE4	1N4148
D14	DIODE4	1N4148
D15	DIODE4	1N4148
D16	DIODE4	IN4148
D17	DIODE4	1N4148
D18	DIODE4	1N4148
D19	DIODE4	1N4148
D20	DIODE4	1N4148
D21	DIODE4	1N4148
D22	DIODE4	1N4148
D23	DIODE4	1N4148
D24	DIODE4	1N4148
D25	DIODE4	1N4148
D26	DIODE4	1N4148
D27	DIODE41	1N5400
D28	DIODE41	1N5400
IC1	F100114	F100114
IC2	F100104	F100104
IC3	F100102	F100102
IC4	F100125	F100125
IC5	MC10198	MC10198

Comp. #	Type	Value
IC6	MC10198	MC10198
IC7	MC10198	MC10198
IC8	74HC14	74AC14
J1	LEMOPC	
J2	LEMOPC	
J3	LEMOPC	
J4	LEMOPC	
J5	LEMOPC	
J6	LEMOPC	
J7	LEMOPC	
J8	LEMOPC	
J9	LEMOPC	
J10	LEMOPC	
J11	LEMOPC	
J12	LEMOPC	
J13	LIST1	
J14	LIST1	
J15	LIST1	
J16	LIST1	
J17	LIST1	
J18	LIST1	
J19	LIST1	
J20	LIST1	
J21	LIST1	
K1	OUTPIN	
K2	OUTPIN	
K3	OUTPIN	
K4	OUTPIN	
P1	POT67W	10k
P2	POT67W	10k
P3	POT67W	10k
R1	RES4	22k
R2	RES4	560
R3	RES4	820
R4	RES4	820
R5	RES4	22k
R6	RES4	560
R7	RES4	820
R8	RES4	820
R9	RES4	22k
R10	RES4	560
R11	RES4	820
R12	RES4	820
R13	RES4	22k
R14	RES4	560
R15	RES4	820
R16	RES4	820
R17	RES4	47
R18	RES4	680
R19	RES4	33
R20	RES4	330
R21	RES4	110
R22	RES4	1k

Comp. #	Type	Value
R23	RES4	680
R24	RES4	330
R25	RES4	330
R26	RES4	680
R27	RES4	820
R28	RES4	10
R29	RES4	10
R30	RES4	47
R31	RES4	680
R32	RES4	33
R33	RES4	330
R34	RES3	330
R35	RES3	330
RES1	SIL9	8*330
T1	NPN	2N3904
T2	NPN	2N3904
T3	NPN	2N3904
T4	NPN	2N3904
T5	NPN	2N3904
T6	NPN	2N3904
T7	PNP	2N3906
T8	PNP	2N3906
T9	PNP	2N3906
T10	PNP	2N3906
T11	PNP	2N3906
T12	PNP	2N3906