Paper presented at the 1990 Nuclear Science Symposium
Washington, October 24 -26 (This paper replaces TRI-PP-90-45)

TRI-PP-90-76
Oct 1990

500 MHz TRANSIENT DIGITIZERS BASED ON GaAs CCDs

D. Bryman, J.V. Cresswell, M. LeNoble, R. Poutissou
TRIUMF, 4004 Wesbrook Mall, Vancouver, B.C., Canada V6T 2A3

Abstract

A wide bandwidth transient digitizer based on a recently produced gallium arsenide charged coupled device (CCD) is under development. The CCD's have 128 pixels and operate at 500 MHz. Initial testing of prototype modules in Experiment 787 at Brookhaven National Laboratory is reported.

Introduction

High speed digitizing of fast detector signals vastly improves the quality of information available enabling the detailed evaluation of piled-up pulses from photomultipliers (PMT) viewing scintillators or from gas detectors as well as permitting improved time resolution to be obtained. The ability to pipeline multiple events is another essential feature for many current and future detector electronics systems.

GaAs charged coupled devices (CCD) can function as wide bandwidth analog shift registers obviating the need for costly high power, high speed direct digitizers. This is accomplished by operating the CCD in a high frequency mode to capture a signal and then, on receipt of a trigger signal, reading out the contents of the shift register at relatively low speed with an inexpensive digitizer and memory system. A 128 pixel GaAs cermet gate CCD (CMCCD) is presently under development at TRIUMF. In this paper, the implementation of the CMCCD in a prototype digitizer for applications in readout of scintillation detectors in Experiment 787 at Brookhaven National Laboratory (BNL) will be described.

GaAs Cermet Gate CCD

A schematic of a GaAs cermet gate charge-coupled device is shown in Fig. 1. A cermet film encapsulating the CMCCD transport region provides control of the surface potential along the interelectrode gaps; this arrangement enables long interelectrode gaps, MESFET compatible active layers and

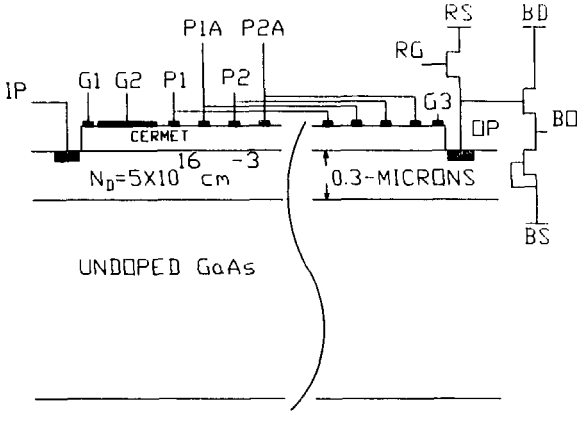

Fig. 1. Cross section of GaAs cermet gate CCD.

short transport electrodes to be used. A GaAs CMCCD has been successfully operated at a clock frequency of 4.2 GHz[1] which is the highest frequency CCD operation reported. CMCCDs have been used in two signal processing applications: a high speed GaAs detector array/CMCCD multiplexer[2] and a GaAs VHF/UHF agile bandpass filter.[3] At TRIUMF, a 128-pixel GaAs CMCCD is presently being developed for implementation in a multi-channel wideband transient digitizer.

Referring to Fig. 1, the CMCCD input region consists of the input ohmic contact (IP) and the two control gates (G1) and (G2). The transport region is comprised of the phase-1 and phase-1a transport electrodes (P1 and P1A) and the phase-2 and phase-2a transport electrodes (P2 and P2A) residing on top of the cermet layer. The devices made at TRIUMF have a 2 μm transport electrode length and a 3 μm gap length. The output region includes a control gate (G3), the output ohmic contact, the reset MESFET and the output source follower amplifier.

GaAs CMCCDs were fabricated on a MBE GaAs wafer having a 0.3 μm thick n-type active layer with $N_D = 5 \cdot 10^{16}\text{cm}^{-3}$. Six mask levels defined the patterns for the Au/Ge-Ni-Au ohmic contacts, the proton isolated active regions, the

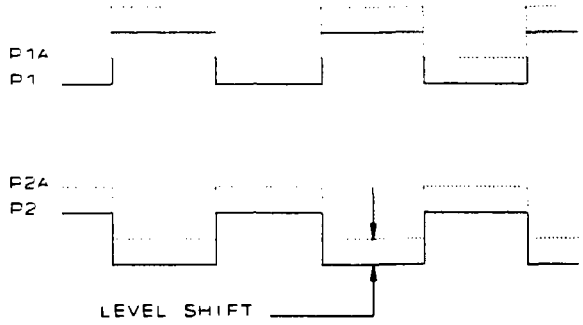

Fig. 2. Two phase clock waveforms used to operate the CCD.

Ti-Pt-Au first level metallization, the Cr:SiO (45% wt. Cr) cermet film, the interconnect vias through a polyimide interlayer dielectric film and the Ti-Au second level metallization. Conventional contact lithography was used. A photoresist liftoff method was used for patterning the ohmic contacts, the metal/GaAs Schottky barriers, the cermet/GaAs contacts and the second level metallization. Proton implants at 200 keV, $1 \cdot 10^{13}\text{cm}^{-2}$ and 35 keV, $1 \cdot 10^{13}\ \text{cm}^{-2}$ were used to isolate the active regions. The metal depositions were done using electron beam and thermal evaporations. The Cr:SiO deposition was performed using rf magnetron sputtering. Oxygen plasma etching was used to pattern the vias in the polyimide film process.

In the present CMCCD application, the device is operated using a two-phase clock illustrated in Fig. 2. The phase-1(2) clock is applied to the phase-1(2) transport electrodes and is positively level shifted by half of the peak-to-peak clock amplitude using capacitive coupling before application to the phase-1a(2a) transport electrodes. The dc level shift introduces a fringing electric field component in the active layer between the phase-1(2) and phase-1a(2a) transport electrodes directing the flow of signal charge through the CMCCD. A charge packet in a potential well under a phase-1a(2a) transport electrode will be transferred to the potential well beneath the subsequent phase-2a(1a) transport electrode on the negative (positive) and positive (negative) transitions of the phase-1 and phase-2 clocks. Charge transfer efficiencies in excess of 0.999 have been achieved using this method of operation, making it practical to use in wideband signal processing applications.

GaAs CCD Based Transient Digitizer

A block diagram of the transient digitizer is shown in Fig. 3. It is comprised of three primary

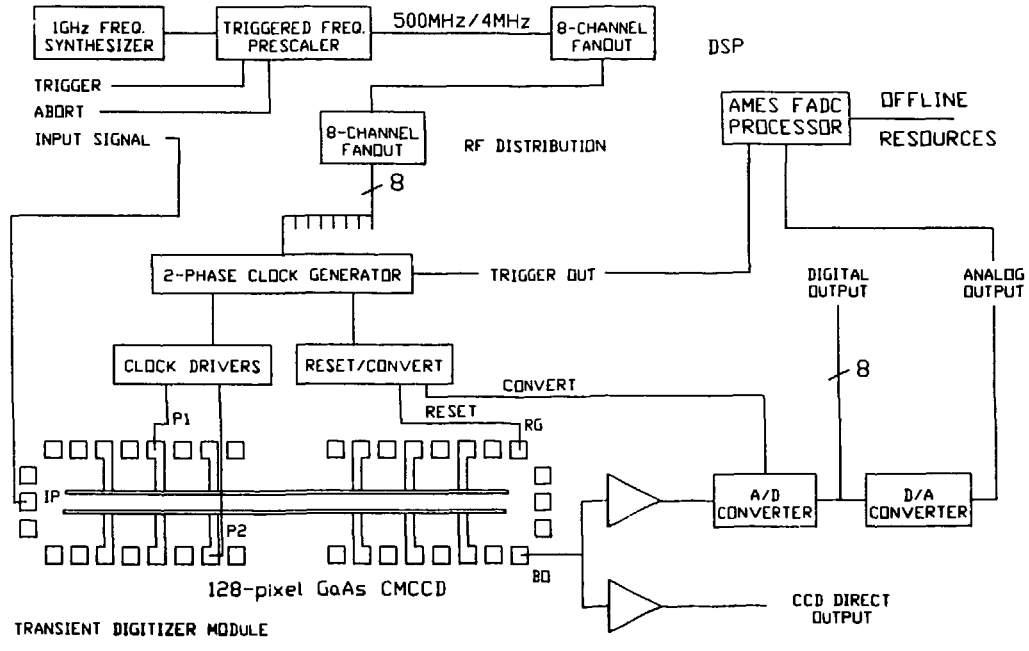

Fig. 3 Block diagram of the GaAs CCD based transient recorder.

sub-systems: the rf distribution system, the CMCCD transient digitizer modules and the FADC-processor system.

The rf distribution system provides rf signals to the CMCCD transient digitizer modules. This system consists of a 1 GHz frequency synthesizer, a triggered frequency prescaler and a power distribution network. The 1 GHz frequency synthesizer followed by the triggered frequency prescaler provides a 500 MHz data acquisition (output) clock signal source. The high frequency output is normally active and is switched to the low frequency state subsequent to the application of an externally supplied trigger signal. The duration of the low frequency state is set to 128 low frequency clock cycles after which the high frequency mode resumes. The 'abort' input is used to asynchronously reset the prescaler to its high frequency output state. Distribution of the rf signal to the transient digitizer modules is accomplished using a bank of 8-channel fanout units.

The CMCCD transient digitizer module provides analog to digital (A/D) or analog to analog (A/A) conversion of the input signal. The input signal is clocked into the 128-pixel CMCCD using the 500 MHz data acquisition clock supplied by the rf distribution system, thus allowing a 250 MHz input signal bandwidth. An externally generated trigger pulse disables the accumulation of the input signal and causes the 4 MHz low frequency pulse burst to be applied to the CMCCD. The captured signal is passed to an 8-bit A/D converter during this time and is transformed into a string of 128 8-bit words providing a low frequency 8-bit wide binary output stream. The binary data stream is also transmitted to an 8-bit digital to analog (D/A) converter providing a low frequency analog output signal.

The CCD and its clock driver circuitry were located on a printed circuit board along with the A/D and a D/A converter. This arrangement facilitates high resolution transmission of the data to a remote data acquisition system. We are employing an inexpensive FASTBUS 8-bit digitizer[4] developed at Iowa State University and Ames Laboratory for the Delphi experiment at LEP. Each FASTBUS board contains 32 FADC channels and 256-deep memories capable of operating at frequencies up to 15 MHz and a programmable 16 MHz TS68000 microprocessor which presently is used to repack over-threshold data for efficient transmission to the data acquisition system. The CCD low frequency clock is used to synchronize the FADC's.

The prototype 500 MHz GaAs CCD transient digitizer performance was investigated. Measurements were made on several digitizer channels to determine the linearity characteristics and to provide a qualitative indication of the overall performance under normal operating conditions. The measurements described below were made using a Tektronix TEK-11403 digital sampling oscilloscope. The "input signal" and the "analog output" signal of the digitizer (see Fig. 3) were measured in all cases. The small zero-level offset signal normally present at the digitizer output was removed using the signal processing capability of the TEK-11403.

Fig. 4 shows the typical input/output response of the transient digitizer operated at 500 MHz. The axes have been normalized to the full scale output value of the "analog output" of the digitizer. The measurements used a 100-mV, 10 ns wide rectangular input pulse applied through a high precision attenuator which was used to vary the pulse amplitude from 0-dB to 40-dB in 2-dB increments. A linear fit to the data using an equation of the form y=m*x is also illustrated in Fig. 4. The slope of the "best" fit line is m=1.003 which is close to the ideal value of unity. Fig. 5 illustrates the percentage of full scale error between the "best" fit line and the data shown in Fig. 4. A linearity error of nominally less than +/-2% of full scale was achieved with the prototype digitizers.

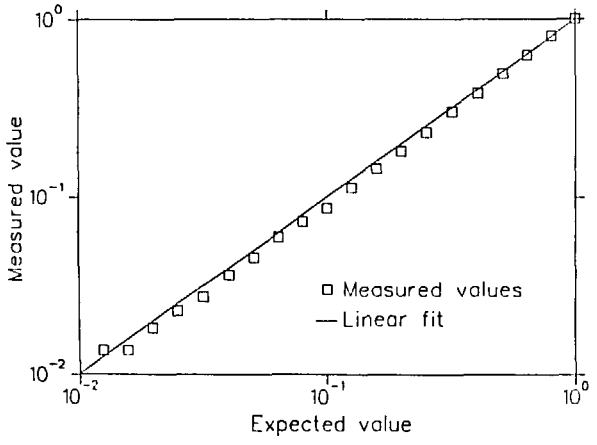

Fig. 4. Response of the GaAs CCD transient digitizer at 500 MHz.

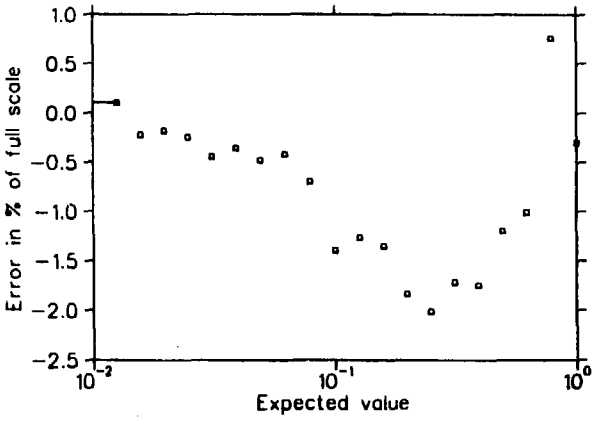

Fig. 5. Deviation from linearity of the GaAs CCD transient digitizer at 500 MHz.

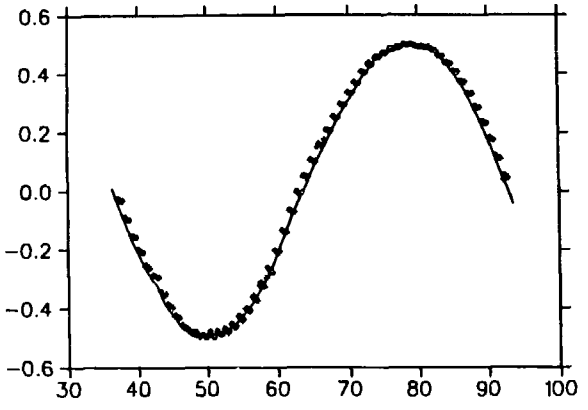

Fig. 6. Sinusoid response of the GaAs CCD transient digitizer at 500 MHz.

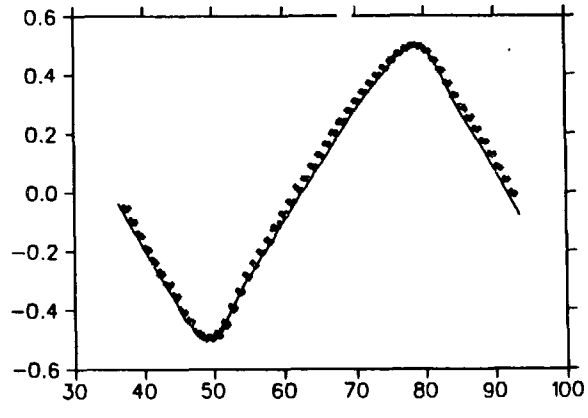

Fig. 7. Ramp response of the GaAs CCD transient digitizer at 500 MHz.

Qualitative demonstrations of the performance of the transient digitizer to known test waveforms are shown in Fig. 6 and Fig. 7. Fig. 6 shows the response of the digitizer to a single period sinusoid waveform spanning 55 bins lying between bin 37 and bin 93 of the 128 CCD bins and Fig. 7 shows a similar digitizer response to a single period ramp waveform. In both figures the input signals (solid lines) have been superimposed onto the output signals by scaling the period of the input signal by a factor of 128.

Application to BNL E787

Experiment 787 at BNL is aimed at studying rare kaon decays, in particular $K^+ \rightarrow \pi^+\nu\bar{\nu}$. Side and end views of the cylindrically-symmetric detector[5] are shown in Fig. 8. Briefly, a 775 MeV/c kaon beam is slowed by a BeO degrader and stopped in a segmented scintillator fiber target[6] located at the center of the detector. The target consists of 3 m long, 2 mm diameter scintillating fibers grouped into 379 triangular clusters of six, each viewed by a 1 cm diameter photomultiplier tube. The target

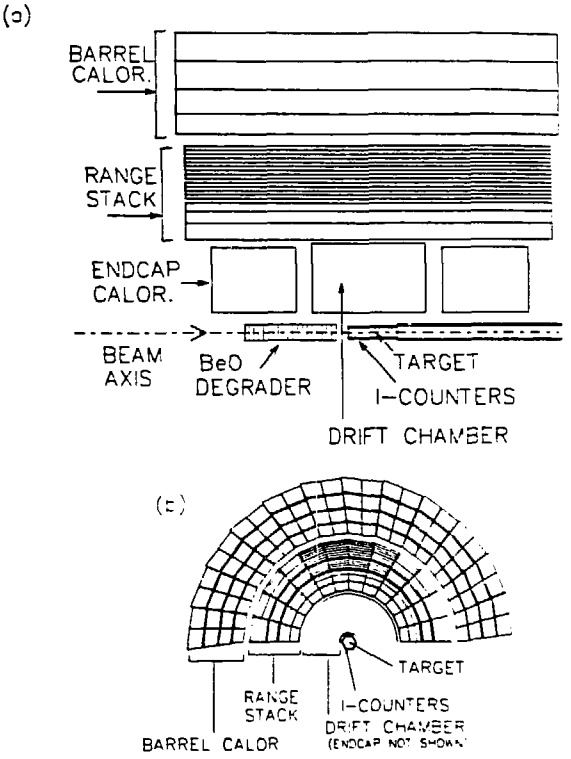

Fig. 8. Side (a) and end (b) views of the E787 detector.

elements are used to track the incident kaons which travel along the fibers as well as to detect the signals from decay pions which cross the fibers transversely into the detector. Charged particles from the K^+ decay are momentum analyzed in a cylindrical central drift chamber[7] in a 1 T solenoidal magnetic field aligned along the detector axis. The particles are stopped in a 15-layer stack of 2 m long plastic scintillators viewed by phototubes at each end. These range stack counters are used to measure the kinetic energy and range of charged particle kaon decay products. Surrounding the drift chamber and range stack are electromagnetic calorimeters which cover almost 4π solid angle to detect photons.

Near the end of a recent data run, 18 channels of prototype CCD digitizers were deployed on the target. The signals from 21 non-adjacent target elements were multiplexed into each digitizer channel. Fig. 9 shows an event display of the target elements hit in a sample event. The numbers within the target triangles in the figure correspond to the values recorded by integrating analog-to-digital converters. The arrows point to the signals digitized at 2 ns intervals for each element hit. CCD pedestals have been subtracted and a threshold of 3 counts has been required in software. Channels A and B were hit by the incident kaon which traversed the target elements longitudinally depositing 50.3 MeV and 15.4 MeV, respectively. The decay particle emerged transversely about 16 ns (8 CCD buckets) later striking channels C, D, and E leaving between 0.6 and 1.5 MeV in each element. The CCD calibration is roughly 3 counts/ MeV.

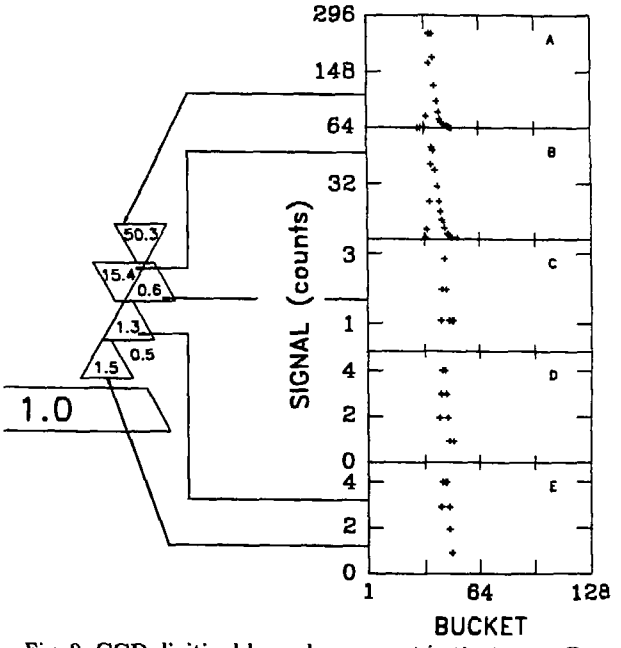

Fig. 9. CCD digitized kaon decay event in the target. On the left is shown the target triangles hit along with the energy deposited as determined by integrating adc's. On the right are shown the digitized pulses as described in the text.

One range stack counter in the pion stopping region was also instrumented with a CCD digitizer. Fig. 10 shows an example of a pion stop signal followed about 25 ns later by the decay to a muon (approximately 4 MeV) as recorded by the CCD digitizer. The range stack scintillators are already instrumented with transient digitizers[8] (TD) based on the Tektronix TKAD508 A/D hybrid with two interleaved 250 Msample/s A/D converters. The CCD digitizers give results consistent with the TD's.

Conclusion

Prototype CCD digitizers which sample at 2 ns intervals for a period of 256 ns have been constructed and tested in Experiment 787 at BNL. The next step in the development of wide band CCD digitizers is to improve the layout by deploying the CCD chip and its driving circuitry on a separate daughter board and create a multi-element motherboard. Further improvements to the on-chip CCD input circuit are also under development to attempt to increase the dynamic range.

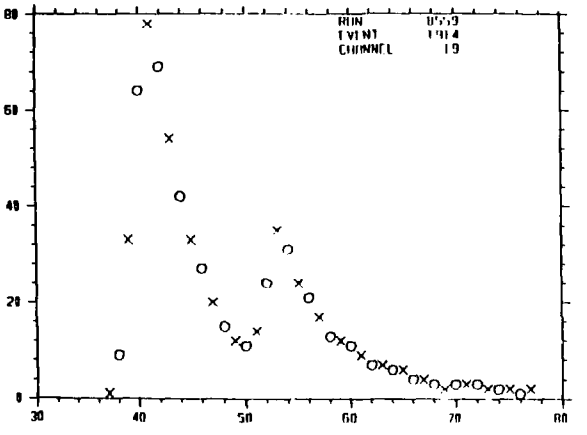

Fig. 10. CCD digitized $\pi \rightarrow \mu$ decay in the range stack.

Acknowledgements

We would like to thank the E787 collaboration for their efforts and assistance in this work. We are particularly grateful to M. Constable, A. Daviel, S. Daviel, M. Burke and A. Turcot. In addition, we would like to thank the Ames group for their help in providing and using the FADC system.

References

[1] E.A. Sovero *et al.*, GaAs IC Symp. Tech. Dig., p 101 (1984).

[2] R. Sahai *et al.*, Proc. SPIE Int. Soc. Opt. Eng., **477**, 165 (1984).

[3] E.A. Sovero *et al.*, GaAs IC Symp. Tech. Dig. p 92 (1983).

[4] H.B. Crawly *et al.*, IEEE Transactions on Nuc. Science **35**, 295 (1988).

[5] M.S. Atiya *et al.*, Phys. Rev. Lett. **64** 21 (1990).

[6] J.S. Frank and R.C. Strand, in *Proc. of the Workshop on Scintillating Fiber Detector Development for the SSC* (FNAL, Batavia, IL, 1988)

[7] J.V. Cresswell *et al.*, IEEE Trans. Nucl. Sci. **35**, 460 (1988).

[8] M.S. Atiya *et al.*, Nucl. Instrum. Meth. **A 279**, 180 (1989).