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DIGITAL ELECTRONICS FOR THE INCLUSION OF SHOWER MAX AND PRESHOWER WIRE DATA IN THE CDF SECOND-LEVEL TRIGGER

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ABSTRACT

As part of the upgrade program at CDF, electronics has been built to bring the shower max (CES) and preshower (CPR) data into the trigger at level 2. After each crossing, 384 bits from shower max and 192 from the preshower wires are latched. Data from tracks are bussed to this module to provide the wire address and momentum which are then successively compared to the wire data in large look-up tables. Approximately 50 nanoseconds is required to determine a match, write the results in FIFO, and make the results available to track memory. Monte Carlo analysis has indicated that an increase in efficiency of a factor of three in triggering on b decays will be achieved with this hardware.

PHYSICS CONSIDERATIONS

Hadron colliders have an enormous potential for the study of b-physics, provided that efficient triggers can be devised for the B-decay products. For example, the $B\bar{B}$ production rates measured at CDF, in the central region alone (e.g., abs (Y) < 1, P_t > 6 GeV/c), correspond to 100 Hz at Tevatron luminosities of 10^{31}. This rate may be contrasted with that expected for an e^+e^- B factory, which would be around 3 Hz at design luminosity of $3 \cdot 10^{33}$. To compare with LEP, the total $B\bar{B}$ production in the CDF central detector, 10^9 pairs in a 100 pb^{-1} run, would be equivalent to $5 \cdot 10^9$ hadronic Z decays. To date, the most useful B-triggers in the CDF experiment are the single lepton (electron or muon) triggers, and the J/ϕ dimuon trigger. Of course, the additional requirement of a second lepton in conjunction with these basic triggers is useful for studies that require b-tagging. While the J/ϕ modes are very useful for reconstructing exclusive B decays (eg, B $\rightarrow$J/ϕ +K, K*, ϕ, Λ) and are the most likely vehicle for the observation of CP violation in the B sector (using B $\rightarrow$J/ϕ K_S), the semileptonic decay triggers are needed if one is to identify the charge of the B. For example, the detection of B_s-$\bar{B}_s$ mixing, an important measurement for the Standard Model, could not be accomplished with J/ϕ modes, but would likely be based on observation of electron-D_S correlations.

The CDF trigger employs a "level-3" processor farm, which does offline reconstruction to select highly enriched event samples for physics analysis. The input to this farm is provided by the "level-1" and "level-2" triggers, which use fast analogue signals from the calorimeter and raw TDC information from the central tracker and muon chambers, to define electron, muon, jet and missing E_t trigger objects. To match the bandwidth of the hardware Event Builder and the level-3 farm, the level-2 accept rate is constrained to be less than around 35 Hz, or 3000 nb at 10^{31}. The CDF single electron trigger, with a 9 GeV threshold, has a level-2 accept rate of 500 nb, or about 18% of the total bandwidth. The actual electron purity is around 7%, or 30 nb after level-3 and offline processing. For central muons, with 1992 central upgrade chambers, the sample purity and level-2 rates are comparable. However, the muon fiducial coverage is less than that for

electrons, and with a fixed P_t threshold, the electron trigger provides about four times the B-physics rate of the muon trigger.

There are several handles for further improving the purity of the level-2 electron trigger, and any improvements translate into a corresponding increase in the rate of B-events written to tape, since the overall trigger is bandwidth-limited. The offline identification of electrons relies heavily on the detailed information on shower development provided by the central strip and preradiator chambers, which are located at depths of $6X_0$ and $1X_0$ respectively. The baseline level-2 trigger associates a high-P_t charged track with an electromagnetic calorimeter cell. The strip and preradiator chambers would allow a much finer-grained match between the track position and the shower energy, and this tighter matching can reject the main backgrounds in the baseline trigger - namely "overlap" events with charged tracks plus gamma rays in the same calorimeter cell. Figure 1 shows the expected level-2 rates for electrons as a function of the calorimeter E_t threshold, for the baseline system (top curve), and with a strip-chamber pulse height requirement (bottom curve). The overall rejection provided by the strip chamber alone is about a factor of three. This would represent a significant increase in the purity of B's written to tape. Numerically, with the baseline trigger and electron bandwidth, CDF can write approximately 10^6 B $\rightarrow$ electron events to tape in 100 pb^{-1} (all backgrounds subtracted); the strip chamber trigger would allow this rate to increase to approximately $3 \cdot 10^6$ per 100 pb^{-1}. That may be compared with B $\rightarrow$ electron or muon rates at LEP, around (45,000 efficiency) per 10^6 Z decays.

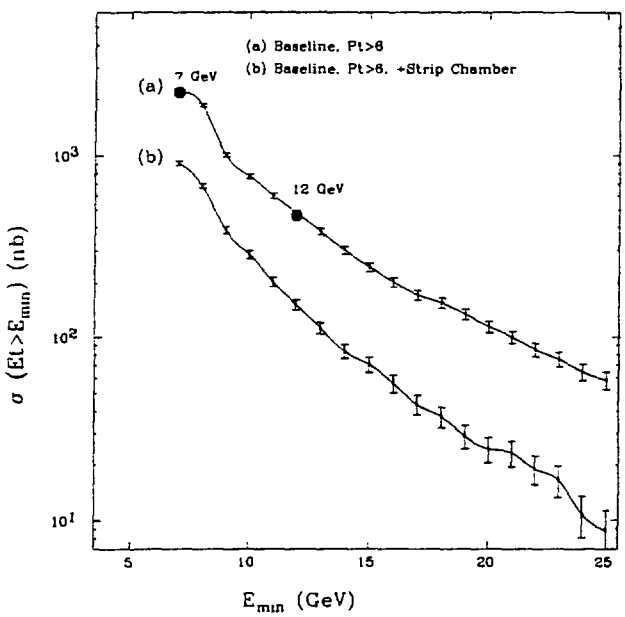

Fig. 1 Level-2 trigger rates in CDF as a function of the calorimeter E_t threshold. The top curve ("a") shows the baseline CDF trigger used in 1989, with a track P_t threshold set at 6 GeV/c (3.3 GeV/c for E_t<9 GeV). The bottom curve ("b") shows the same rates with an additional strip-chamber pulse height requirement, set to be 90% efficient for electrons for each E_t threshold. The solid points are the measured level-2 cross sections for the 1989 CDF run.

HARDWARE DESCRIPTION

The digital electronics to incorporate CES and CPR data in the CDF second level trigger is built in FASTBUS protocol. Two identical cards, one for CES and one for CPR reside in FASTBUS adjacent to the CTCX card. The electronics is built on two cards because it is extremely difficult to provide space for chips and the necessary connector space required for the 384 CES and 192 CPR bits. The two physically identical cards are configured under software to accommodate either CES or CPR information. The cards are built using multi-layer technique as 12 layer cards with essentially all devices implemented in surface mount, and with integrated circuits mounted on both sides of the card. Layout and routing were done at Argonne using the Telesis system.

In order to deal with the connector problem the 384 CES bits and 192 CPR bits are brought to an active patch panel near the digital electronics. The bits are carried from the detector on approximately 50 meters of twisted pair as differential TTL and translated to single-ended TTL on this patch panel. They go from there

as single-ended TTL signals on approximately 2 meters of flat ribbon cable to the digital electronics. Honda high density connectors with .025" pitch are used to bring the single-ended bits from the active patch panel to the digital module. FASTBUS interfaces are provided on both cards since it is necessary to program both cards and execute diagnostics on both individually, and since it was desired to make the cards identical as far as layout and routing. After a crossing, a sequence of sets of track data is provided by the Central Fast Track Processor (CFT). Track data provided by the Central Fast Track Processor is latched by strobes from the CTC. Data and strobes are bussed from the adjacent CTCX card.

The logic is shown in Fig. 2. After a crossing, the 384 bits from the CES and the 192 bits from the CPR are received from the front end electronics, and after an appropriate time for data to become valid, are latched. The CES bits are partitioned as 48 busses, each containing 8 bits from the East or West wedges, and numbered from 0 to 23, E or W. The CPR bits are partitioned in like fashion as 48 busses, each containing 4 bits from the East or West wedges, and numbered from 0 to 23, E or W. Each of these busses forms part of the address word which addresses an SRAM look-up table. Following the latches, the bits are masked by a set of mask words previously written into on-card registers from FASTBUS. Mask bits may be used to remove noisy wires and for diagnostic purposes. The latched and masked bits are logically OR'ed to proved CES and a CPR bits for each wedge, which are translated to differential ECL and provided at a connector.

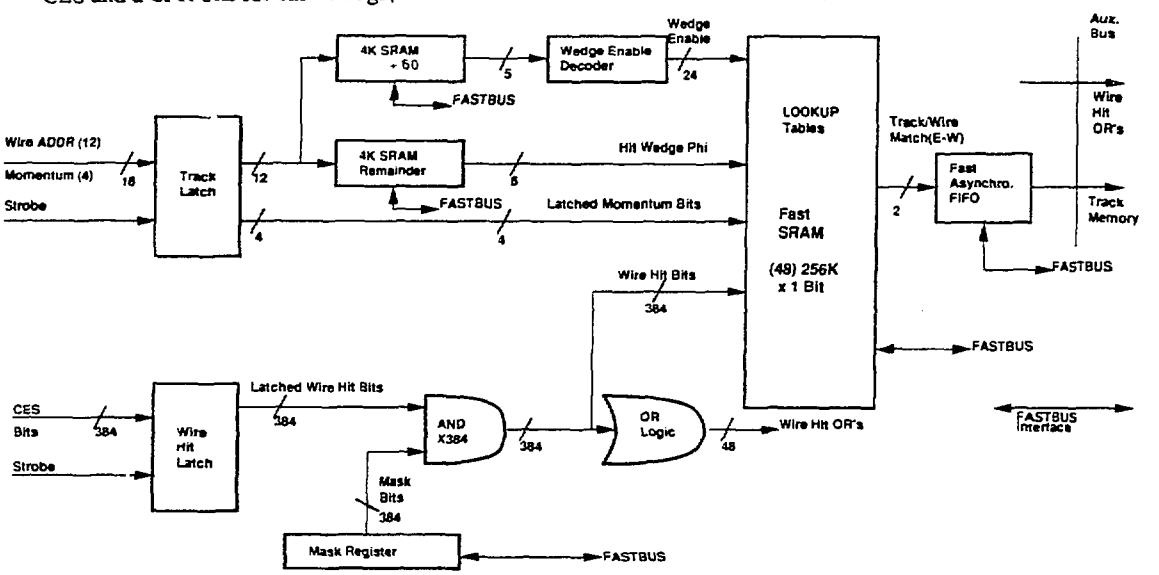

Fig. 2 Simplified Block Diagram: Digital Electronics for the Inclusion of Shower Max and Preshower Wire Data in the CDF Second-Level Trigger

When an 12 bit WIRE_ADDR word and 4 bit MOMENTUM word are received from the CFT, they are latched by RD_STR which is also received from the CTCX. The 12 bit WIRE_ADDR word constitutes the address word for two 4k SRAM's. The first SRAM performs an algorithm which divides the value represented by the 12 bit word by 60, and produces a 5 bit output word. Since there are 1440 wires, the quotient is a wedge number going from 0 to 23. This 5 bit wedge number can then be decoded to yield 24 enable signals, which can be used to enable the appropriate SRAM's, each of which is associated with one wedge. The other 4k SRAM performs an algorithm which yields the remainder when the wire address is divided by 60, which is a representation of the hit position in phi across the wedge which has been selected by the other SRAM. It is necessary only that there be a defined one-to-one relationship between WIRE_ADDR and wedge number and phi position across a wedge. There is no requirement for exact monotonicity.

In the case of the CES, the 6 bits from the second SRAM, the 4 MOMENTUM bits, and the 8 CES bits constitute the address supplied to the SRAM which is enabled by the decoded wedge number. In the case of the CPR, the 6 bits from the second SRAM, the 4 MOMENTUM bits, and the 4 CPR bits constitute the address supplied to the SRAM which is enabled by the decoded wedge number. The outputs of these SRAM's are tied together and since 23 of the 24 chips are not enabled, the one which is enabled will produce output data on the CESE, CESW, CPRE, and CPRW line. This output data is strobed into an asynchronous FIFO, where it can then be strobed into track memory in time with the muon data by a strobe supplied by the muon hardware. The logic is implemented in high-speed CMOS SRAM's and ACT logic and data is valid at the output FIFO in less than 50 ns. from the time WIRE_ADR is latched by RE_STR. The card has logic to allow all SRAM's to be read/written from FASTBUS to permit initialization and execution of diagnostics.

All memories and registers can be written/read from FASTBUS, and for diagnostic purposes it is possible to set bit patterns of the CES and CPR hits. This is accomplished by permitting all the input latches

to be set, and then the mask words are used to create the bit patterns which can be run through memory, and the output data tested. It is necessary that test bits be latched in the WIRE_ADR latch so that complete address information is supplied to the 256k SRAM's.

TESTING AND SOFTWARE

The first tests of the digital electronics fastbus card were performed at Argonne in a test setup which consisted of an IBM PC interfaced to a fastbus crate. A programmable LeCroy 1821 Segment Manager provided the interface between the fastbus board and the IBM PC, the latter from which diagnostic commands were issued. We used a Single Platform Diagnostic Package, called SPUDS[1] both to troubleshoot the board as well as to read and write to the various board registers and RAMs which resided in both data and CSR space. In addition, we built a test input cable which allowed us to fake data to the input latches to test data flow through the board.

The second phase of testing occurred at Fermi National Laboratory. We used a mini fastbus crate which housed a Kinetic Systems Q-bus Processor (QPI). The QPI was interfaced to a mini VAX computer which was clustered with the CDF online computers. Several diagnostic software packages were developed.

The first diagnostic program performed tests similar to those already conducted at Argonne. Namely, the program performed read and writes to the various registers and RAMs. Also available in this program are more extensive tests which march 0's and 1's through the registers and rams. In addition, the program tests the performance of the asynchronous FIFO. A second program allowed the user to download specific look-up tables to the various RAMs. This second program was designed to test software algorithms which matched electron pulses measured in the shower max detector with tracks measured in the CFT.

The final stage of testing the fastbus board consisted of integrating it into the L2 trigger in a parasitic mode. This was done by installing it into its designated L2 fastbus crate and connecting it to electronic members both upstream and downstream of itself. A schematic of the output signals received by the track list card is shown in Fig. 3.

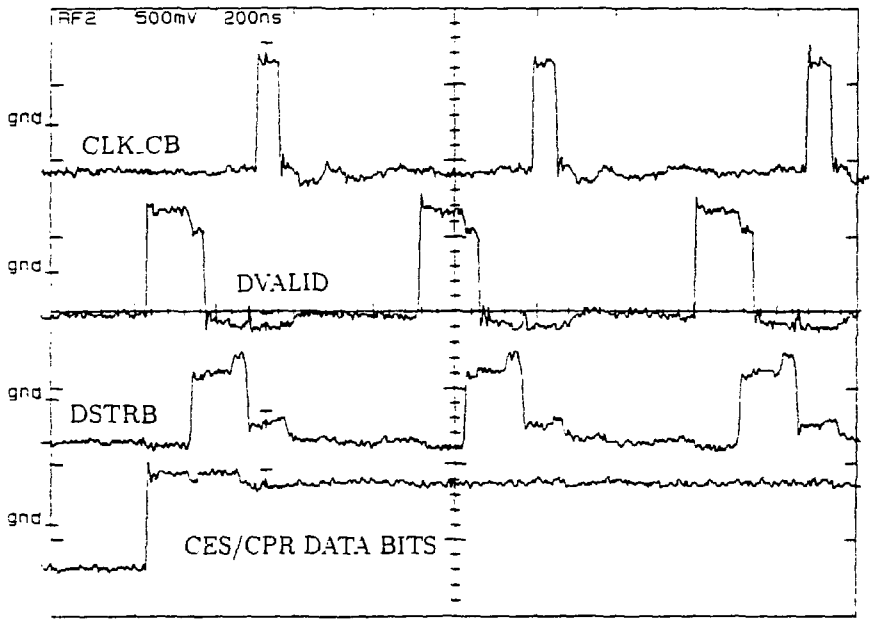

Fig. 3 The FIFO generates the signal DVALID and transmits it to the track list card along with the CES/CPR data bits for every track. When the track list card has received the DVALID signal, it latches the CES/CPR data bits and responds to the our card with the handshake signal DSTRB. When the signal DSTRB is received by the FIFO, it causes the FIFO to upload the next pattern of CES/CPR data bits and generates another DVALID.

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REFERENCES

1. J. Anderson and J. Franzen, Data Acquisition Hardware Group, SPUDS User Manual, FNAL (1992).