Fermi National Accelerator Laboratory

FERMILAB-Conf-94/391-E

CDF

SVX II a Silicon Vertex Detector for Run II of the Tevatron

Daniela Bortoletto
The CDF Collaboration

Fermi National Accelerator Laboratory
P.O. Box 500, Batavia, Illinois 60510

November 1994

Presented at the *Third International Workshop on Vertex Detectors*, Bloomington, Indiana, May 12-16, 1994

Disclaimer

SVX II A SILICON VERTEX DETECTOR FOR RUN II OF THE TEVATRON

Daniela Bortoletto [1]
Purdue University
West Lafayette, IN, 47907

Abstract

A microstrip silicon detector SVX II has been proposed for the upgrade of the vertex detector of the CDF experiment to be installed for run II of the Tevatron in 1998. Three barrels of four layers of double sided detectors will cover the interaction region. The requirement of the silicon tracker and the specification of the sensors are discussed together with the proposed R&D to verify the performance of the prototypes detectors produced by Sintef, Micron and Hamamatsu.

[1]Presented at the Third International workshop on Vertex Detectors, Bloomington, IN, May 12-16,1994

1 Introduction

High precision vertex detection is a key element of the first experimental evidence for the top quark presented by the CDF collaboration [1]. The analysis of the decay $t \to Wb$ is based on the capability of the silicon vertex detector (SVX) to identify b decay vertices within collimated high P_t jets. Vertex detection with the SVX detector, which was operational during run 1A of the Tevatron between 1989 and 1992, has also contributed to the CDF b-physics program. CDF has measured the lifetime of neutral and charges B mesons in the fully exclusive decays $B^- \to \psi K^-$ and $B^0 \to \psi K^*$. These measurements are not affected by the systematic errors due to missing neutrinos and excited D^* present in the study of the semileptonic decays $B \to D^* \ell \nu$ [2] and therefore are complimentary to the LEP results. CDF has also presented the best measurement of the lifetime of the B_s meson [3] and has collected about 50 events in the golden mode for CP violation $B^0 \to \psi K_s$ [4].

The SVX detector was replaced in 1993 by a radiation hard detector SVX'. The planned increase in the number of p and $\bar{p}$ bunches in the accelerator by 1998 and the resulting shorter bunch spacing of 132 or 396 ns requires a replacement for the SVX' detector. The installation of the new detector [5], SVX II, and the higher luminosity will increase the physics reach of CDF. SVX II which is roughly twice as long as SVX will cover a larger fraction of the Tevatron interaction region. The increase in solid angle coverage together with adding $r-z$ information will enhance the b-tagging efficiency for top events by a factor 1.6 to 2.0 depending on the top mass. The capability of using impact parameter information from the vertex detector in the level 2 trigger (SVT) will possibly allow the study of some CP violating modes such as $B \to \pi\pi$.

The main injector upgrade in 1998 will provide a peak luminosity in Run II of $\approx 10^{32}$ cm^{-2} sec^{-1} and an integrated luminosity of about 1 fb^{-1} per year. The radiation environment of Run II is challenging and the experience gained with the SVX II detector and the SVT trigger will be extremely valuable for the design of silicon detectors for the LHC.

In this paper we describe the first stage of the SVX II upgrade consisting of a four layer three barrel system. Future upgrades could include the addition of two further layers and/or forward disks. We do not discuss these upgrades here.

2 Mechanical design

The design of SVX II is largely based on improvements to the original SVX design. The overall length of about 1 meter, about twice the original detector, is required to cover the long interaction region of the Tevatron ($\sigma_z = 30$ cm) and to extend the coverage in pseudorapidity to about η of 2. The overall coverage is achieved by a three barrel geometry mounted symmetrically with respect to the interaction point. Each barrel covers 32 cm in z and consists of four radial layers of silicon sensors in a twelve wedge geometry. The location of the layers is shown in table 1. Four silicon detectors are mounted together into a single mechanical unit called a ladder and are wirebonded in pairs which are read out at each end. The design of a prototype ladder is shown in fig. 1. The ladders are arranged in a twelve wedge geometry with each wedge covering about 30°. This geometry provides suitable segmentation for the SVT processor. The layer are staggered allowing overlap between detectors (> 5 strips) for alignment purposes. In order to minimize the gaps between the barrel the hybrid circuit containing the read-out chip will be mounted in direct contact with the silicon. The dead space between barrels in SVX was about 4 cm while the goal for SVXII is about 1.5 cm.

The ladders are supported by a bulkhead structure which surrounds a beam pipe with a

Table 1: SVX II geometry

Layer	$r_a(cm)$	$r_b(cm)$	pitch (μm)	N_{chip}	width (cm)	overlap (in strips)
0	2.4	2.9	60	2	1.8	17
1	4.1	4.6	62	3	2.6	7
2	6.6	7.0	58	5	3.9	10
3	8.3	8.7	60	6	4.8	7

1" inner diameter. The bulkhead will be machined in Beryllium because of its long radiation length. The design of a prototype bulkhead is shown in fig. 2. The bulkhead will also provide cooling by an integrated channel operated at underpressure to reduce the risk of leaks.

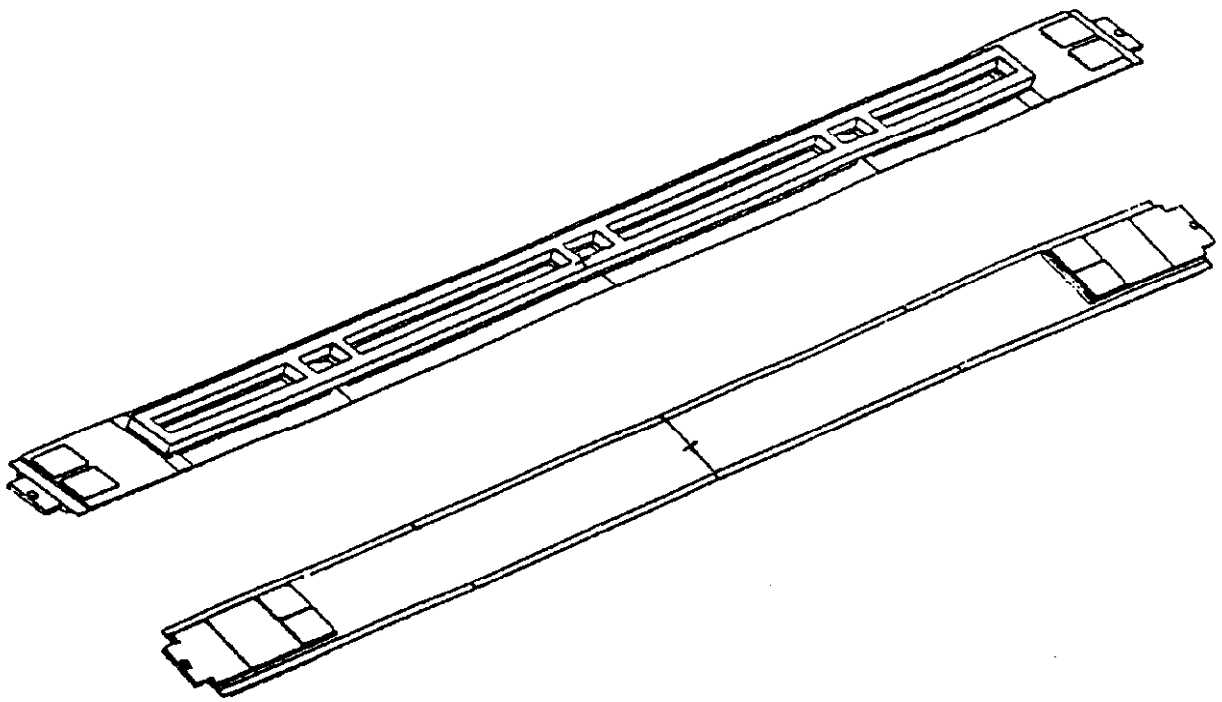

Figure 1: Layout of the SVX II ladders

The alignment requirements for SVX II are severe. The ladder support structure is designed to maintain detector-to-detector alignment to within $\pm 5\mu$m in the $r-\phi$ direction and to provide sufficient stiffness and thermal stability to eliminate gravitational and thermal bowing. The maximum amount of intrinsic bow in the ladder is designed to be less than 50μm and will

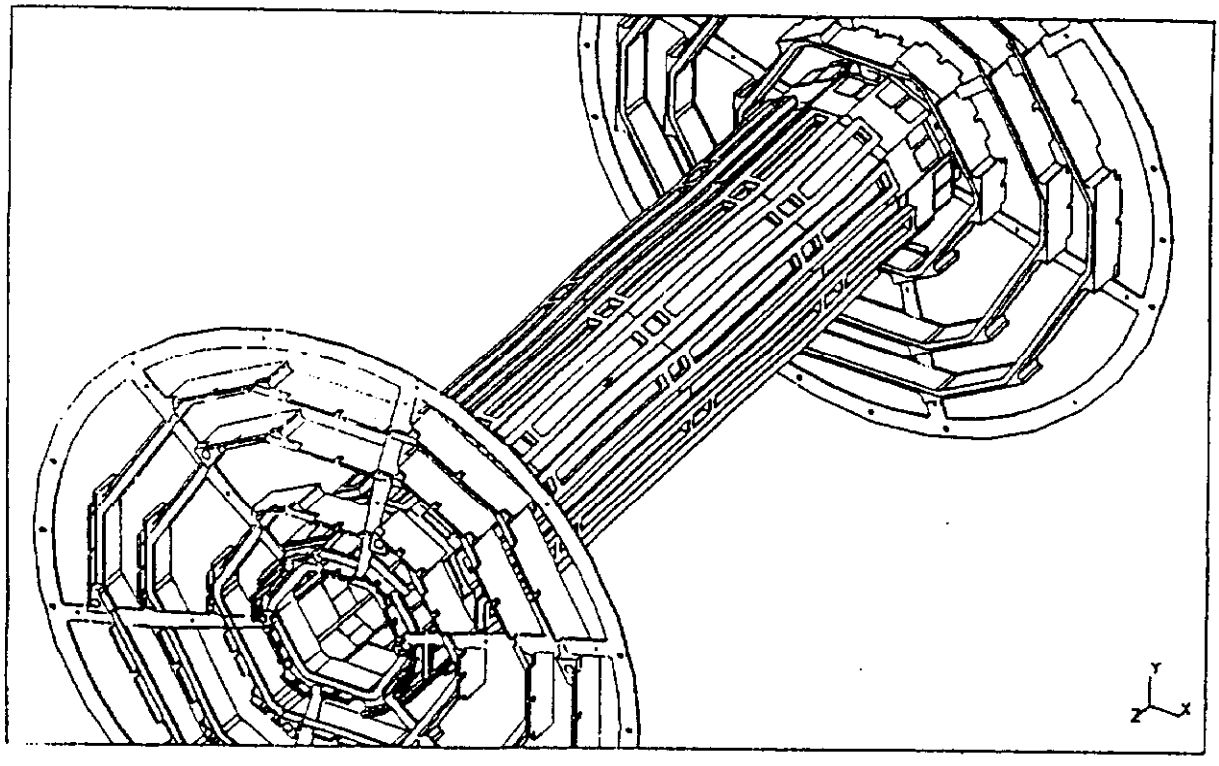

Figure 2: Layout of the SVX II bulkhead

be measured with an accuracy of $\pm 10\mu$m. Since the double sided detectors have orthogonal $r-z$ strips a tight tolerance on the radial positioning of the detectors is required because of the coupling between radial and z position uncertainty for tracks at large angle of incidence. The z-position uncertainty in the placements of the detectors during the ladder construction process should be less than $\pm 10\mu$m. The three barrels will be supported by a frame which will allow alignment of the entire system with respect to the accelerator beam line to an accuracy of 100 μradians as needed by the secondary vertex trigger SVT. Preliminary studies show that these requirements urge a stiffer support system than the carbon-fiber Rohacel foam hybrid used for SVX. The SVX II design group has looked at various hybrids and a carbon-boron composite by Textron looks promising [6].

3 Temperature and Cooling

Initial measurements of the SVX II chip estimate a dissipated power of 280 mW per chip. The power generated by the front-end electronics/ladder is also greater than SVX because of additional channels readout from double sided detectors. The cooling will be provided by water with an input temperature of 2°C. We are considering a cooling channel machined into the bulkhead. The present design achieves, with a gas temperature of 10°C a temperature of about 18°C under the chip. The temperature profile along a silicon half-ladder varies from

about 8 to 12°C.

In order to operate the detectors at a low temperature we are carefully evaluating the coefficients of thermal expansion (CTE) of the material used in ladder construction to match that of silicon. For example, the boron-carbon material does not only provide the required stiffness but also has a CTE of 2.5 ppm/°C very similar to the CTE of silicon of 2.6 ppm/°C. We are also evaluating the possibility of using coolants in the water to reach a even lower temperature but we are very concerned about the thermal stress.

4 Detectors

The SVX II will be equipped with double sided silicon detectors in order to minimize the material and maximize the tracking information. The detectors will be made with 300 μm thick n-type high resistivity bulk silicon. Longitudinal p^+ implant strips on one side (p-side) will collect holes and will measure the $r-\phi$ coordinate while the $r-z$ coordinate will be measured by orthogonal n^+ strips collecting electrons on the other side (n-side). The biasing scheme is achieved via polysilicon resistors. The method has been chosen for its radiation hardness and variation in resistance at the few per cent within a wafer. On both sides the strips will be coupled to the readout electronics through an integrated coupling capacitor formed by a thin insulator layer and an aluminum electrode. The aluminum electrode will be called the AC coupling electrode in this document.

In double sided detectors one anticipates applying the biasing voltage across the insulator. Since the SVXII detector will undergo radiation damage there is the possibility that the bias voltage will be increased during the lifetime of the sensors in order to reach full depletion. Therefore, we want to guarantee that the insulator will withstand over 120 V. The insulator between the implant and the Aluminum read-out strip consists of a 100 nm SiO_2 layer and a 100 nm Si_3N_4 layer. This thickness represents a good compromise between having a high breakdown voltage of the insulator (thicker insulator) and a large capacitive coupling C_c (thinner insulator). With these parameters the coupling capacitance is about ten time larger than the interstrip capacitance C_i allowing a good charge collection. We choose the oxide-nitride insulator technology because the probability that a pinhole in the nitride falls exactly in front of a pinhole in the oxide is extremely small leading to a smaller percentage of pinholes. The presence of an electron accumulation layer on the interface between the n^+-type strip of the n-side and SiO_2 requires an isolation scheme. For the SVX II detector the n^+ strips are isolated via p^+ implants. The specification for the SVXII detectors are shown in table 2.

Two different techniques are being pursued to bring the $r-z$ signals out on the same edge as the p-side strips. This is required both to reduce the mass in the sensitive area of the detectors and to facilitate cooling. The two techniques are :

- The double metal scheme where a thin insulation layer is deposited on the first metal layer. Contact holes (vias) allow electrical contact between the first and the second metal layer.
- The Z- interconnect where a printed circuit on a substrate routes the z-strips in such a way that they can be readout on the p end side.

Since there is a larger number of readout channels on the z side several n-strips are multiplexed together and readout by one electronic channel. An example of the multiplexing scheme for the double metal and the interconnect is shown in fig. 3. The choice of the multiplexing technique impacts on the final detector physics performance. The following factors have to be taken into consideration:

Table 2: Specification of the SVX II double sided detectors

Substrate		
	type	n-type Si
	thickness	$280 \pm 15\mu$m
	resistivity	$> 3000\Omega$-cm
Capacitances		
	AC coupling	10 pF/cm
Bias resistor		
	Polycristalline silicon	2 ± 1 MΩ
	bias voltage	45 ± 15 V
Voltage breakdown		
	Bulk	> 150 V
	AC coupling	> 120 V
n-side separation	type	p^+ implants
Maximum leakage current		< 250nA/cm^2 at V_b+10 V

- The position resolution is determined by the pitch and the Signal/Noise (S/N). The noise is made up of a parallel component and a series component. The parallel component is determined by the value of the bias resistors and the leakage current. A factor of $\sqrt{(N)}$ is expected in the case of multiplexing by N. The series component is determined by the characteristics of the amplifier and the input capacitance. The latter increases linearly with the number of strips connected together.
- Ambiguities occurs when several non adjacent strips are read out in parallel in a multiplexing scheme. They can result in incorrect track parameters if a track lies in the neighbourhood of the image hit and is associated with it.

We have started to perform a Monte Carlo study to determine the optimal multiplexing in order to minimize the effect of ambiguities. The multiplexing proposed in table 3 avoids three or four hit ghost tracks.

4.1 Glass - Kapton interconnect

The OPAL and L3 experiments have both been using the interconnect technique [7, 8]. The idea is straightforward: the signals on the z side are re-routed to the electronics via gold plated lines on a substrate. The choice of the substrate material must be such as to minimize multiple scattering and the cross talk between strips. The substrates that we are examining are glass and Kapton and their properties are presented in table 4. The glass is 50 μm borosilicate glass D263 which has excellent flatness and is easy to cut. The 50 μm thick Kapton is prepared by Polyonics [9]. From the parameters presented in table 4 we expect that the cross talk between the metal lines on the top of the interconnect is about twice as large for glass as for Kapton since the dielectric constants of Kapton and glass are 3 and 6.8 respectively. Nevertheless, the glass is more stable than Kapton against temperature and humidity changes.

The glass metallization and the gold plating has been performed by OPTIMASK [10]. The

Table 3: SVX II multiplexing.

Layer number	Multiplexing	Space between ghosts (cm)
0	4	4
1	3	5.3
2	3	5.3
3	2	8

Table 4: Properties of the substrates.

material	Glass	Kapton (E Type)
manufacturer	Schott D263	Polyonics
thickness (μm)	50	50
radiation length (cm)	12.7	21
Coefficient of Thermal Expansion (ppm/C)	7	17
Coefficient of Humidity Expansion (ppm/ % R.H)	small	9.
Dielectric constant	6.7	3

lines are made of sputtered Chrome and Gold. The thickness of the metal lines is about 1μm. The pad line geometry for the Kapton was digitized at Max Levy[11]. The circuit is etched on Kapton foils coated with 0.25 μm of nickel and 2.5 μm of copper. A layer of 0.7 μm of nickel and 0.5 μm of gold is then electro-plated.

We checked the feasibility of the two techniques on a circuit similar to OPAL. The prints were electrically tested to check for open/short. A defect rate of < 1.5 % was achieved by both companies. Bondability tests on glass were successful while the kapton presented problems that we have not yet solved.

4.2 Double metal

The realization of the double metal layer is largely dependent on the detector manufacturer. We are trying two different approaches with our prototypes. Sintef will use polyimide as an insulator between the two metal layers while Hamamatsu and Micron will use SiO_2. The specified thickness of the insulator is about 5 μm for all vendors.

5 Prototype detectors

We ordered prototypes detectors from Sintef, Micron and Hamamatsu. The design of the Sintef/ Micron prototypes is similar but not identical. The geometries of the p-side and n-side detectors are described in table 5 and table 6 respectively. The Hamamatsu geometry in table 7 is closer to the final detectors. Detector C and D are full size similar to layer 0 while A and B are half size layer 1. The passivation layer is polyimide and silox for Sintef and Micron respectively. Studying the behaviour of the detectors from Sintef and Micron will allow us to study the surface charge effects in polyamide and to determine if Silox is mechanically strong. It is known that it is possible to improve the resolution of the sensors without increasing the amount of electronics by interleaving each ac-coupled electrode pair with an implant which

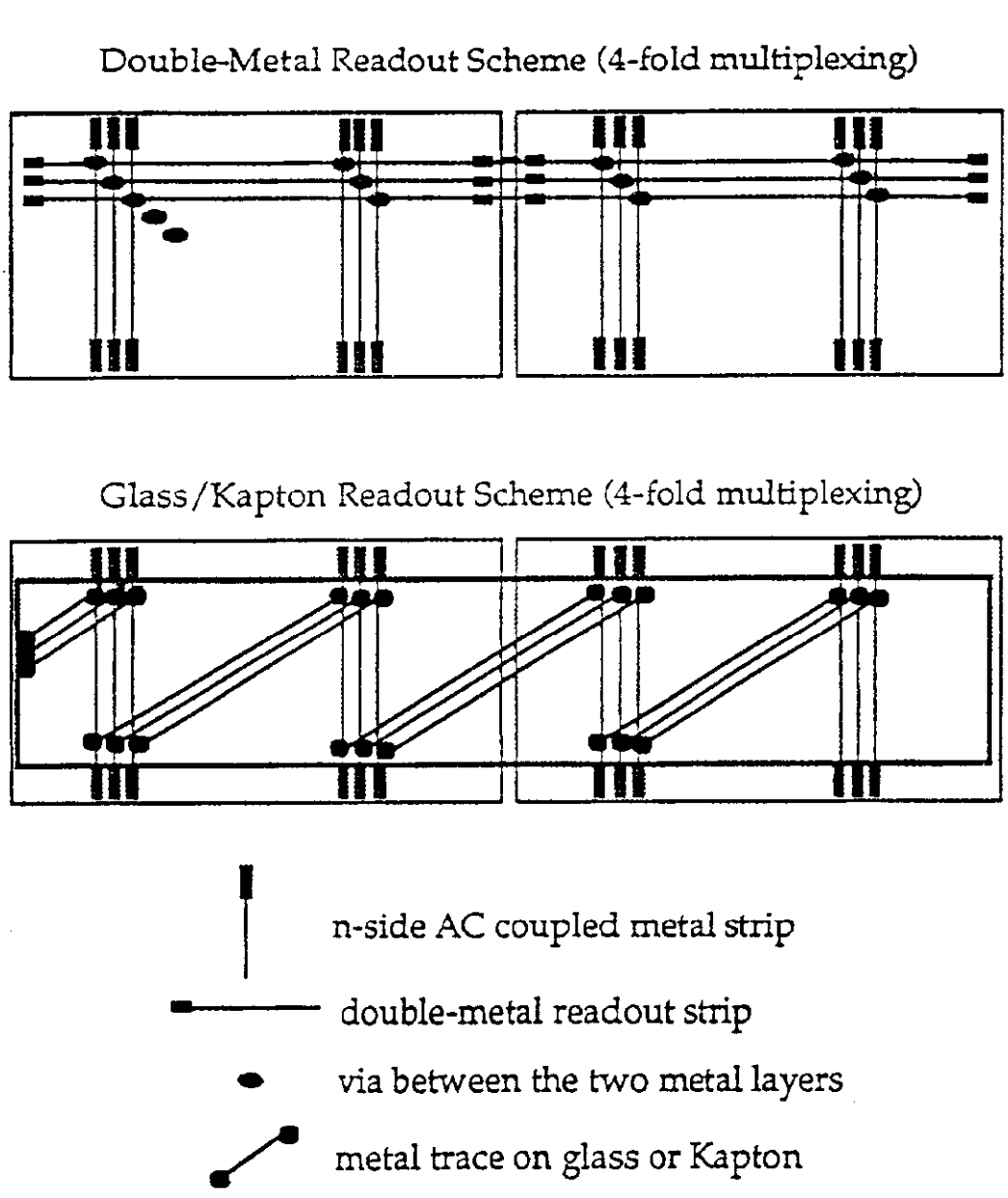

Figure 3: Schematic layout of the interconnect and the double metal.

Table 5: p-side geometry of the prototype detectors from Micron and Sintef.

detector	dimension (cm^2)	pitch μm	read-out pitch μm	$N_{channels}$
A	4.25 × 2.07	25	50	384
B	4.25 × 2.07	50	50	384
C	8.5 × 1.43	50	50	256
D	8.5 × 1.43	50	50	256

Table 6: n-side geometry of the prototype detectors from Micron and Sintef. The number in parenthesis refer to Sintef.

detector	pitch μm	read-out pitch μm	$N_{channels}$
A	103	103	384
B	103	103	384
C	80(79)	160(158)	512
D	160(158)	160(158)	512

Table 7: Geometry of the prototype detectors from Hamamatsu.

Parameter	Layer 0	Layer 1
Length(cm)	7.812	7.812
Width(cm)	1.804	2.649
N(ϕ) readout strips	256	384
N(ϕ) extra-strips	22	20
N(ϕ)	278	404
$r-\phi$ pitch (μmm)	60	60
N(z)	512	576
z pitch (μm)	149	132

is biased but not read out. These interleaved, non-readout implants are called "intermediate strips." The charge collected by these strips is transferred by capacitive coupling to the readout strip. Even if the use of intermediate strips is widespread at LEP, we will have to evaluate carefully the effect of the signal loss due to the presence of intermediate strips for SVX II since we already expect loss of signal and increase in noise due to radiation damage. Therefore, we have ordered prototype A and C to evaluate the intermediate strip design separately for the p-side and the n-side. All prototypes detectors came with the two different schemes of n-side read-out. One type bears the double metal structure. The second type is identical but for the absence of the thick insulator layer and second metal. The double metal technique is preferred for ease of assembly while the glass/kapton scheme is expected to have lower capacitance for the readout electronics and therefore better signal to noise.

In summary, the combination of prototype detectors that we have chosen will allow us to:

- study the effect of intermediate strips on the p and n-side separately
- compare the performance of double sided double metal detectors to double sided detectors with interconnects
- study different insulators in between the double metal layers and/or as a passivation layer.

6 Design issues

In the design of silicon detectors that have to operate in high radiation environments several issues become severe. We have tried in the design of the prototype detectors for SVX II to avoid some of the problems encountered by previous *R&D* projects and experiments.

6.1 Capacitance

One of the concerns is to maintain a low capacitance in order to have a good signal to noise. Here, we adopt the convention of denoting the total capacitance and the capacitance per unit length by a capital C and a small c respectively and we use some of the measurements from [13].

- Coupling capacitance

  The coupling Capacitance of the silicon detectors can be calculated using the parallel plate formula and by assuming the thickness of the SiO_2, Si_3N_4 to be equivalent to an SiO_2 thickness $t_{ox} = 270$ nm. Therefore :

  $$c_c = \epsilon\epsilon_0 w/t_{ox} = 3.9 \times 8.8 \times 10^{-2}\text{pF/cm} \times (8\mu\text{m}/0.270\mu\text{m}) = 10\text{pF/cm}$$

  where w is the implant width, ϵ_0 and ϵ are the permittivity constant of vacuum and SiO_2 respectively.

- p- side capacitance

  The total capacitance of the p-side is the sum of the interstrip capacitance c_i which is mainly due to the neighboring strips and the bulk capacitance c_b. The interstrip capacitance depends on the ratio between the width of the implant w and the pitch p:

  $$c_p = c_b + c_i = 0.75 + 1.8(w/p) = 0.75 + 1.8(8/60) = 1.04 \text{ pF/cm}$$

  In order to minimize the interstrip contribution we minimize w. Since in a ladder two detectors are electrically connected to give a length of 16 cm we can estimate the total

capacitance of the p-side is $C_p = 18 \pm 4$ pF before radiation damage. Radiation damage measurements predict that the p-side capacitance will increase by about 50 % after inversion to about 28 pF.

- n-side capacitance

  The contributions to capacitance of the n-side are the overlap capacitance between the two metal layer c_{cross}, the interstrip capacitance c_{imp} between the lines of the first layer, the intertrace capacitance c_{trace} between the metal lines of the second layer and the bulk capacitance. The overlap capacitance between the two metal layers has been measured on prototypes built by Hamamatsu for the Delphi experiment to be $c_{cross} = 0.0023$ pF/N_{cross}. For our prototypes $N_{cross} = 2048$ and therefore we expect C_{cross}= 4.7 pF. The interstrip capacitance and the intertrace capacitance have been measured to be c_{imp}= 1.5 pf/cm and $c_{trace} = 0.25$ pf/cm. Therefore, defining $C_{int} = C_{imp} + C_{trace}$, we obtain:

$$C_{int} = 4(1.5 \text{ pF/cm} \times 1.5\text{cm}) + 0.25 \text{ pF/cm} \times 16\text{cm} = 13\text{pF}$$

  where the factor of four arises from the layer 0 multiplexing. The capacitance to the back-plane $c_{back} = 0.5$ pf/cm

$$C_{back} = 2(0.5 \text{ pF/cm} \times 1.5 \text{ cm}) = 1.5 \text{ pF}$$

  Therefore we expect a total capacitance on the n-side of $C_n = 19.2$ pF. Since, the calculations of the n-side capacitance have always yielded smaller values than the measurement we arbitrarily increase the previous estimate by 20% to $C_n = 23 \pm 4$ pF. We expect that the capacitance of the n-side will improve after inversion to 19 pF.

6.2 Radiation hardness

The R&D studies in preparation for the LHC and the SSC [14, 12] and the measurements taken during the operation of the SVX detector offer some guidance about the damage to silicon due to radiation exposure. The effects that are known are:

- In n-type silicon radiation causes the removal of donors and the creation of acceptors, which results in type inversion from n-type to p-type at $\Phi_{inv} = 2 \times 10^{13}$ particles/cm^2
- The increase of the effective dopant concentration. Since the effective depletion voltage V_b is proportional to N_d the operation of the detector requires a higher V_b after inversion and this can cause the possible breakdown of the integrated coupling capacitors
- The increase in interstrip capacitance and the reduced signal to noise
- The creation of carrier-trapping centers in the bulk which reduce the collected charge (< 10 %)
- An increase in leakage current due to bulk damage

Recently two component annealing and anti-annealing have been observed. The two processes have different time constants and the time constant has been found to be dependent on the temperature. Cooling the detectors to below 10°C slows the annealing process and essentially stops the anti-annealing [15].

We can estimate the dose and the leakage current for the SVX II detector using the measurements taken during the operation of the SVX[16]. The SVX group reported [17] a dose rate of approximately 0.35 krad/pb^{-1} at $r_0 = 2.99$ cm in Run Ia after the Tevatron commissioning. From this rate it is possible to extrapolate to 1 fb^{-1} of data and to the SVX II layer 0 radius of 2.416 cm.

$$\Phi_{\rm SVX} = 0.35\ {\rm Mrad/fb^{-1}}\ \times\ 1\ {\rm fb^{-1}} \left(\frac{2.99}{2.416}\right)^{1.7} = 0.6\ {\rm Mrad} = 2\ \times\ 10^{13}\ {\rm MIPs}/cm^2. \quad (1)$$

The fluence $\phi_{\rm invert}$ necessary for type inversion using protons has been measured to be between $7.5 \times 10^{12}\ p^+/{\rm cm}^2$ [18] and $1 \times 10^{13}\ p^+/{\rm cm}^2$ [14]. Therefore SVX II could experience type inversion in layer 0 during run II. This is a conservative estimate because it is based on the fluence required to invert the n-bulk silicon using protons, which are approximately twice as damaging as pions.

The measured change in the SVX leakage current during 30 ${\rm pb^{-1}}$ of data was 2 nA/krad or about 1 ${\rm nA/pb^{-1}}$ at room temperature. Therefore, we expect an increase in the leakage current in SVX II of about 1 μA after 1 fb^{-1} of data since even if layer 0 of the SVX II is closer to the beam pipe the length of a strip (2×8 cm) is shorter than SVX (3×8.5 cm). The predicted value of the leakage current after radiation implies that for 100 V applied bias, each strip, would draw 100 μW which is a significant amount of heat for the gas to dissipate. The severity of the increase in leakage current with luminosity may prove to be a limiting factor and the inner layers of SVX II may require replacement before type inversion is reached due to the excessive leakage currents or the operation of the detectors at low temperature. In fact, the leakage current increases by a factor of two for a 7.5°C rise in temperature.

6.3 Signal to Noise

Special attention must be given to the signal to noise ratio when working with silicon microstrip detectors. The most probable charge deposited in a 300 μm thick detector is about 22000 electrons and there is no multiplication. Furthermore, tracks at large angle share their charge over a large number of strips. Several components contributes to the noise. The electronic noise is the sum of a constant term and a term which depends on the detector itself. The main contribution to the detector dependent term comes from the capacitance of the strip to its neighbour and to the back plane which acts as a load capacitance on the amplifier. The electronic noise is given by :

$$ENC = A + B \times C_{input}$$

where A and B depend on the read-out chip amplifier. The measured equivalent input noise due to electronic noise and detector capacitance for the radiation soft version of the SVX II chip [19] is shown in table 8. On the p-side we can expect at the beginning of the run a capacitance of about 20 pF and ENC= 1690. This will worsen to a capacitance of about 30 pF and a ENC = 2300 after inversion.

For AC-coupled detectors such as SVX II the leakage current will not saturate the front-end chip. However, the shot noise equivalent in electrons $Q_{\rm shot}$, seen by the input of the amplifier for a simple CR-RC filter is given by[20]:

$$ENC_{shot} = \frac{e}{q} \times \sqrt{\frac{qI_{\rm leak}\tau_{\rm p}}{4}} \quad (2)$$

where e is the natural logarithm base, q is the electron charge, $I_{\rm leak}$ is the strip leakage current and τ_p is the peaking time which we can assume to be equal to the integration time. For SVXII, assuming $\tau_{\rm int} = 100\ ns$ and $I_{leak} = 1.00\ nA$ before irradiation we obtain:

$$ENC_{\rm shot} = 2.7 \times \sqrt{\frac{1\ nA \times 100\ ns}{4 \times 1.6 \times 10^{-19}\ {\rm C}/e^-}} = 33\ e^- \quad (3)$$

After 1 fb^{-1} of data assuming $I_{leak} = 1\ \mu A$ we obtain:

$$ENC_{\rm shot} = 2.7 \times \sqrt{\frac{1\ \mu A \times 100\ ns}{4 \times 1.6 \times 10^{-19}\ {\rm C}/e^-}} = 1070\ e^- \tag{4}$$

Table 8: Rad soft SVX II front end chip measured input noise

$C_{\rm input}$ (pF)	$\tau_{\rm rise}$ (ns; 10 % to 99 %)	$Noise_{\rm input}$ ENC
10	105	1020
10	170	860
10	320	780
20	105	1690
20	170	1350
20	320	1250
30	105	not measured
30	170	1870
30	320	1760

The contribution of the bias resistor due to Johnson noise can be calculated using:

$$ENC_{\rm Johnson} = \frac{e}{q}\sqrt{\frac{\tau_p kT}{2R}} \tag{5}$$

where k=1.381 $\times$ 10$^{-23}JK^{-1}$ and T is the temperature. Since the specification of SVXII requires R = 2 MΩ:

$$ENC_{\rm Johnson} = \frac{2.7}{1.6 \times 10^{-19}\ {\rm C}/e^-}\sqrt{\frac{1\ {\rm ns} \times 1.381 \times 10^{-23}JK^{-1} \times 293^\circ\ K}{2 \times 10^6\ \Omega}} = 178\ e^- \tag{6}$$

Therefore, the contribution of the Johnson noise is always negligible while the noise due to the leakage current is a factor after the detectors are irradiated. Adding the contributions of $ENC_{\rm Johnson}$, $ENC_{\rm shot}$ and $ENC_{\rm input}$ in quadrature we obtain

$$ENC = \sqrt{(178\ e^-)^2\ +\ (1070\ e^-)^2\ +\ (2300\ e^-)^2} = 2543\ e^- \tag{7}$$

after irradiation. Note that we assumed that the noise for the 30 pF input capacitance for τ_{rise}= 105 ns is about 20 % higher than for the 200 ns measurement as is the case for input capacitance of 10 and 20 pF. From this number we can conclude that the signal to noise on the p-side will degrade from about S/N=22000/1700=11.8 at the beginning of the SVX II operation to S/N =22000/2543 = 8.6 after 1 fb^{-1} where we have not considered possible reduction of the signal due to radiation effects and charge sharing.

6.4 Depletion Voltage

In the design of the detector we took into account the dependence of depletion voltage V_d on the geometry. The depletion voltage V_{D_0} is given by:

$$V_{D_0} = t_d^2/(0.53)2\rho$$

Table 9: Dependance of the effective voltage.

pitch (μm)	implant width (μm)	f(w/p)	p/t_d	V_d/V_{d_0}
50	10	0.4	0.17	1.13
50	20	0.2	0.17	1.07
60	12	0.4	0.2	1.16
100	10	0.7	0.33	1.46
100	20	0.4	0.33	1.26
100	30	0.26	0.33	1.17
150	15	0.7	0.5	1.70
150	30	0.4	0.5	1.40
150	50	0.26	0.5	1.26
200	20	0.7	0.67	1.94
200	40	0.4	0.67	1.54

Table 10: Geometry of the implants and read-out strips.

element	width μm	thickness μm
p-side implant	10.5	
p-side Al strip	8	1.2
n-side implant	11.5	
n-side Al met 1	8	1.5
n-side Al met 2	7	1.2

where ρ and t_d are the resistivity and the thickness of the bulk silicon respectively. The effect of the finite pitch and width is to increase the effective depletion voltage and decrease the body capacitance according to:

$$V_D = V_{D_0} \times (1 + 2(p/t_d)f(w/p))$$

where p is the pitch, w is the width of the implants and f is a function which depends on p and w [21]. The dependence of the effective depletion voltage from the geometry is illustrated in table 9. It is clear that since the depletion voltage has to increase during the run because of radiation, we must specify p and w such that the effective depletion voltage is close to the ideal value. This concern is reflected in the smaller n-side pitch of the Hamamatsu prototype detectors.

6.5 Microdischarges

In AC coupled double sided detectors the coupling capacitance must withhold full voltage. It was observed in [22] that a steep increase in the leakage current and noise occurred at low-reverse bias voltages. These discharges are due to the large potential difference between the

external electrode and the implanted strip which result in a strong fields at the edge of the strip inside the silicon substrate. The calculated field strength in the silicon as a function of the edge separation between the external electrode and the implant [22] is shown in fig. 4. If

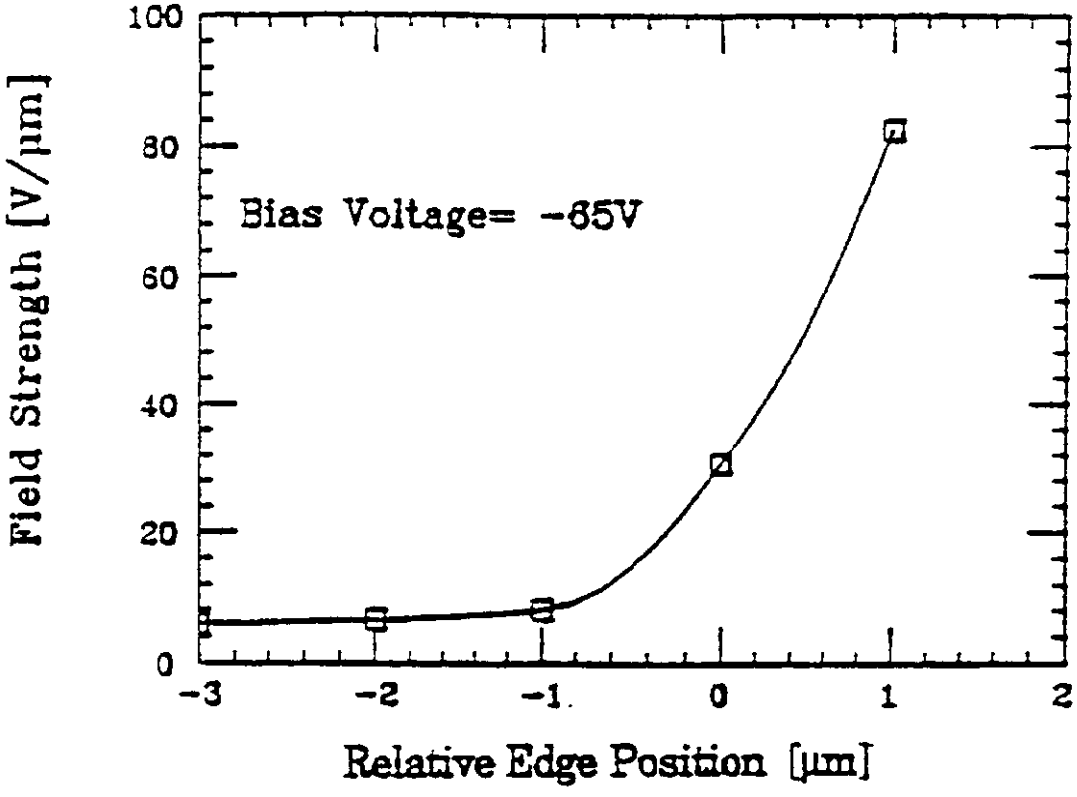

Figure 4: Field strength around the implant as the function of the edge separation between the Al readout strip and the implant

the edge of the Aluminum read-out strip is placed on the edge of the implant the field at the SiO_2 interface is about 35 V/μm which exceeds the breakdown voltage of silicon. The effect is minimized if the edges of the electrode are stepped back by at least one micron from the edge of the implant. Therefore, we have designed our detector to satisfy this criteria as shown in table 10.

7 Schedule

The prototype detectors from Sintef and Micron are expected at the end of June 1994 while Hamamatsu will deliver their sensors in the middle of October 1994. Systematic studies of i-V, C-V, $V_{breakdown}$, R_{bias}, $R_{interstrip}$, $C_{interstrip}$, C_{tot}, resolution will be performed on the prototype detectors. We will be able to evaluate the performance of n-side intermediate strip, double sided double metal detectors versus double sided detectors with glass/kapton interconnect and the effect of different passivation layers. Radiation tests on all components are important to guarantee a good performance of the detector. Therefore, radiation runs at TRIUMF are planned for September 94 and February 95. Subsequentally, beam tests at KeK are planned for December 94 and March 95. After re-evaluation of the prototype detector exposed to radiation and measurement of the resolution we will decide the optimal geometry and technology for the production detectors. We expect to order the production detectors at

the end of 1995 and that their delivery will take about one year. That will allow one year for ladder construction and installation for Run II which is predicted to start in the summer of 1998.

8 Conclusions

The design and R&D for a new microstrip detector for run II of the Tevatron has begun. The SVXII detector incorporates various improvements upon the SVX design:

- two dimensional read-out capability
- twice the longitudinal length of SVX
- smaller inner radius
- larger ratio of the outer layer to inner layer radii
- smaller inactive region between the barrels

These features will improve the tracking performance and increase the physics capability of the CDF detector. The design and operation of this detector will give important information to the construction of silicon detectors for the LHC. In fact at the expected luminosity of the main injector (10^{32} cm^{-2} s^{-1}) the radiation level for the innermost layer at about 2.5 cm is similar to the one expected for silicon trackers at the LHC (10^{34} cm^{-2}s^{-1}) at a radius of about 20 cm[23].

9 ACKNOWLEDGEMENTS

This work was supported by a grant from the United States Department of Energy under contract number DE-FG02-19ER40681 Task G, the Sloan Foundation and the NSF. I would like to thank all members of the SVX II design team

References

[1] F. Abe *et al.*, *Evidence for top quark production in $p\bar{p}$ collisions at $\sqrt{s}$ = 1.8 TeV* Fermilab-Pub-94-116-E submited to *Phys. Rev. Let.*

[2] S. Wagner *et al.* , *Phys. Rev. Lett.* **64**, 1095 (1990); P. Abreu *et al.* , *Z. Phys.* C**57** 181 (1993); D. Buskulic *et al.* , CERN PPE/93-42 to be published in Phys. Lett. B; D. Buskulic *et al.* , *Phys. Lett.*B **314**, 459 (1993); P. D. Acton *et al.* , CERN-PPE/93-33.

[3] F. Abe *et al.* , *Measurement of the B_s lifetime at CDF*, CDF/PUB/BOTTOM /PUBLIC/2613.

[4] *Expression of interest in a future collider detector in B0* CDF/DOC/ADVISORY /PUBLIC/2436.

[5] N. Bacchetta *et al.*, *SVX II Upgrade Proposal &Simulation Study* CDF/DOC /SECVTX/CDFR/1922 (January 1993).

[6] Ratzman, Paul *Analysis of ladder support fiber options* unpublished.

[7] G. Ambrosi, "The development of the Kapton signal router for the silicon microvertex detector of L3"

[8] O. Runolfsson, "A silicon microstrip vertex detector with two coordinate readout for the OPAL experiment

[9] Polyonics Corp., Newbury, MA (U.S.A.)

[10] OPTIMASK, Morangis, France

[11] Max Levy Autograph, Inc., Philadelphia, PA (U.S.A.)

[12] N. Tamura *et al. Nucl. Inst. and Meth.* **A 342**, 131, 1994.

[13] T. Ohsugi talk at the SVX II meeting.

[14] A. Holmes-Siedle *et al.* , *Radiation Tolerance of Single-Sided Silicon Microstrips*, CERN-PPE/93-137, submitted to *Nucl. Instr. and Meth.*, (July 1993).

[15] H. J. Ziock *et al.* , *Nucl. Inst. and Meth.* **A 342**, 96, 1994.

[16] N.M. Shaw contribution to this conference and M. Frautchi CDF/DOC/ SECVTX/PUBLIC/2368.

[17] D. Amidei *et al.* , *Status of Radiation Damage to the SVX detector* CDF/SVX/ DOC/PUBLIC/2061.

[18] H. J. Ziock *et al.* , *IEEE Trans. on Nucl. Sci.*, **40**, Number 4, 344 (1993).

[19] Zimmerman, T. and Yarema, R. *et al. SVX II Design Group Chip Performance Review.* Unpublished (October 1993).

[20] E. Nygard *et al.* , *Nucle. Inst. and Meth.* **A301**, p. 506, (1991).

[21] E. Barberis *et al.* , *Nucl. Inst. and Meth.* **A342**, 90, (1994).

[22] T. Ohsugi *et al.* , *Nucl. Inst. and Meth.* **A342**, 23, (1994).

[23] J. Spalding contribution to the Elba conference 1994.