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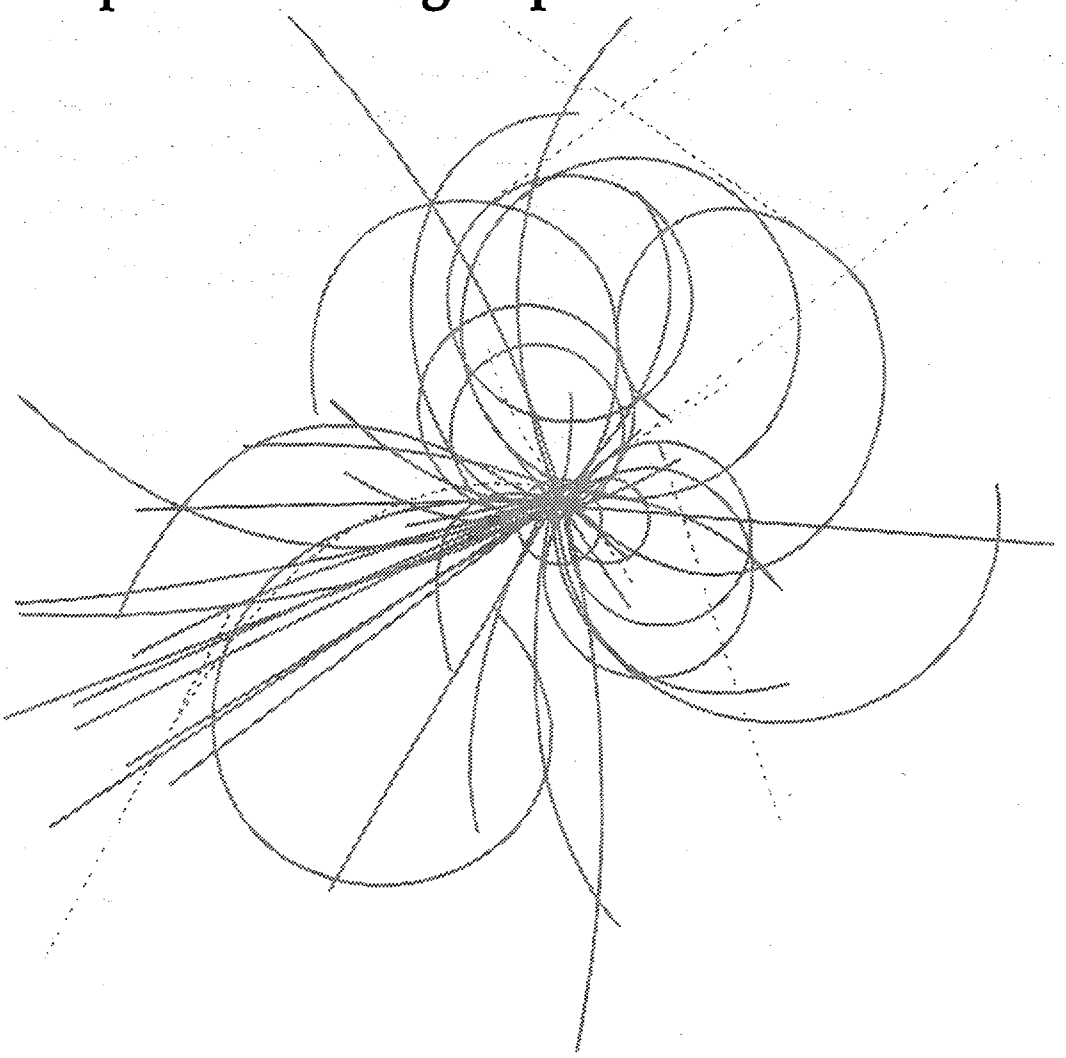
Superconducting Super Collider Laboratory



A Method to Quench and Recharge Avalanche Photo Diodes for Use in High Rate Situations

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T. O. Regan, H. C. Fenker, J. Thomas, and J. Oliver*

Superconducting Super Collider Laboratory†
2550 Beckleymeade Ave.
Dallas, TX 75237

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*Harvard University High Energy Physics Lab, Cambridge, Massachusetts.

†Operated by the Universities Research Association, Inc., for the U.S. Department of Energy under Contract No. DE-AC35-89ER40486.

A METHOD TO QUENCH AND RECHARGE AVALANCHE PHOTO DIODES FOR USE IN HIGH RATE SITUATIONS

Thomas O. Regan, Howard C. Fenker, and Jennifer Thomas
Superconducting Super Collider Laboratory*
2550 Beckleymeade Avenue
Dallas, Texas 75237

John Oliver
High Energy Physics Laboratory
Harvard University
42 Oxford Street
Cambridge, Massachusetts 02138

Abstract

We present a new method of using Avalanche Photo Diodes (APDs) for low level light detection in Geiger mode in high rate situations such as those encountered at the Superconducting Super Collider (SSC). The new technique is readily adaptable to implementation in CMOS VLSI.

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INTRODUCTION

Because of their small size, high quantum efficiency, and low operating voltages, APDs are desirable for use as low-level light detectors in High Energy Physics (HEP) experiments. As well as simply replacing photo multiplier tubes in many conventional applications, APDs are especially interesting as transducers in high density, large channel count systems using scintillating fibers, such as those being considered for SSC detectors.[1]

To date, APDs have seen applications in HEP experiments only in test situations requiring a modest number of devices.[2] This is primarily due to their low gain and high gain dispersion when operated in "linear" mode (bias below breakdown voltage, V_{br}) and their slow recovery time (a microsecond or more) in Geiger mode (bias above V_{br}). This slow recovery time is particularly unfortunate because APDs operated in Geiger mode are very attractive photon detectors in many other respects: their response time is of the order of 1 ns, a single photon can initiate an avalanche that directly yields a signal of at least 100 mV, and the noise rate is acceptably low when the APD signals are read in coincidence with a trigger.

PASSIVE OPERATION OF THE APD

An APD is normally operated reversed biased at several thousand volts per millimeter. This field varies with device type and is higher in the multiplication region than in the collection region.[5] When a photon strikes the silicon, an electron/hole pair is knocked from the valence band into the conduction band, and the electron is accelerated toward the cathode. This free electron undergoes multiple collisions with the silicon lattice and quickly attains a limiting velocity. As a result of one of these collisions, another electron may be promoted to the conduction band as well. In Geiger mode ($V_{bias} > V_{br}$), the mode of interest for this report, additional electron/hole pairs are produced by the holes propagating toward the anode and, possibly, by photons produced in the collisions. Thus initiated, the cascade continues until the voltage across the device decreases below the breakdown point, and the current through the APD falls below the breakdown point and the current through the APD falls below some critical value, typically about 50 μA. This quenching of the avalanche is in fact a complicated process within the APD itself. From a practical point of view, however, it can be viewed as the result of the signal flowing through an external resistor to produce a voltage that decreases the bias across the diode to the point at which the avalanche ceases and the APD starts recharging (Figure 1). The

APD used in the development of the circuit described here is an EG&G[3] type C30902S. Its diameter is 0.5 mm, and its breakdown voltage is of order 200 V.

While the avalanche and recharge cycle is in progress, the APD is effectively dead as a photodetector (on the order of microseconds), imposing a serious rate limitation problem. One can vary the recovery rate somewhat by choosing different values for the series resistor. However, if the value is made too low then the diode current becomes excessively high and the avalanche may continue until the junction is destroyed.

METHODS TO QUENCH AND RECHARGE THE APD JUNCTION

Figure 2 shows a circuit that has been used to recharge the junction in less than 5 ns. While this recharging was fast, we observed the device immediately after firing nearly all of the time. This seemed to indicate that the junction of the APD still had free electrons available to start more avalanches.

An effort was made to electronically clamp the avalanching APD to a level below V_{br}. A PNP transistor circuit was configured to act as a switch, clamping the anode of the APD to +5 V when an avalanche was detected (Figure 3). This clamping action would, in about 5 ns, force the junction 4 V below the bias voltage, which was nominally set 1 V above the V_{br} given for the device by the manufacturer.

Using the trigger output from a light pulser as a trigger source for a dual-pulse generator (Figure 4), a sequence of two pulses was generated. The first, a negative-going pulse of +5 V to ground, would switch on the PNP clamp transistor, creating the quenching pulse. The second, a positive-going TTL pulse, would activate the recharging circuit. The results were encouraging, as there was a large reduction in the after-firing rate. However we were able to process only one avalanche signal per flasher trigger with this setup, and we could not investigate double pulse sensitivity or resolution.

THE WORKING SYSTEM

The elements of the active quench and recharge circuit are shown in Figure 5. The APD is biased a few volts above V_{br} with a high-value resistor in series with the anode lead to ground. In

the normal state, both the PMOS and the NMOS transistors are turned off. As the current in the APD is near zero, the voltage at the anode is a few millivolts. When a Geiger breakdown occurs, a comparator set at a threshold of order 50–100 mV fires, triggering the sequential generation of quench and recharge pulses.

The quench pulse turns on the PMOS FET, which clamps the anode of the APD to +5 V. Thus the voltage across the APD is quickly reduced to a value below V_{br} and the Geiger avalanche is quenched. Following the quench pulse is a recharge pulse that turns on the NMOS device, returning the APD anode to ground and recharging the junction. The APD is then armed to detect the next light pulse.

As shown in Figure 6, we designed a closed-loop system using a tri-state CMOS gate—in this case a SN74HC365—in place of the PNP transistor and the DMOS FET (Figures 2 and 3). In the quiescent state, the tri-state gate is disabled, which turns off both the output PMOS and NMOS devices and results in a high impedance state. On detection of a Geiger avalanche, the AD9696 comparator enables the tri-state gate, and with the gate input high the PMOS device turns on and quenches the APD. With the gate still enabled, the delay network causes the input to go low, which turns on the output NMOS transistor and recharges the APD. The tri-state gate then returns to its high-impedance condition since the recharging causes the comparator to drop below threshold.

As seen in Figure 7, the signal was easily detected at 50 mV, at which point the comparator was triggered. After approximately 17 ns, the +5 V quench signal is observed, staying up for about 15 ns followed by the reset edge. The "on" time for the quench and recharge signals is determined by the RC time constant set by R1-C1. The 74HC365 has fairly long propagation delays associated with it: T_{ena} = 48 ns, and T_{pd} = 24 ns, both for a 50 pF load, as specified by the manufacturer.[4]

To address the problem of afterfiring of the APD, we experimented with the width of the quenching pulse. We found that a quench pulse as short as 15 ns was sufficient to practically eliminate afterfiring. We note that for this test it was extremely important to use a light source that emits all of its light in a short burst. We were finally able to probe the operation of the APD only after switching from a pulsed LED source to a pulsed laser diode. Pulsing an LED with a short current spike (5 ns) causes it to continue to produce light for 100 ns or more while the laser diode more accurately follows the applied electrical signal.

CONCLUSIONS

We have designed, built, and tested a circuit that can enhance the performance of an APD in Geiger mode so that it can respond to two light flashes less than 50 ns apart. This has important implications for detectors using scintillating fibers, or bulk scintillator readout via fibers, in very-high-rate environments such as the SSC.

It is probable that the cycle time could be improved through the use of custom CMOS devices. With reduced gate delays it appears likely that the system would be ready for use after 30 ns, assuming 15 ns is used for quenching, 5 ns is used for recharging, and the remaining time is allotted to internal gate delays. The prompt signal from the comparator could be used as a trigger edge for data acquisition systems.

Although the concepts of quenching and recharging have been investigated by others,[5] the circuit described here is an initial demonstration of a self-triggered system employing active quenching and recharging that is stable, is simple enough for application in a large system, does not have the propensity to damage the APD, and is easily implemented using a few readily available electronic components.

Presently, a multi-channel custom CMOS chip has been designed at the SSC Laboratory[6] and is being fabricated.

ACKNOWLEDGEMENTS

We wish to thank Mitch Wright for his fine work on the many iterations the prototype circuit underwent, and Charlotte Tatsch for her thoughts and conversations relating to the physics of the APD that provided the impetus for the quench design.

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[6] VLSI Design Group, Experimental Physics Department, MS-2000, SSC Laboratory, Dallas, Texas 75237.

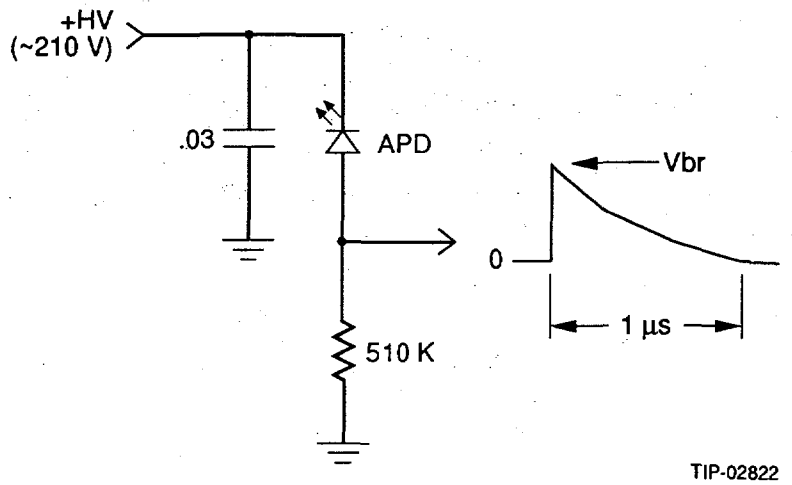

Figure 1. Passive resistor quenching.

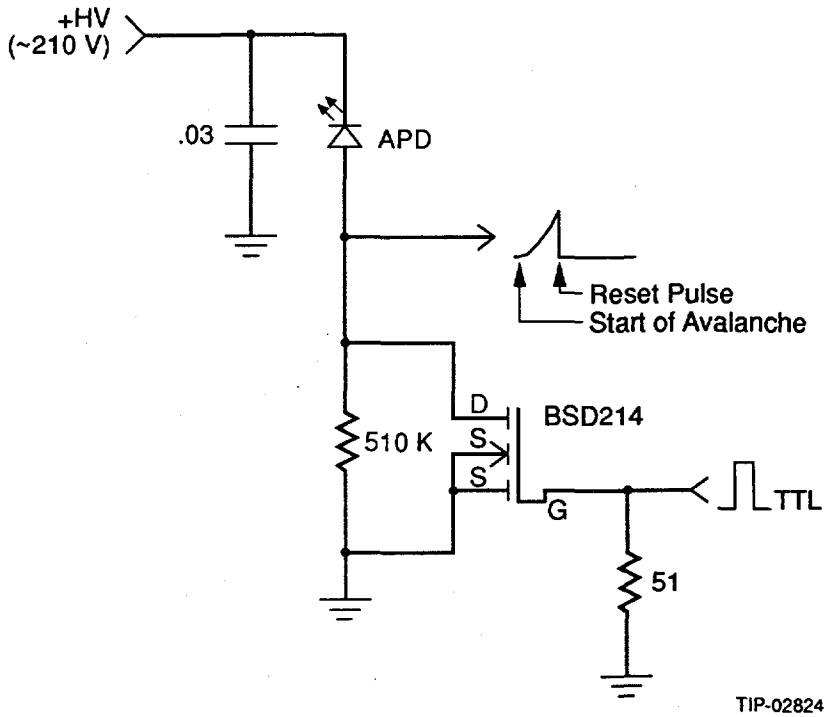

Figure 2. Recharge circuit using Phillips BSD214 DMOS FET.

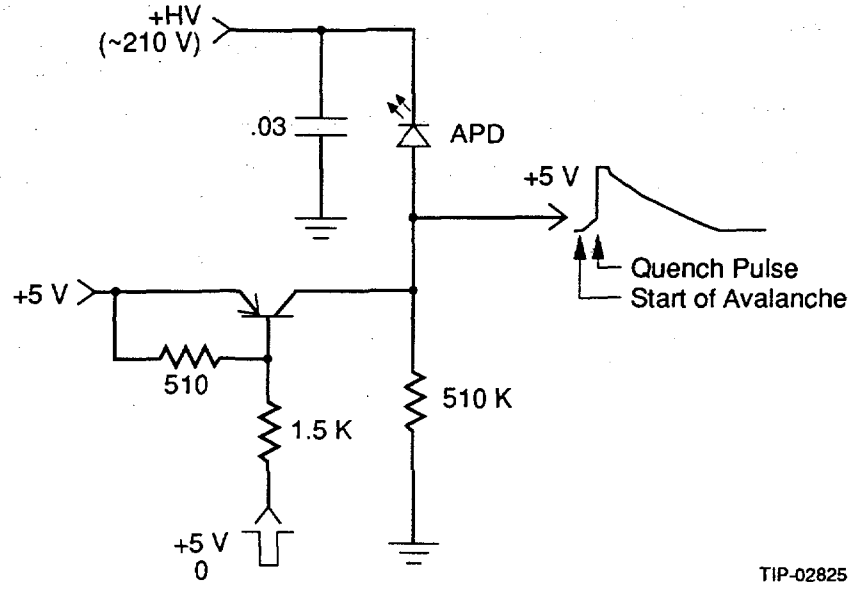

Figure 3. Quench circuit using pnp switching transistor.

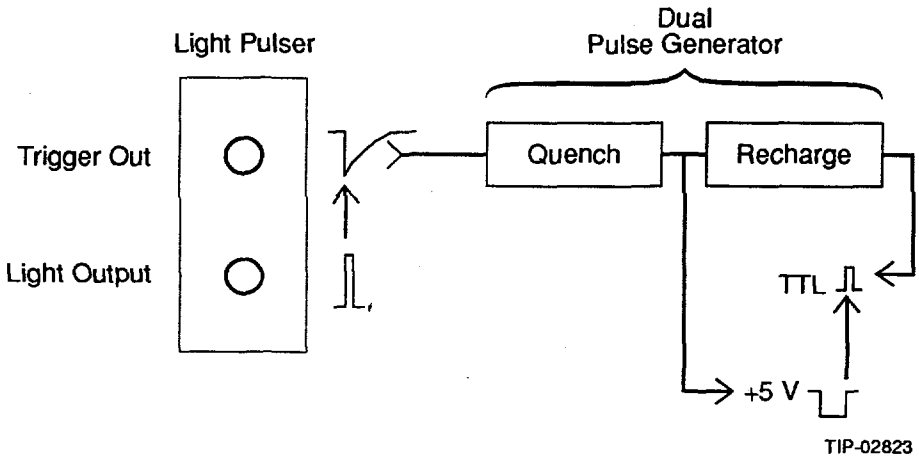

Figure 4. Light pulser and dual pulse generator.

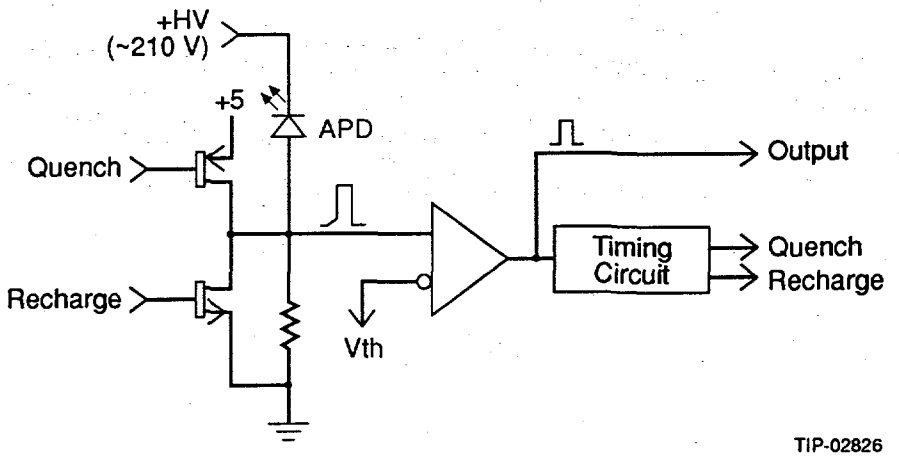

Figure 5. Use of CMOS for quenching and recharging.

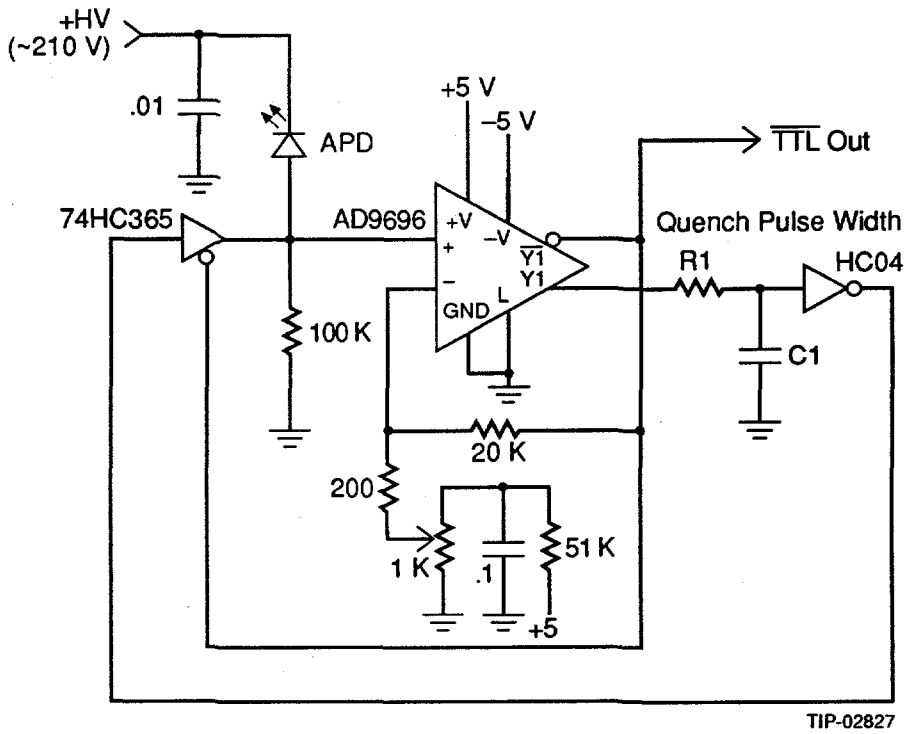

Figure 6. Working schematic for quenching and recharging the APD.

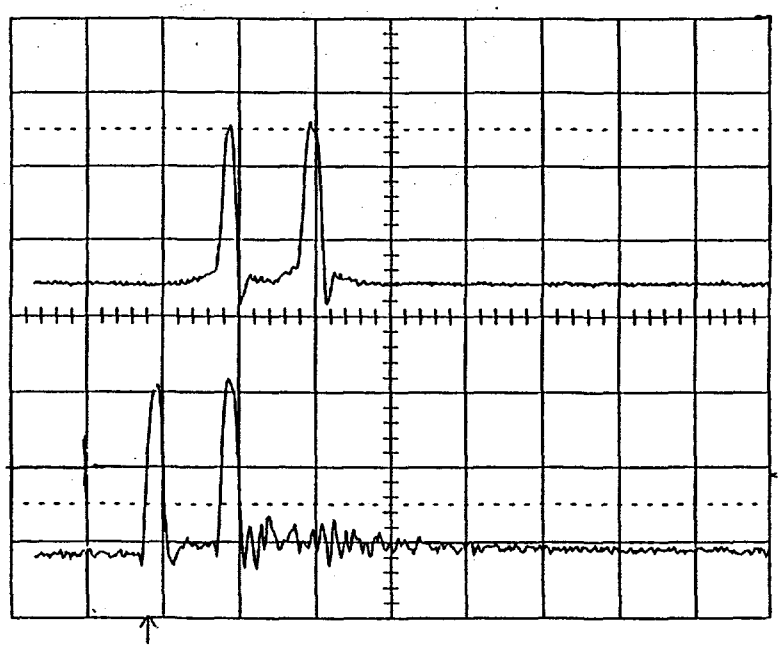

Figure 7. Top trace shows signal, quench and recharge waveform at APD anode. Bottom trace shows pulsed laser diode waveform. Horizontal divisions are 50 ns.