KEK Report 96-3
May 1996
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KEK--96-3
JP9609022

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Performance Evaluation of a High-Bandwidth Timing Module

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Abstract

The ability to generate highly precise timing signals is essential for the operation of particle accelerators, particularly so in future linear colliders. As a tool to generate precise fixed delays, a module called TD-2.1 has been developed for use at the ATF (Accelerator Test Facility). TD-2.1 is an improved version of a previous module called TD-2, developed for the TRISTAN accelerator [1, 2]. The new version can be used at clock frequencies of up to 1.5 GHz, almost three times the bandwidth of the previous version. Since TD-2.1 is applied in many places to synchronize the ATF accelerator operation, high reliability and stability (low jitter) are essential. The long-term stability and timing jitter of the module were evaluated. The jitter was found to be around 5 ps within the operating range. Stable operation of the module was verified in long-term tests.

Keywords: timing, jitter, delay

1. Programmable Delay Module, TD-2.1

TD-2.1 is a module that generates programmable delays from an incoming trigger pulse by counting the incoming clock pulses. It is typically used to synchronize accelerator components to the RF base frequency of the accelerator or to generate start pulses for data acquisition at a fixed time relative to the beam. TD-2.1 can also be used to synchronize the input clock with an unsynchronized start pulse. Regardless of the phase of the start pulse the output pulse is always synchronized with the input clock.

A block diagram of the TD-2.1 module is provided in figure 1. The required delay as a number of clock cycles is stored in a register (CAMAC data register), from which it is loaded to a high-speed up/down counter. The counter operation is started by a trigger signal (START). The counter then counts clock cycles down from the set value and gives an output pulse (Trigger Out) when the count reaches zero. The counter is reloaded at this point to give a continuous series of output pulses.

The 13-bit counter comprises a one-bit prescaler and three 4-bit up/down counters in cascade. The input clock is first divided by two with the prescaler (11C70) and fed into the 4-bit counters (ECL, 100136, 10136). The maximum achievable delay is thus 8192 clock pulses. At 714 MHz input clock frequency this corresponds to (8192 * 1.4 ns =) 11.47 μs.

2. Measurements

The objectives of this evaluation were to confirm the proper operation and to evaluate the jitter of the trigger output of the TD-2.1 module. Timing jitter means here the uncertainty of the time interval between the input trigger and the output pulse. The jitter can thus be measured as the variation of the delay length. By measuring the delay length several times, the jitter can be deduced from the statistical properties of the data. The standard deviation (σ) of the delay length distribution is used here to represent the timing jitter values.

The measurement setup is shown in figure 2. To measure the jitter, we used the TD-2.1 output pulse to trigger the oscilloscope. The output signal should then be in constant phase relative to the clock signal. By histogramming the zero-crossing (or any constant phase) times of the clock signal, the phase difference of the clock and the trigger is measured, and gives the delay values. The statistical variation of the delays then gives us the jitter value (figure 3). This method relies on the assumption that the counters operate properly. The validity of this assumption was verified in the reliability measurement, presented later in this report.

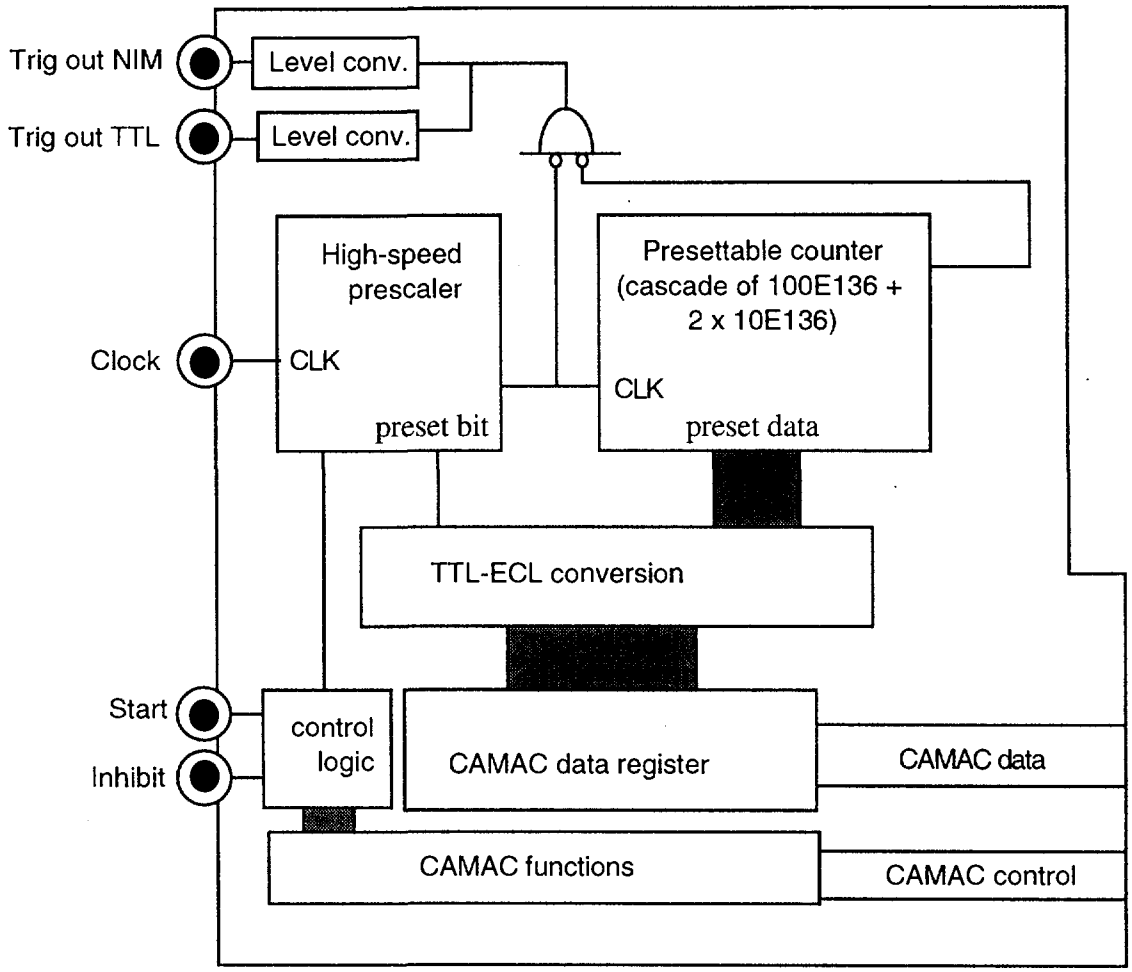

Figure 1. Block diagram of TD-2.1

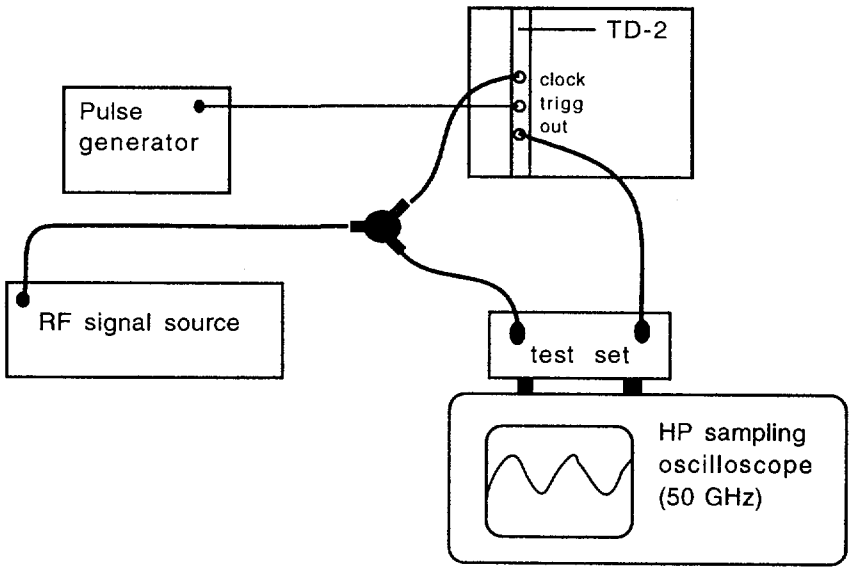

Figure 2. Setup for the jitter measurement

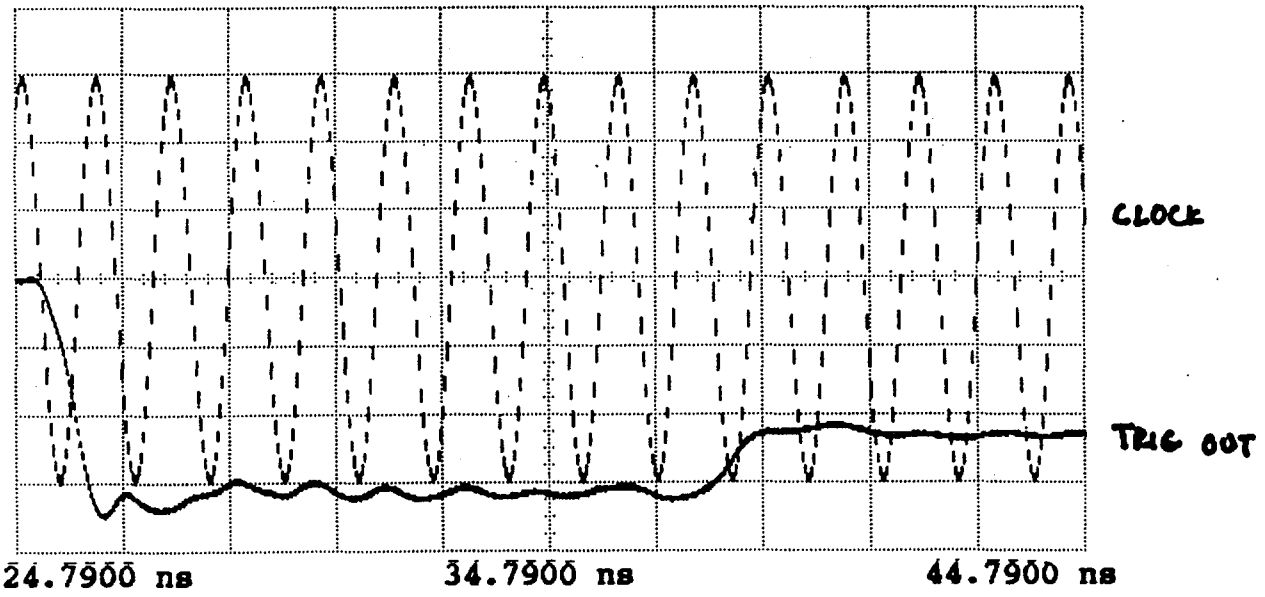

Figure 3. Jitter measurement of the clock signal

The time-interval resolution of the digitizing oscilloscope (HP54124T) used in the measurements is quoted by the manufacturer to be 0.25 ps. To establish the accuracy limit of this method, a measurement in which the same clock pulse was fed into both the trigger and the input channels was made. Ideally, the jitter value should then be zero. The factors that contribute to the measured jitter in this case are: 1) the triggering accuracy of the oscilloscope, 2) the hardware used, e.g. the power splitter and 3) the properties of the RF signal generator. The contribution from 1) is the largest since the slope of the triggering pulse is relatively slow compared to the bandwidth of the oscilloscope. The jitter value (σ_T) for a 1 GHz input signal was found to be 1.1 ps. For these measurements this method is sufficiently accurate.

The distribution of the phase difference at 714 MHz input frequency is shown in figure 4. Although the peak is too narrow to draw any conclusions based on only its shape, the distribution is very nearly Gaussian. The jitter (σ) here is 4.9 ps; the full width, i.e. difference between maximum and minimum delay, is 9.8 ps.

The jitter was measured over a range of frequencies, and the results are plotted in figure 8. As can be seen here, the output is stable over a wide frequency range: from 700 MHz up to 1.5 GHz[1]. At frequencies near the maximum value the jitter sharply increases. At slightly over 1.6 GHz, the counter/prescaler ceases to work. At the maximum operating frequency (1.6 GHz) the jitter was measured to be about 9.5 ps.

[1]The stable range extends to the lower frequencies also. In this measurement we, however, were primarily interested in the high-frequency performance.

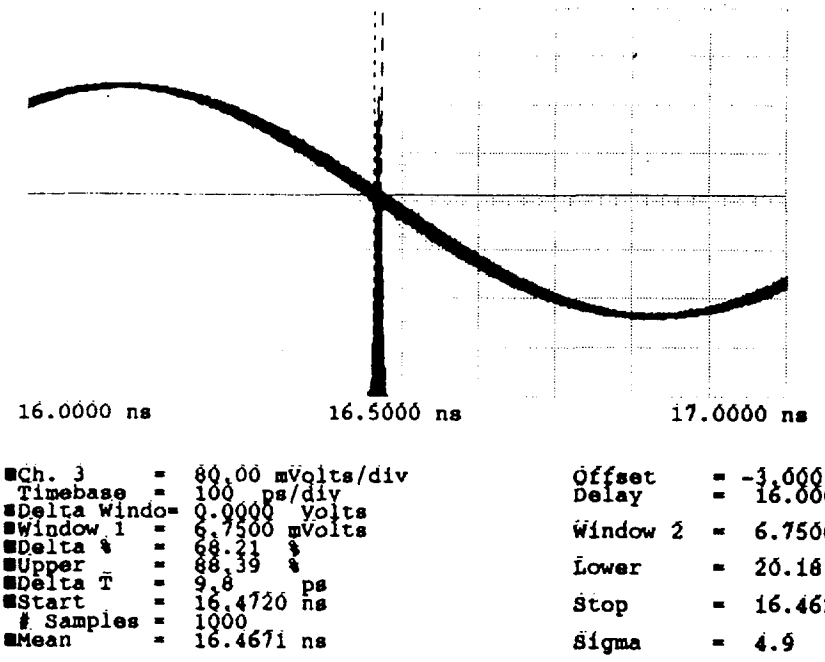

Figure 4. Distribution of the observed jitter at 714 MHz

The proper operation of the counters is another essential requirement, which had to be verified. This could be done by measuring the time difference between start and output signals for a longer interval. Any potential counting errors would then be detected as jumps in the delay time that are multiples of the clock frequency.

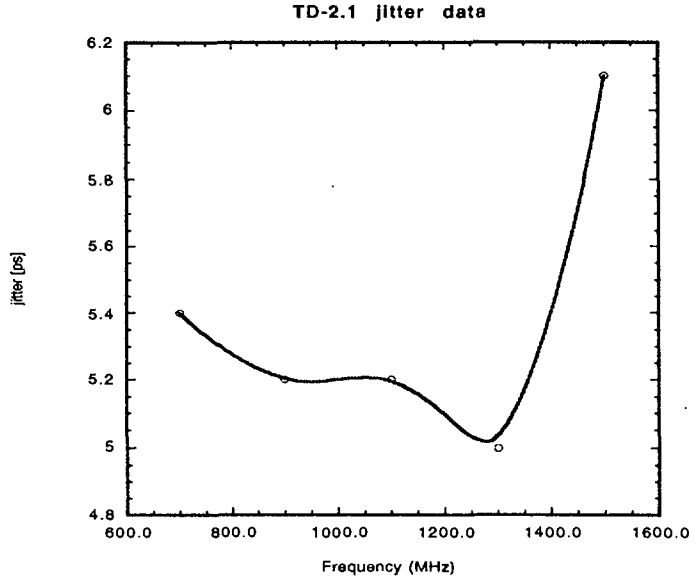

Figure 5. TD-2.1 jitter versus frequency.

For the counting error test, we used a time-to-digital converter (TDC) to measure the delays. The setup is shown in figure 6. One TD-2.1 is used to synchronize the trigger

signal with the input clock. The synchronized trigger is then fed into the TD-2.1 under measurement. The trigger pulse is used to start the TDC conversion and the output from the TD-2.1 delay is used to stop it. When the TDC receives a stop pulse, the converted value can be read. The tests were performed using a set of delay values (20, 80, 150, 270, 310 and 560 pulses) and measuring the delay 100000 times for each delay value.

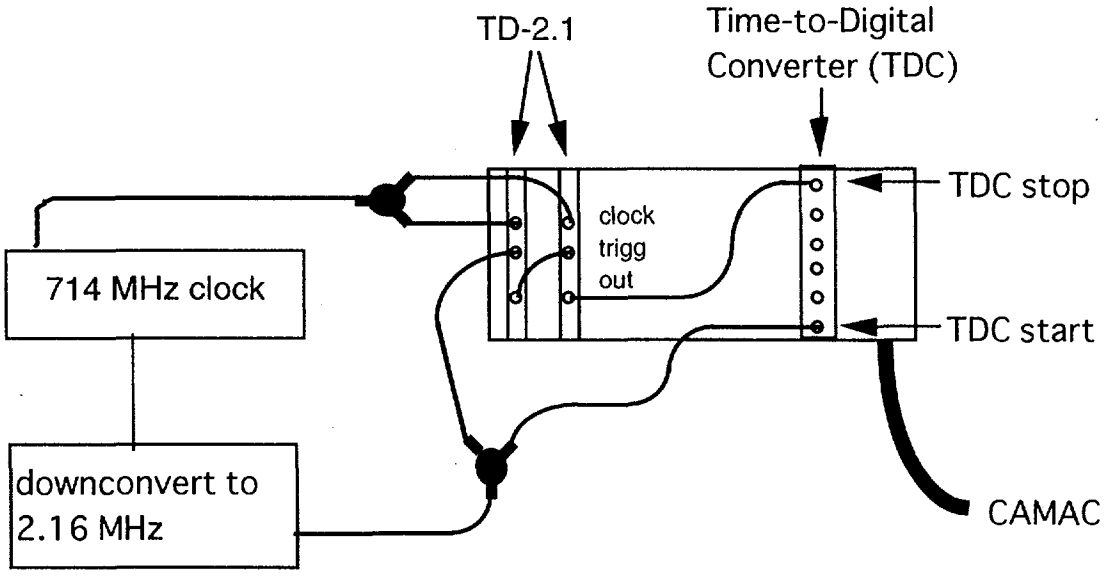

Figure 6. Reliability measurement setup

Since the TD-2.1 accuracy is much higher than the time resolution of the TDC, so this method does not yield any jitter data, but can provide a verification that the TD-2.1 counters work correctly with no synchronization errors. Since the TD-2.1 operates by counting input clock cycles, any errors would show up as time differences that are multiples of the clock cycle (i.e. at least 1.4 ns here). To measure longer delays, the resolution of the TDC was set to 200 ps/count. A counting error would show up as pulse counts differing by nearly one clock cycle from the count mean of each measured module.

The operating stability of the TD-2.1 modules could be verified. The probability of counting error was established to be smaller than 10^{-6} in a measurement series of delays of 520 clock pulses[2]. All of the other (shorter) delay measurements gave similar results. The combined delay values from a series of measurements performed on a set of modules is shown in figure 7. The peak width is mostly due to the resolution of the TDC.

[2]The error rate is probably even smaller than this, judging from the series of measurements made with different delay values.

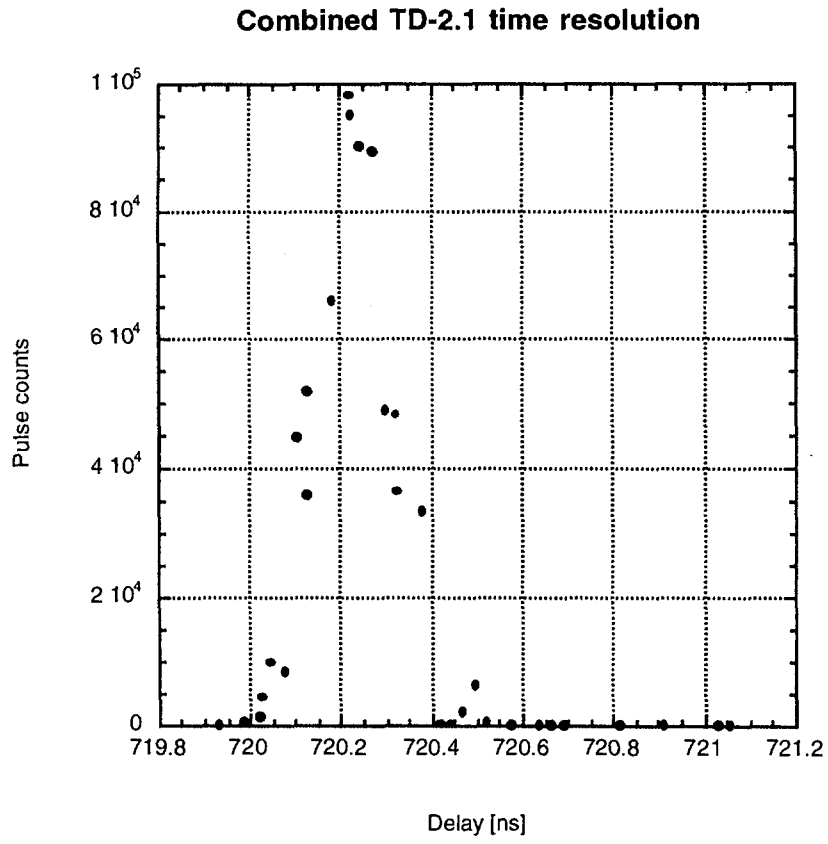

Figure 7. Combined resolution data from TD-2.1 measurement.

One point to note is that after switching on, the TD-2.1 requires some warm-up time to reach a stable state. Before warming up, the counters do not behave correctly and miscounts may occur. This time is somewhat module dependent, ranging from less than one minute to about ten minutes. All of the TDC tests were performed after the modules had reached a stable state.

3. Conclusions

The performance of the TD-2.1 programmable delay module was measured and evaluated. It was found out that it works reliably over a wide range of input clock frequencies, up to 1.6 GHz. The jitter (σ_T/T) of the output is low in the desired operation range, and below 6 ps up to a frequency of 1500 MHz.

References:

1. J. Urakawa et. al., "TRISTAN Timing System" Nucl. Instr. and Meth., A293, 1990, 23

2. K. Ishii, "Digital Delay CAMAC Module with 550 MHz preset Counter (TD-2)" KEK Report, KEK 83-14, September 1983

Appendix. Operating Instructions

TD-2.1 can be controlled either remotely using CAMAC functions or by the front-panel switches. To use TD-2.1, first connect the clock, start (trigger) and the output signals. The clock input can be either a sine or a square wave, and should have a peak-to-peak amplitude of at least about 500 mV. The absolute maximum input level is 1 V peak-to-peak. Clock signal amplitude of 800 mV P-P amplitude should be sufficient in the whole operating range.

The start pulse is required to be in **NIM** level. The counter operation can be inhibited using the Inhibit NIM-level input. Output trigger signal is available in both **NIM** and **TTL** levels. The front-panel signals are listed in table 1 and the CAMAC function codes in table 2.

Use either the front panel switches or the CAMAC interface to set the desired delay values. The delay counter value can be increased/decreased by pressing (continuously) the front panel button. The speed of the increment can be selected to be high (20 Hz) or low (2 Hz). Before first Start pulse, the Load button (or CAMAC function) is used to load the delay value into the counter; subsequently the counter is automatically reloaded after each output pulse.

Signal	Level	Explanation
CLOCK (input)	Square or sine wave, 500 mV to 1V p-p (4 to 10 dBm)	Counter clock. 800 mV p-p level recommended
START (input)	NIM	Counter start signal
INH (input)	NIM	Counter inhibit
OUT1	NIM	Trigger out (terminal count)
OUT2	TTL	Trigger out

Table 1. Input/output signals of the TD-2.1 (front panel)

Function code	Explanation
F0A0	Read preset delay value (13 bits)
F16A0	Load preset delay value (13 bits)
F24A0	Counter inhibit
F26A0	Counter enable

Table 2. CAMAC functions of the TD-2.1