VME Data-Taking Module

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A general-purpose DSP-based VME data acquisition module has been designed and built in the Electronics Laboratory. It is designed as the VME 6U slave module equipped with an exchangeable input board. Digital input signals are scheduled to control data acquisition. The module prototype is dedicated as an intelligent readout controller during microstrip detector tests.

The main features of the module are as follows:

- 96002 Motorola DSP processor running at 33MHz for data processing,
- 56002 Motorola DSP processor running at 33MHz for input queue handling,
- 64k x 32 static memory, shared among the 96002 and VME,
- 32k x 32 of program memory and 32k x 32 of working memory connected to the 96002,
- two 64k x 32 static memory pages working as interface between 56002 and 96002,
- microcontroller (μC), responsible for booting the DSP and all "slow control" tasks on the board,
- exchangeable input daughterboard controlled by byte-wide bus directed by the microcontroller,
- 32k-deep 18-bit FIFO between the input daughterboard and the 56002.

Data flow goes from the input board, through the FIFO, the 56002, one of the memory pages, the 96002, to the shared memory. This memory shared between the 96002 and the VME interface is accessible directly from the VME.

The module is equipped with an exchangeable input board. The following types of input boards are considered:

- 1 analog input,
- 8 analog inputs,
- 16 digital inputs with selectable threshold level (TTL, ECL),
- mixed input: e.g. 1 analog + 5 digital inputs.

The input board is attached to the main board by two connectors:

- "fast" - with data bus, data enable signal and Acquisition Clock. The Acquisition Clock is used either as a convert signal for an ADC or as a clock for latching digital data. It can be delayed on the input board.
- "slow" - with extension of an 8-bit-wide bus of the μC for slow controls.

The prototype input daughterboard will be equipped with a 10-bit 18-MSPS ADC accompanied by a 12-bit DAC (for adjusting the DC level of input signal) and by a programmable delay generator (for trimming conversion timing). Four control signals are received at the module. These are:

- Acquisition Clock;
- Start of Event;
- Stop of Event;
- External Convert;

All control signals are differential at TTL level. The Start/Stop signals, together with the Acquisition Clock, are used for generating the two MSB's passed to the FIFO (event marking) and the FIFO "write" signal. The mechanism for skipping initial pulses and limiting event size is implemented in a programmable logic (Xilinx 4005). Event size and number of skipped pulses can be programmed (the μC or VME).

Short and fast procedure in the internal program memory of the 56002 transfers data from the FIFO to one of memory pages. "Stream oriented" calculations (calculating mean value and standard deviation, finding minimum and maximum value, event size and event numbering) are performed during this step.

The 96002 performs intensive computational tasks on events appearing in page memories and puts results in to the output memory, shared with VME. The 96002 has two-port architecture. Port B is connected to the shared memory and VME interface. Pages, program and working memory are on port A. On-chip program memory of the 96002, loaded by the microcontroller, should contain programs ("firmware") which make it possible:

- to access all memories on port A "through the chip",
- to manage pages properly,
- to load and execute user programs.

PADEL - Data Acquisition Package

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The PADEL controls the operation and reads data from a multiparameter data acquisition system. CAMAC crate controlled by IBM PC/AT computer contains the following modules: a crate controller, Silena 4418/V analog-to-digital converter, Polon 712 analog-to-digital converter, 401 binary counter and a coincidence module. The data read from the detectors are sent via Ethernet to the VAX 4000/60 work station and written to the disk. Another IBM PC connected to the VAX by Ethernet is used for monitoring the collected data.

The tasks of the PADEL package are given below:

- loads configuration parameters from VAX file to PC memory and shows them on the screen,
- programs the CAMAC modules (coincidence module, ADCs and counters),
- starts the measurement,
- suspends and resumes data collection,
- stops the measurement.

The coincidence module and ADCs are programmed and counters are cleared at the beginning of the experiment. The coincidence module selects interesting coincidences and then the ADCs are read and an event is formed. The events are written to the file on the VAX disk. The counters are read both on user's demand and automatically at the end of the measurement. When data acquisition is suspended, the events in PC memory are automatically transferred to the VAX. During data acquisition, PADEL offers the basic file-handling functions like viewing the file or deleting it.

PADEL has been written in object-oriented C++ language. The Turbovision graphic library has been used to provide windows and menu system. The CAMAC crate controller used in the system is a custom design of the INP Electronics Laboratory.

Fig. 4 presents the logical structure of the PADEL package.