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Comparison between two possible CMS Barrel Muon Readout Architectures

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Dirección de Tecnología

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32 pp. 13 figs. 1 refs.

Abstract

A comparison between two possible readout arquitectures for the CMS muon barrel readout electronics is presented, including various aspects like costs, reliability, installation, staging and maintenance. A review of the present baseline architecture is given in the apendix.

"Comparación entre dos posibles arquitecturas de la electrónica del Barril del Detector de Muones del CMS"

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Resumen

Se presenta una comparación entre dos posibles arquitecturas para la electrónica de lectura de las cámaras de muones del experimento CMS. Se discuten varios aspectos tales como costes, fiabilidad, instalación, etapas de desarrollo y mantenimiento. En el apéndice se presenta la versión actual del diseño de base.

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Introduction

In what follows we compare two possible approaches to the Barrel Muon Readout Architecture: the standard one, stated in the Technical Proposal and presented with more detail in Appendix 1, in which most of the electronics—except for preamplifiers, discriminators and cable drivers—will sit outside the iron yoke; and an alternative approach[1], in which as much electronic as possible is put inside the volume of the chambers.

This comparison includes cost considerations, reliability, installation, staggering, maintenance, and is followed by some conclusions.

Costs

By putting the electronics inside the chambers, the first obvious cost reduction would be in cables and crates. This cost is estimated to be of the order of 2.5 MCHF and 1 MCHF respectively. This reduction may be true for the 200k twisted-pair cables that would be replaced by some 100 fibre optics. But it is not so clear for crates, as some new housing has to be prepared inside the chambers. Some draw-backs are the following: space is one of the major issues in this approach and it would require specially design mechanics, the electronics would require water cooling, cabling between readout boards implies hundreds of connections for the trigger logic without the ease of a backplane, the installation would be interlocked with the chamber construction, and probably would have to be "home-made". The real cost of this solution would easily equal the cost of cables and crates together.

As a general statement, the cost of electronic components and boards would be similar in both cases.

Reliability

The impossibility to access the chambers, once installed inside the iron yoke, makes reliability a great concern. On one hand, the alternative approach would reduce the number of cables and connections to extract wire signals outside the magnet volume. On the other hand, it would increase the number of electronic components and connections between boards for trigger purposes. Part of the problem could be rounded by redundancy at some extra cost. But the real problem, to make a valid comparison, is the lack of information about reliability of connectors. In general, manufacturers do not give this information except for very expensive units suited for military or space applications.

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[1] "A front-end readout architecture for the barrel muon detector: a feasibility study", CIEMAT Group. April 26, 1995.

Installation

In the standard scenario, the installation of the readout electronics is independent of the construction of chambers, and installation of cables. On the contrary, the alternative approach links together these tasks. The installation of the electronics would be part of the assembly procedure of the chambers.

Staging

One clear advantage of the standard design is the possibility, if necessary, to arrange the installation of the readout electronics in steps over a long period of time. Otherwise, the complete installation has to be done synchronously with the assembly of the chambers, and concluded before the chambers are put inside the magnet yoke. The opportunity of staging could be very convenient for the management of resources.

Maintenance

In the alternative design there is no possibility of maintenance. Provision has to be made for redundancy based on the probability of failure.

Conclusions

The following table summarises the situation.

	Standard	Alternative
Cost	same	same
Reliability	?	?
Installation	easier	difficult
Staggering	possible	not possible
Maintenance	possible	not possible

We may conclude that the alternative approach can be rejected.

References

C. Willmott et al., "A Front-End Readout Architecture for the CMS Barrel Muon Detector: A Feasibility Study". Informes Técnicos CIEMAT 789, Febrero 1996.

Appendix 1

The CMS Barrel Muon Readout Architecture

Introduction

The CMS Technical Proposal presents a brief description of the Barrel Muon Detector Readout Architecture. Here we discuss some possible implementation and considerations of such architecture.

Overview

Front-End

The chambers will provide discriminated signals at a feed-through connector (FTC) grouping 16 wires. The signals will be of differential type and the signal drivers will be able to drive a 25 meter cable. The FTC will have 32 usable pins.

Signal Cables and Connectors

The signals will be taken to a patch panel sitting at one end of the chambers. There will be one patch panel per chamber. The link between FTC's and patch panel will be a twisted-pair flat-and-round cable (CBL1). In principle these cables will be of equal length. A relaxation of this constrain and its implications has to be studied. These cables will have a plug on each end.

At the patch panel there will be two sets of connectors mounted on a PCB: one looking at the wires (PPC1) and the other looking at the readout electronics (PPC2). The later will group 32 signals, i.e. it will have 64 usable pins.

Signals will be taken from PPC2 to the Local Readout Crates (LRC) by a 20 meter twisted-pair flat cable (CBL2). At the LRC end there will be one connector per cable (LRCC), grouping 32 signals. The LRCC will have 64 usable pins.

TDC and Readout

There are many possible arrangements to connect wires to boards, and to place boards on crates. The approach followed here has been to group wires first by planes (φ, θ), then by chambers, and last by sectors. With this approach we could place one sector in 2 crates. Therefore:

- One Readout Board (ROB) will receive signals from 128 wires (Fig. 1). It could be a VME 9U like board.
- TDCs and Mean Timers (MT) corresponding to the same wires will be placed on the same board.
- 32 TDCs will be packed in one chip together with one Readout Controller (ROC). This is the TDC/ROC chip.
- There will be 32 MT's in each ROB.
- In the φ-plane, one MTC will be connected to 4 MT's from the inner SL and up to 12 MT's from the outer SL. There will be 4 MTC's in one ROB.
- There will be one TS per plane (φ, θ). TS_φ will be implemented in 2 boards. TS_θ will be implemented in θ-ROB's or/and TS_φ boards.
- 14 ROB, 4 TS board, 1 TTC board, and 1 Readout Server (ROS) board will be sitting in one Local Readout Crate (Fig. 2). At present, such a crate is not standard. Future VME64 or VME/P could be used.
- 1 Digital Data Link (DDL) will collect data from 2 Readout Crates.
- 8 DDL will be connected to one Front-End Driver (FED).
- 8 FED will be sitting in one FED Crate.

Table 1 summarizes this readout architecture.

Table 1: Readout architecture. Number of units.

		Wires	TDC/ROC chip	MT	MTC	TS	ROB	CBL1	CBL2	LRC	ROS	DLL
MS1	θ	252	8	63		1	2	16	8	2/14		
	φ	392	15	98	13	1	4	26	13	4/14		
MS2	θ	252	8	63		1	2	16	8	2/14		
	φ	472	15	118	15	1	4	30	15	4/14		
MS3	θ	252	8	63		1	2	16	8	2/14	1	
	φ	576	18	144	18	1	5	36	18	5/14		
MS4	θ	252	8	63		1	2	16	8	2/14		
	φ	800	25	200	25	1	7	50	25	7/14	1	1
Σ		3248	103	812	71	8	28	206	103	28/14	2	1
x 60		194880	6180	48720	4260	480	1680	12360	6180	120	120	60

TDC/ROC chip

Fig. 3 shows a block diagram of one TDC channel and Fig. 4 shows a block diagram of the TDC/ROC chip. The operation is as follows:

Input signals

- At each bunch crossing, the content of TDC_Register and BX_Counter are written to TDC_FIFO—only when the former is different from zero. TDC_Register is reset and BX_Counter is incremented.
- When a trigger arrives after a fixed delay—the trigger latency—it is stored in TRG_FIFO.

Comparator

There is one Bunch_Crossing_Comparator per TDC channel (Fig. 5). The parameters OFF1, OFF2 and TRGLAT will be introduced in the chip by the slow control. The comparator performs 3 comparisons simultaneously to execute one decision in one clock cycle. According to the results of COMP_X, COMP_Y and COMP_Z, one of the following actions is executed:

1. Write EV#, TBXN, TDCN, and BXN into RO_FIFO and read next datum from TDC_FIFO.
2. Read next datum from TRG_FIFO.
3. Read next datum from TDC_FIFO.

The decision logic is the following:

```
IF ∃ BXN THEN
        IF ∃ TBXN THEN
                IF TBXN–OFF1 ≤ BXN ≤ TBXN + OFF2 THEN
                        WRITE TDC_FIFO & TRG_FIFO INTO RO_FIFO
                        NEXT TDC_FIFO
                ELSE IF BXN > TBXN + OFF2 THEN
                        NEXT TRG_FIFO
                ELSE IF BXN < TBXN–OFF1 THEN
                        NEXT TDC_FIFO
                ENDIF
        ELSE IF BXN ≤ BXC–TRGLAT
                NEXT TDC_FIFO
        ENDIF

ELSE IF ∃ TBXN THEN
        NEXT TRG_FIFO

ENDIF
```

Readout

In the present scheme the readout of RO_FIFO is driven from ROC. The sequence can be the following:

- ROC presents at ROC_BUS the event number (RO_EV#) to be read.
- With signal COMP2_EN RO_EV# is stored in COMP2.
- The presence of an event in RO_FIFO with the same event number is signaled by EVENT_HIT. (In case the event stored at RO_FIFO is older than RO_EV#, the event is unloaded to nowhere. This should never happen, but may prevent RO_FIFO to be blocked for ever.)
- With signal RO_EVENT_HIT ROC reads all EVENT_HIT signals, via ROC_BUS.
- With address lines S0 to S4 and signal ROE ROC reads one RO_FIFO with hits.
- The sequence is repeated until all hits for this event number are read.

ROC

Fig. 6 shows a ROC block diagram. The operation is as follows.

- At each trigger the trigger event number (EV#) and trigger bunch crossing (TBX#) is stored in ROC_TRG_FIFO.
- With the appropriate delay RO_EV# will be presented at ROC_BUS and COMP2_EN line is set.
- ROC sets line RO_EVENT_HIT and reads all 32 EVENT_HIT bits at ROC_BUS.
- With address lines S0 to S4 ROC selects one RO_FIFO and reads its data by setting line ROE. (The presence of more hits in the same RO_FIFO can be signaled at one of the spare ROC_BUS lines.)
- Data will be stored in EVENT_STORAGE memory, together with the corresponding Wire_Code.
- The sequence is repeated for all RO_FIFO's with hits.
- ROC writes in EVENT_STORAGE the event number (EV#), a word count, and an End_Of_Event word. (Plane, chamber and sector ID can be included).
- Once the Event_Block is completed it is send to ROC_FIFO. Eventually it may content no hits.
- Event_Block's in ROC_FIFO wait for ROS_BUS_Driver to be read.

The following table shows the structure of Event_Block:

Table 2: Event Block format

Event number (EV#)
Word Count
Hit 1/Wire Code
Hit 2/Wire Code
...
Hit n/Wire Code
End-of-event

TDC/ROC package

The TDC/ROC chip will need connections for the following signals:

- 32 Wire_in: differential, 64 connections.
- 15 TTC signals: 1 CLK, 1 LV1_accept, 1 BXC_reset, and 12 data lines.
- 1 Fast_status (any FIFO almost full).
- 18 data lines to ROB_BUS (see later).
- 6 address lines from ROS_BUS.
- 3 control lines from ROS_BUS.
- 2 Slow Control lines.
- Chip Reset
- 8 Power lines.
- 5 JTAG.

The total number of lines is 123.

MT, MTC and TS[†]

Here we are only concerned about the required space and connections between plane and chamber groups.

[†] Design and simulations of the trigger electronics for the CMS muon barrel chambers. M. De Giorgi et al., CMS TN/95-01. January 1995.

Wire signals

In one ROB there will be 32 MT's. As one plane will occupy from 2 to 7 ROB's and each MT receives signals from 9 wires, it will be necessary to pass up to 10 wire signals from board to board (Figs. 7 and 8).

φ-plane groups

It seems convenient to connect MT's to MTC's in bunches of 4. Therefore each MTC will receive signals from 12 to 16 MT's. Also if we place in each ROB correlated wires from Outer and Inner SL, in each ROB there will sit 4 MTC's. In general, in each φ-plane ROB it will be necessary to provide connections for the following signals (Figs. 9 and 10):

- 4 MT's from previous ROB. Except for the first one.
- 4 MT's to previous ROB. Except for the first one.
- 4 MT's from next ROB. Except for the last one.
- 4 MT's to next ROB. Except for the last one.

As each MT provides 8 signals for the MTC's (6 trkpar, 1 H/Lb, and 1 trg), it will be necessary to pass up to 64 signals from board to board

In addition there is one common connection from TS_θ (TRGθ) to every MTC in the φ-plane group.

We need to place one TS_φ per φ-plane group. It will receive signals from every MTC in the group. Each MTC has 25 connections to its TS (8 trkang, 6 trkpos, 5 $\Delta\varphi$r, 1 sel_MTC, 1 CORR, 1 MULT, 1 OVLP, and 2 TRG). It will be required to pass 43 signals from each ROB to its TS board.

The connection of each TS_φ to the Muon Regional Trigger is done using 2 optical links.

θ-plane groups

In the θ-plane, every MT is connected to its TS_θ (Fig. 11) by two lines plus 6 bus lines. Therefore, as there are always 252 wires in this plane, 70 connections are required.

The connection of each TS_θ to the Muon Regional Trigger is done using 2 optical links.

ROB types

From the kind of components and interconnections between boards, it may be convenient to make provision for 2 types of Readout Boards: φ- and θ-plane:

Table 3: Types and number of Readout Boards.

φ-plane	1200
θ-plane	480
Total	1680

To reduce the number of connections it may be convenient, if possible, to place TS_θ in one of the θ-ROB's.

Back panel and ROS_BUS

The readout link between ROC's and ROS will be done by a back panel bus (ROS_BUS).

Presumably the back panel will also provide the required connections between ROB's and TS boards.

Table 4 shows the necessary connections between the different boards.

It should be possible to handle this situation with the coming VME-like standards, having 160-pin connectors.

ROB board

Fig. 12 shows a possible layout of a Readout Board. It has the following IC's:

- 4 TDC/ROC.
- 32 MT. As they are SMT type, there are 16 on each side of the board.
- 4 MTC.

ROS Board

Fig. 13 shows a block diagram of ROS Board.

At each trigger ROS_BUS_Driver will collect one Event_Block from each ROC. Data will be stored in ROS_FIFO.

Event_Blocks will be packed in one Half_Sector_Event_Block by ROS_Processor and sent to FED via DDL.

Digital Data Link

This link is the "optical backplane" solution proposed in Front End Drivers in CMS DAQ, CMS TN/95-020, Rev. 1.03, Feb. 1995. One DDL will collect data from 2 Readout Crates.

Table 4: Connections between boards.

#	Board	TS	Tθ	MTC → TS								MT → MTC						W	Bus	Total
1	MS1 θ1	70																5	27	102
2	MS1 θ2 TS	68	1															5	27	100
3	MS1 φ1		1	19	24							64						10	27	145
4	MS1 φ2		1	19		24						64	64					20	27	219
5	MS1 φ3		1	19			24						64	64				20	27	219
6	MS1 φ4		1	19				24						64				10	27	145
7	MS1 φ TS			19			96												27	142
8	MS1 φ TS			19			96												27	142
9	MS2 θ1	70																5	27	102
10	MS2 θ2 TS	68	1															5	27	100
11	MS2 φ1		1	19	24							64						10	27	145
12	MS2 φ2		1	19		24						64	64					20	27	219
13	MS2 φ3		1	19			24						64	64				20	27	219
14	MS2 φ4		1	19				24						64				10	27	145
15	MS2 φ TS			19			96												27	142
16	MS2 φ TS			19			96												27	142
17	MS3 θ1	70																5	27	102
18	MS3 θ2 TS	68	1															5	27	100
19	ROS																		27	27
20	MS3 φ1		1	19	24							64						10	27	145
21	MS3 φ2		1	19		24						64	64					20	27	219
22	MS3 φ3		1	19			24						64	64				20	27	219
23	MS3 φ4		1	19				24						64	64			20	27	219
24	MS3 φ5		1	19					24						64			10	27	145
25	MS3 φ TS			19			120												27	166
26	MS3 φ TS			19			120												27	166
27	MS4 θ1	70																5	27	102
28	MS4 θ2 TS	68	1															5	27	100
29	MS4 φ1		1	19	24							64						10	27	145
30	MS4 φ2		1	19		24						64	64					20	27	219
31	MS4 φ3		1	19			24						64	64				20	27	219
32	MS4 φ4		1	19				24						64	64			20	27	219
33	MS4 φ5		1	19					24						64	64		20	27	219
34	MS4 φ6		1	19						24						64	64	20	27	219
35	MS4 φ7		1	19							24						64	10	27	145
36	MS4 φ TS			19				168											27	214
37	MS4 φ TS			19				168											27	214
38	ROS																		27	27

FED

DDU

The following interfaces are required[†]:

- Data link interface
- Control link interface.
- Merge interface.

† Front end driver in CMS DAQ. S. Cittolin et al., CMS TN/95-020. Revision 1.03. February 1995.

- Status interface.
- General purpose access.

Slow Control

The following information will be required at different levels of the readout system:

- LV1 trigger latency: a parameter, required at TDC/ROC chip.
- OFF1 and OFF2: parameters, at TDC/ROC.
- Clock deskew: parameter. Required at every TDC/ROC.
- Wire enable/disable: one control bit at TDC/ROC. Is it necessary?
- Maximum number of bunch crossings: at TDC comparator?

Also the following functions can be performed by Slow Control:

- Start chip internal test
- Read chip status
- Reset chip

A slow serial link may connect the Slow Control to every chip.

Reliability

In the present architecture the only parts not accessible for maintenance and reparations are cables and connectors sitting in the chambers and at the patch panels.

The following table shows the expected number of failures in 10 years of operation, assuming a failure rate of 1 FIT per contact (??):

Table 5: Number of failures in 10 years of operation.

Link	Type	Signals	Contacts	Units	Failures
FTC	connector	16	32	12360	40
CBL1	cable	16	64	12360	79
PPC1	connector	16	32	12360	40
PPC2	connector	32	64	6180	40
CBL2	cable	32	64	6180	40
Total					237
					0.12%

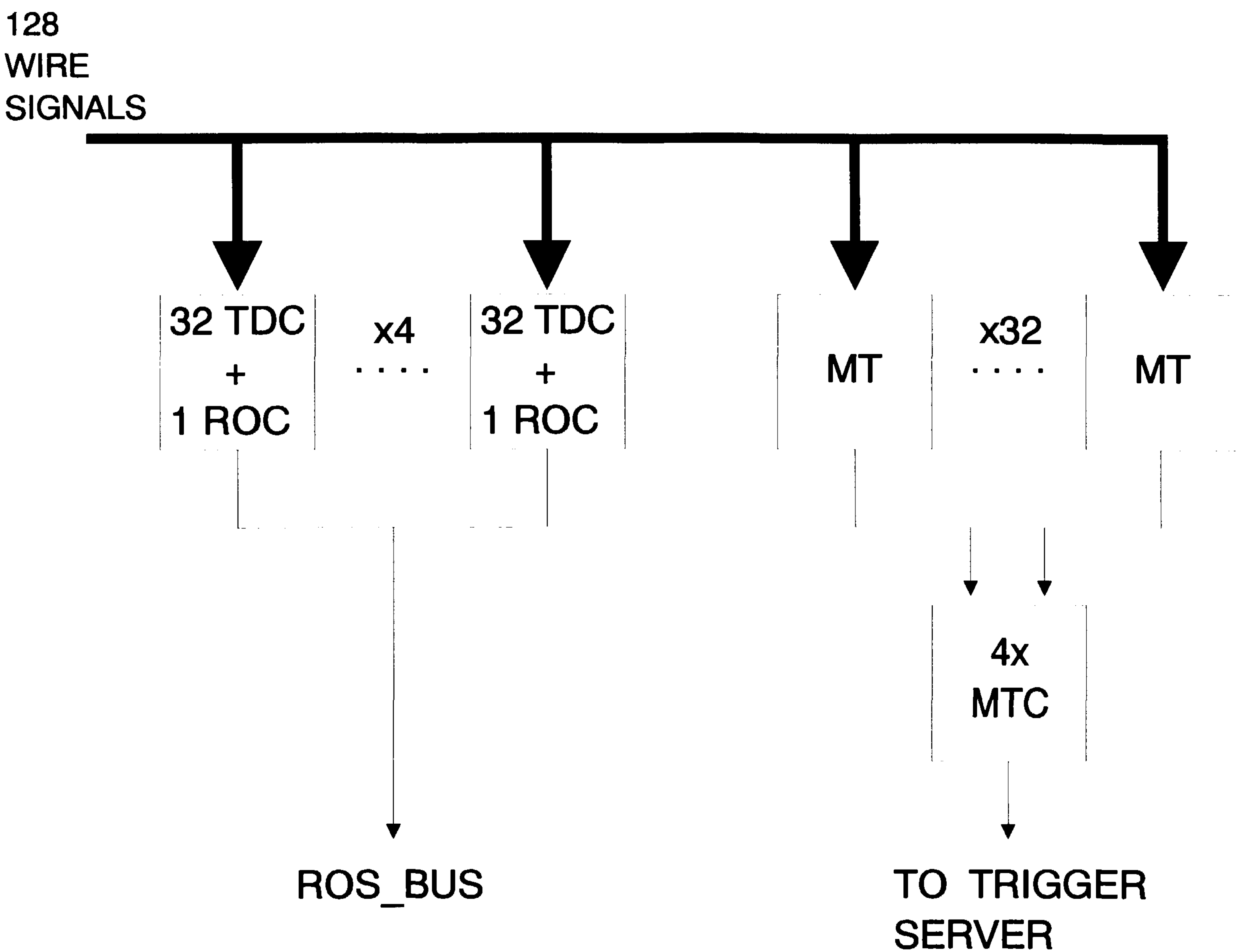

Figure 1: Readout Board

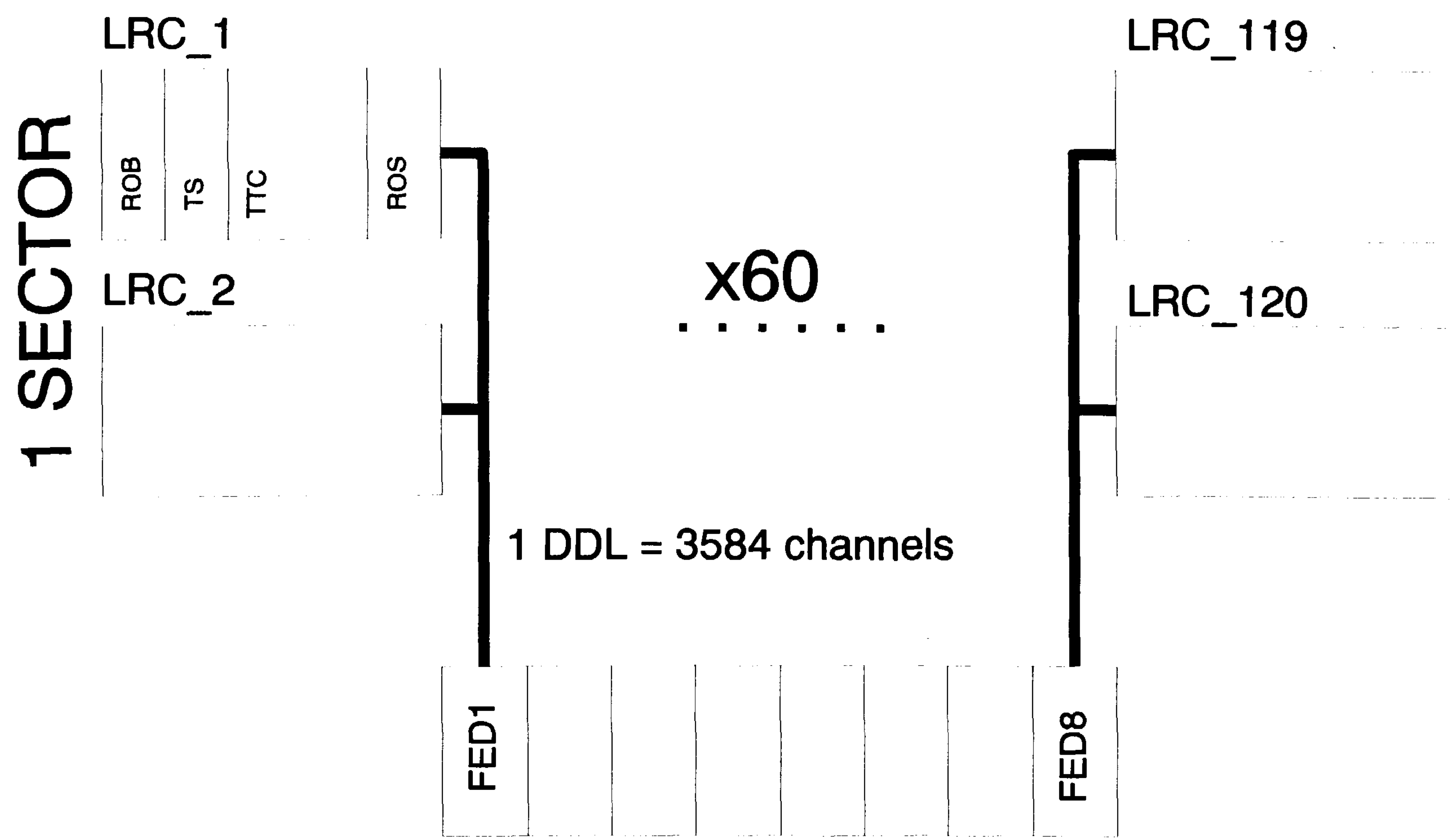

Figure 2 : Local Readout Crate Layout

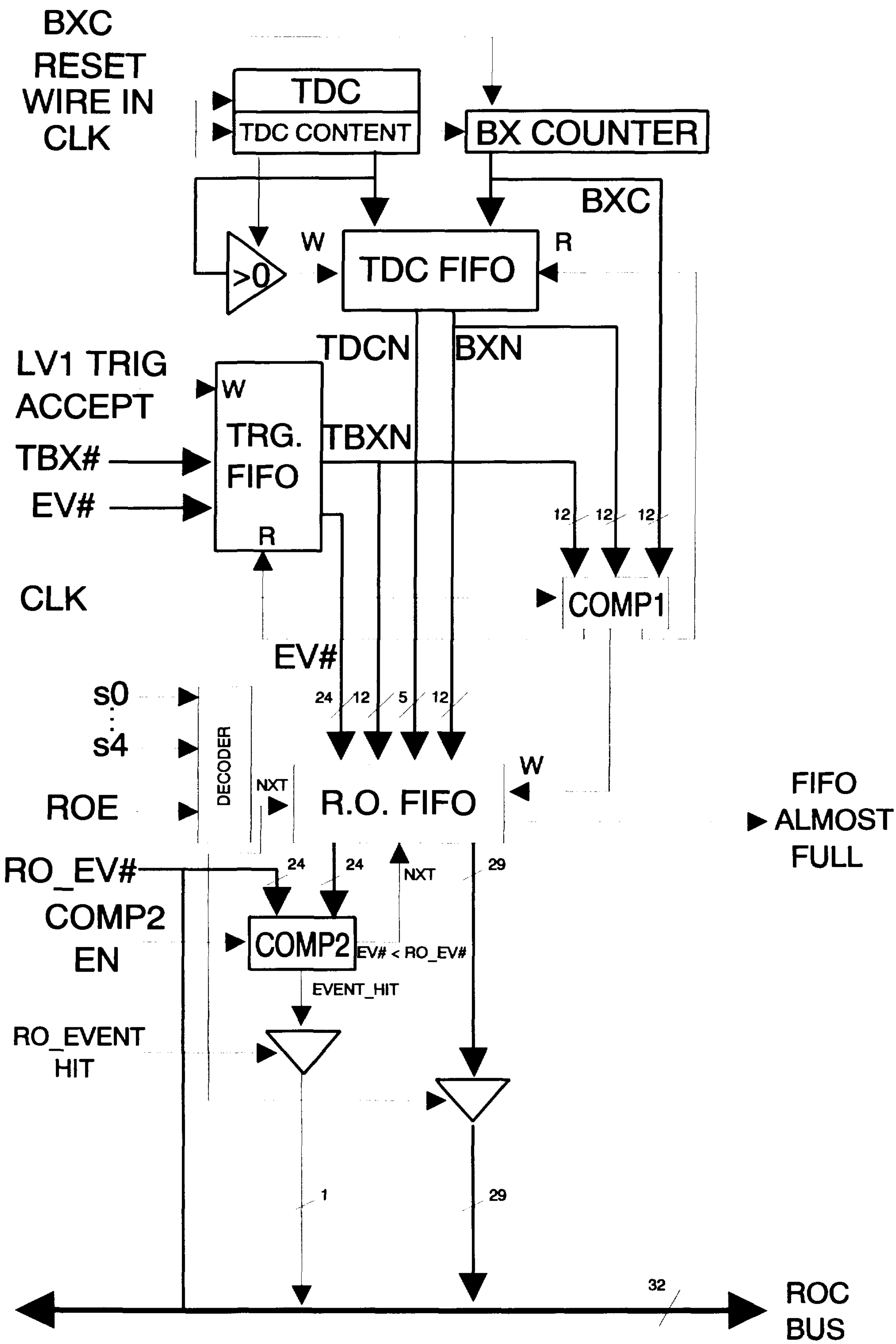

Figure 3: TDC Readout logic.

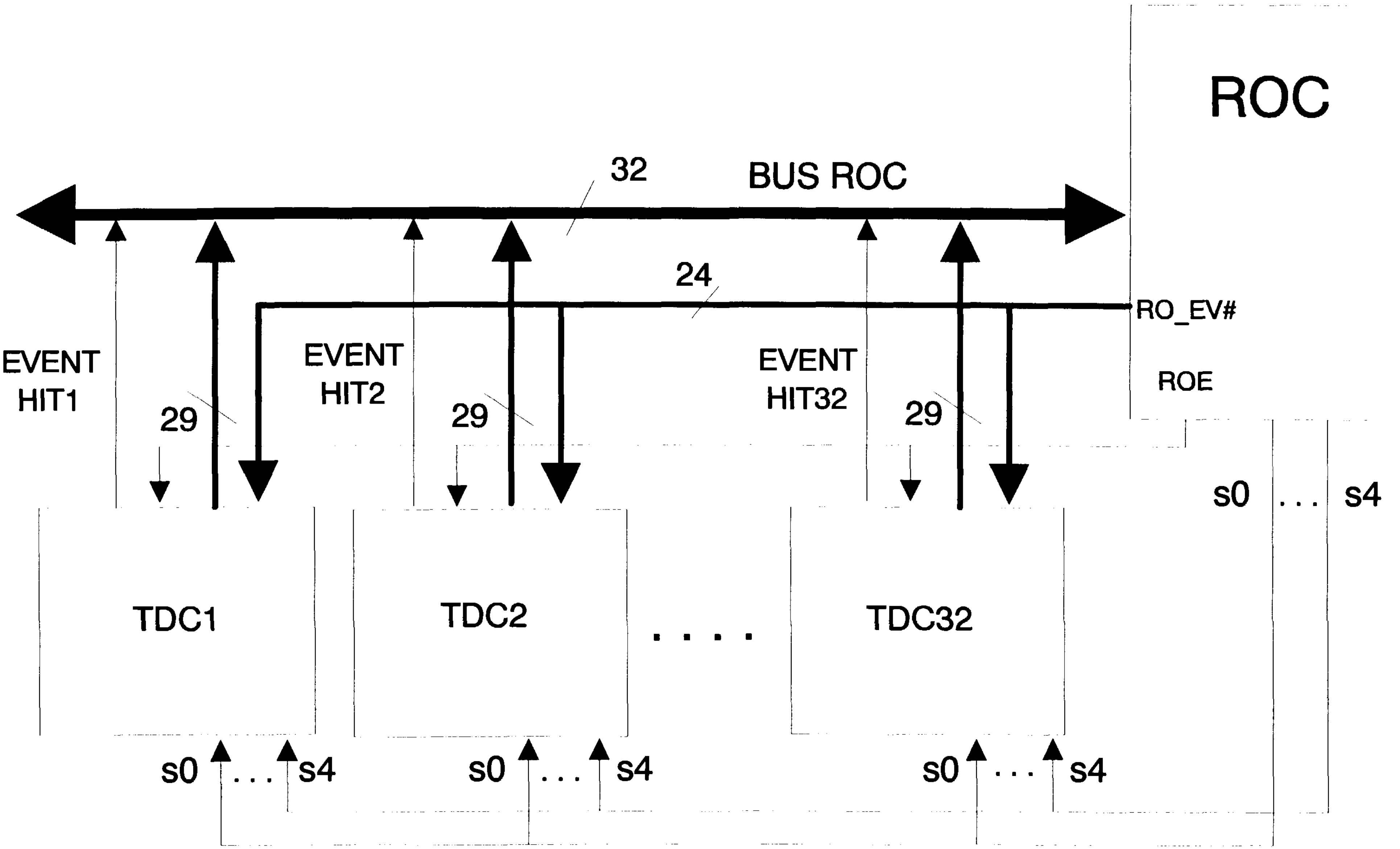

Figure 4 : TCD/ ROC Chip block diagram.

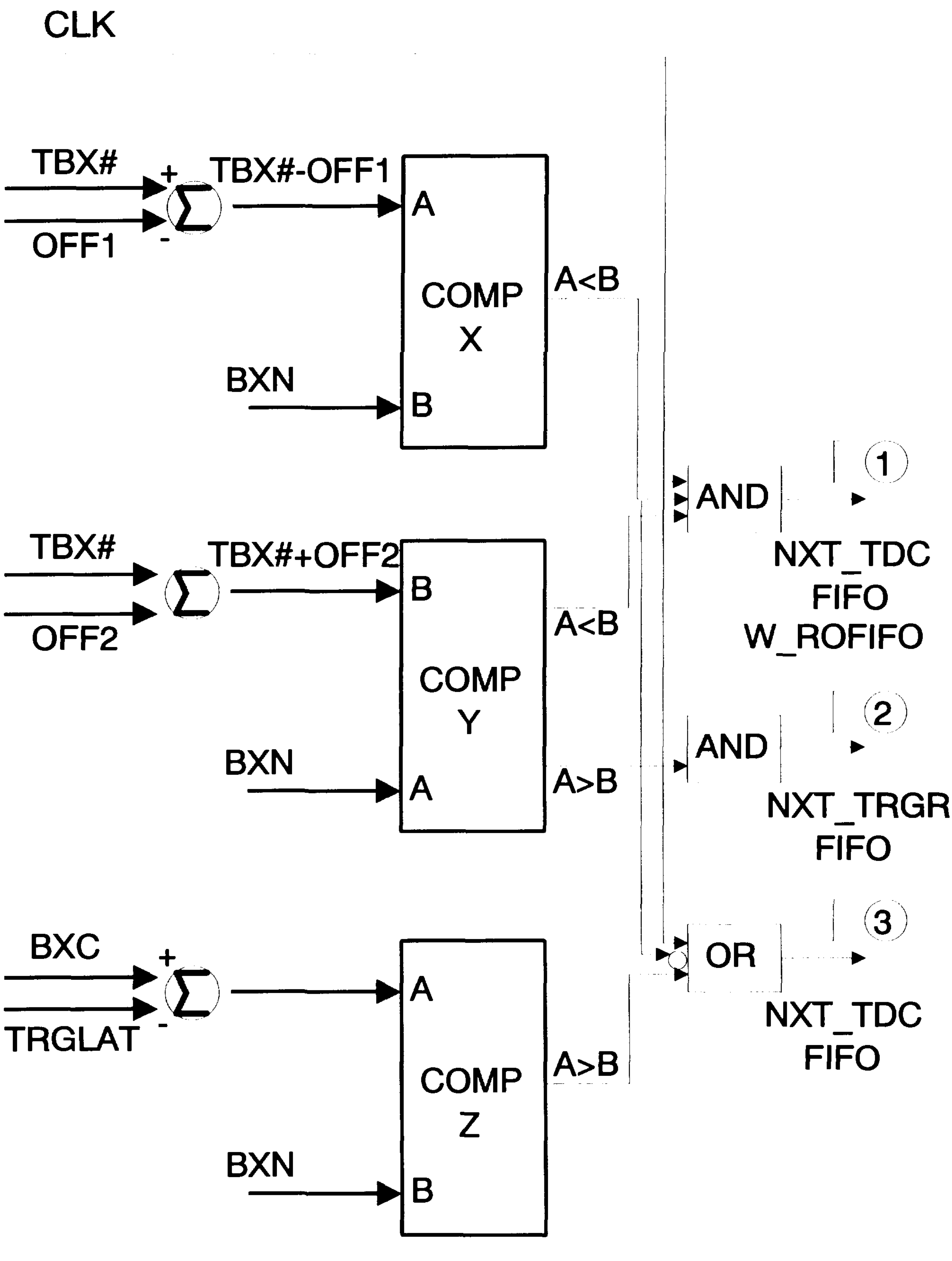

Figure 5: Bunch-crossing comparator block diagram

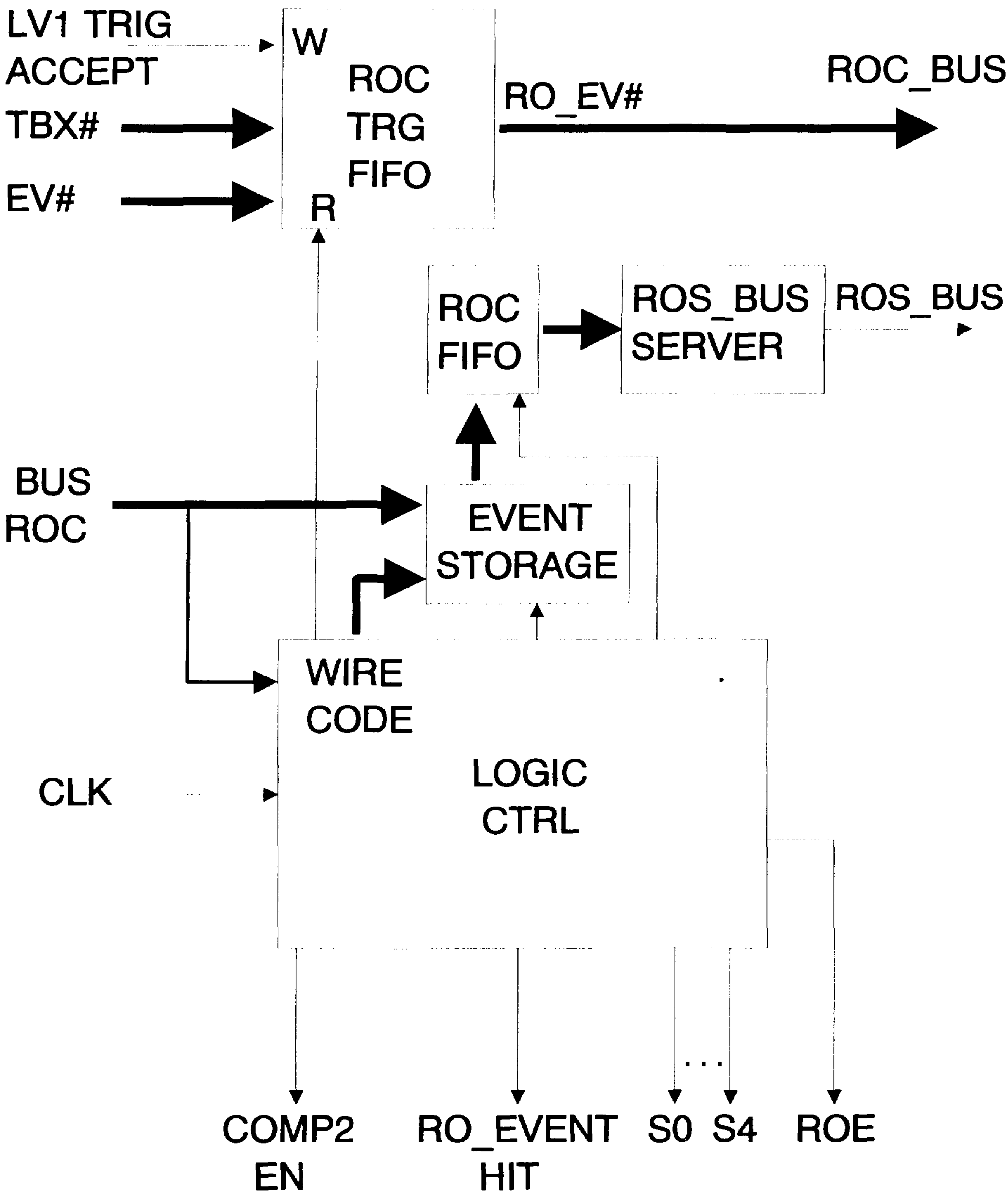

Figure 6: ROC block diagram.

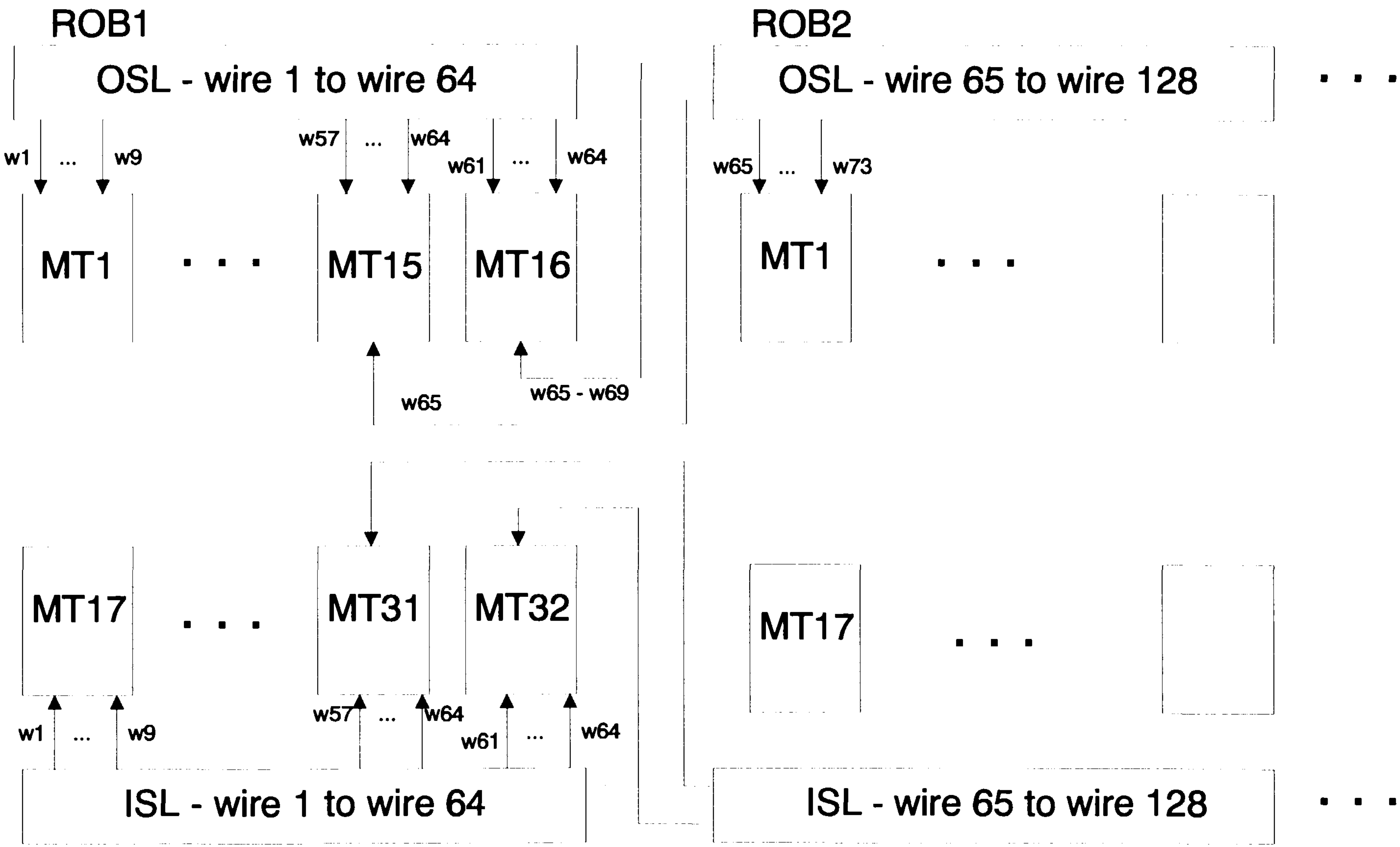

Figure 7: Wire to MT connections (ϕ-plane)

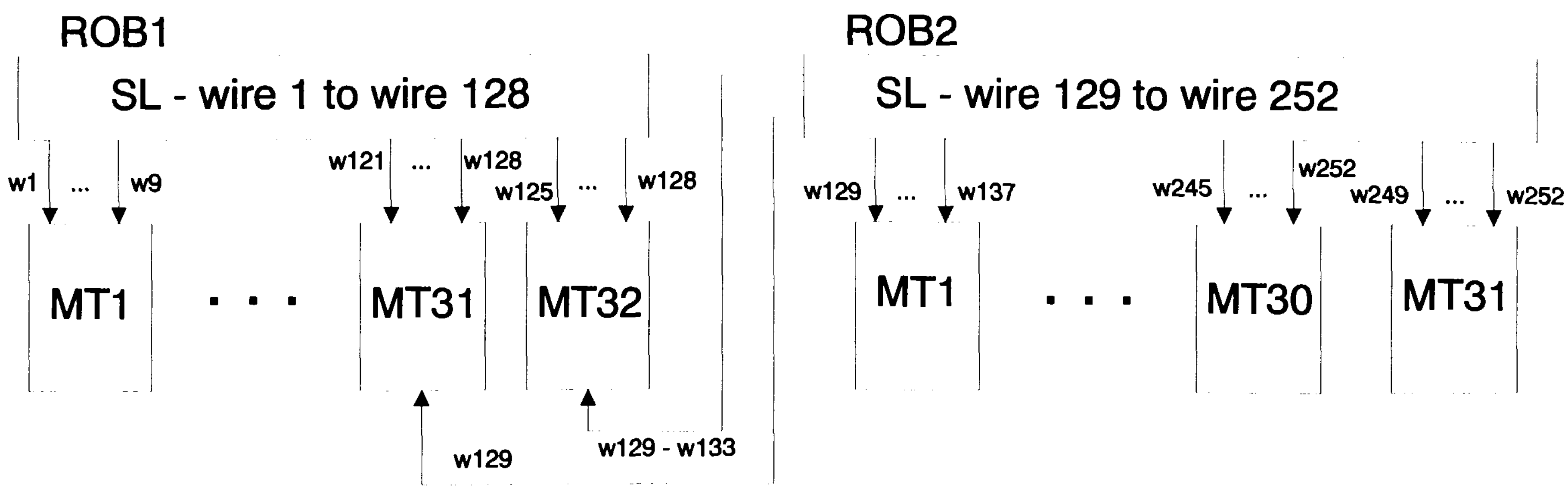

Figure 8: Wire to MT connections (θ-plane)

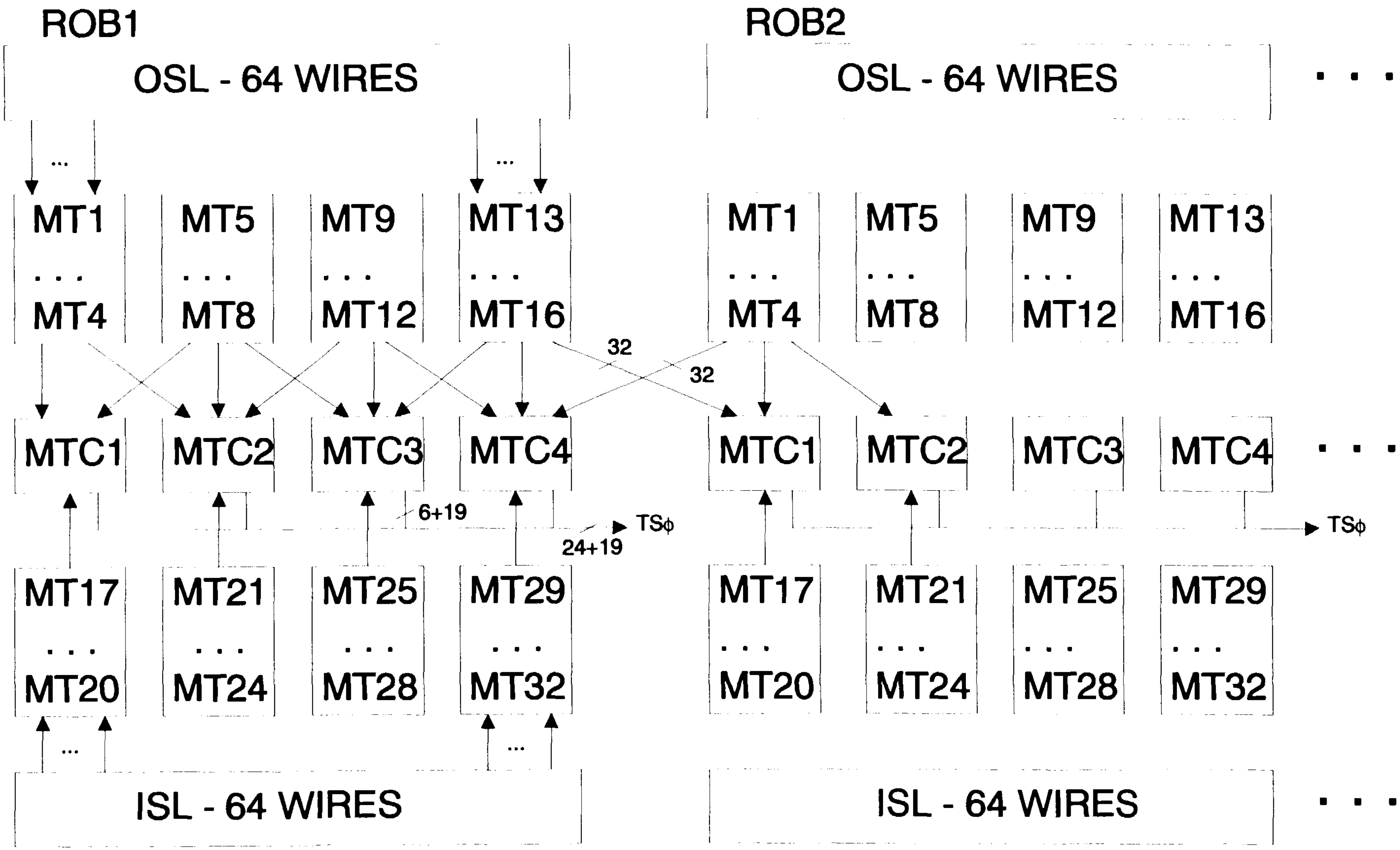

Figure 9: MT to MTC connections (ϕ-plane)

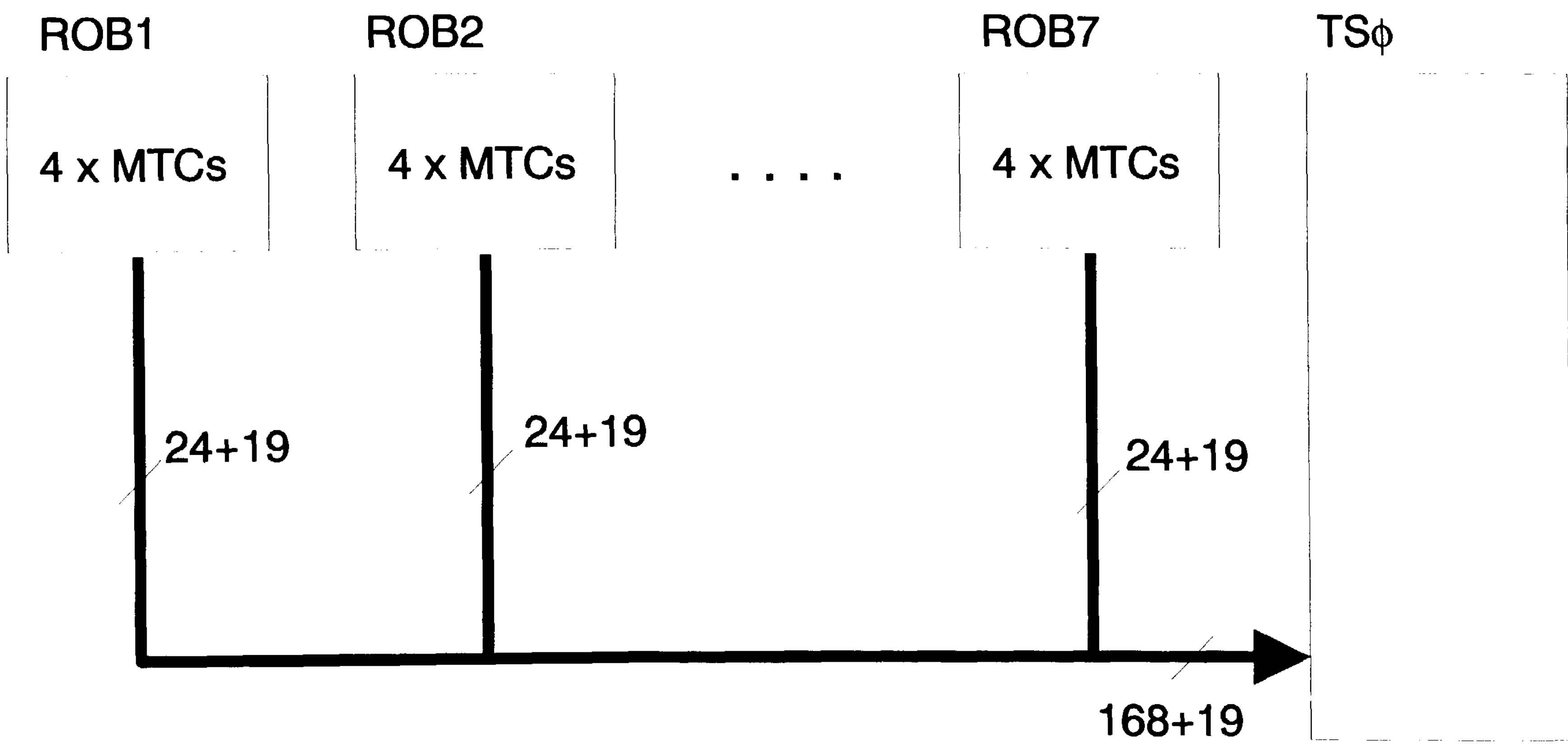

Figure 10: MTC to TS connections (MS4, ϕ-plane)

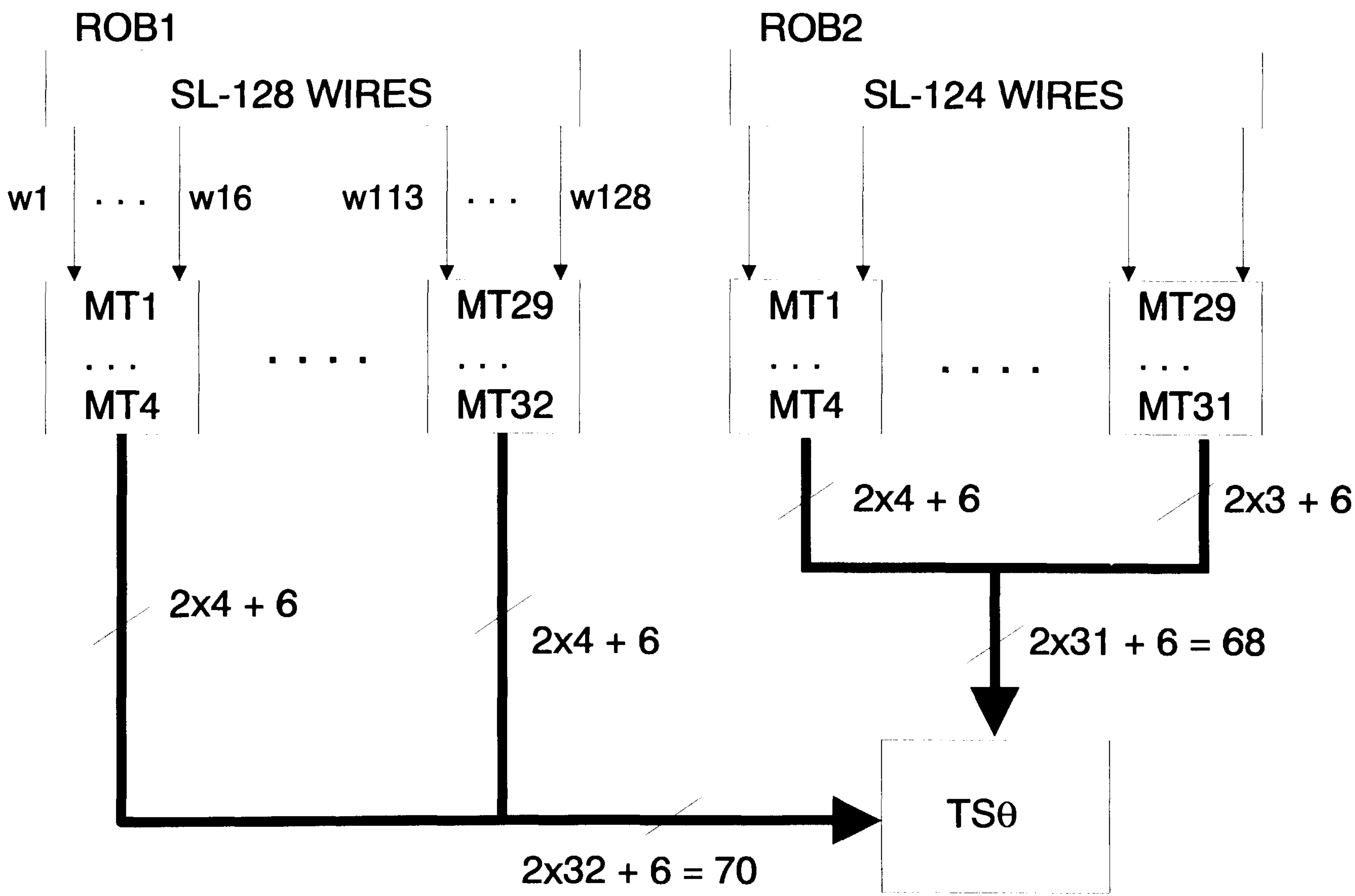

Figure 11 : MT to TS connections (θ-plane)

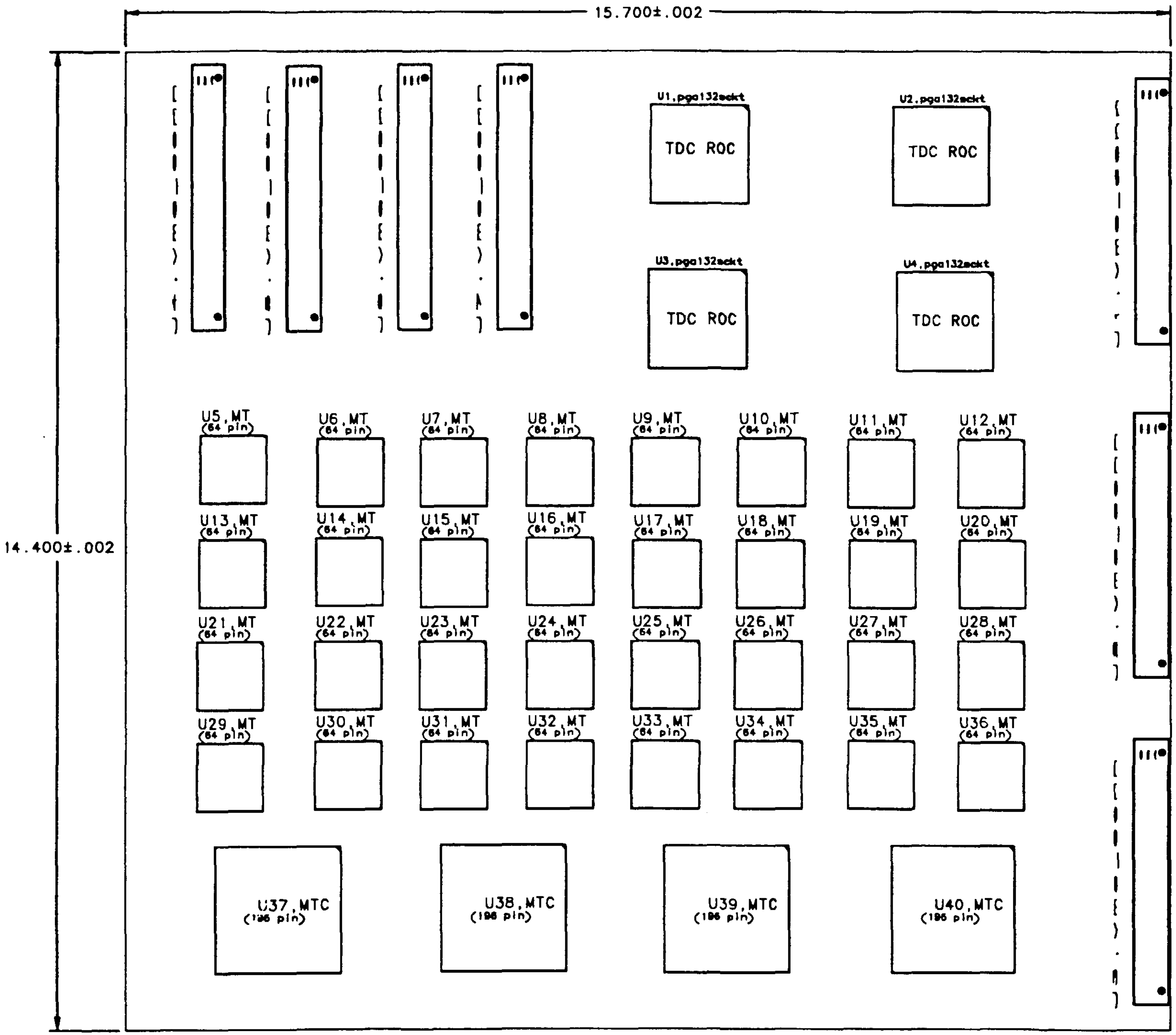

Figure 12: Readout Board layout

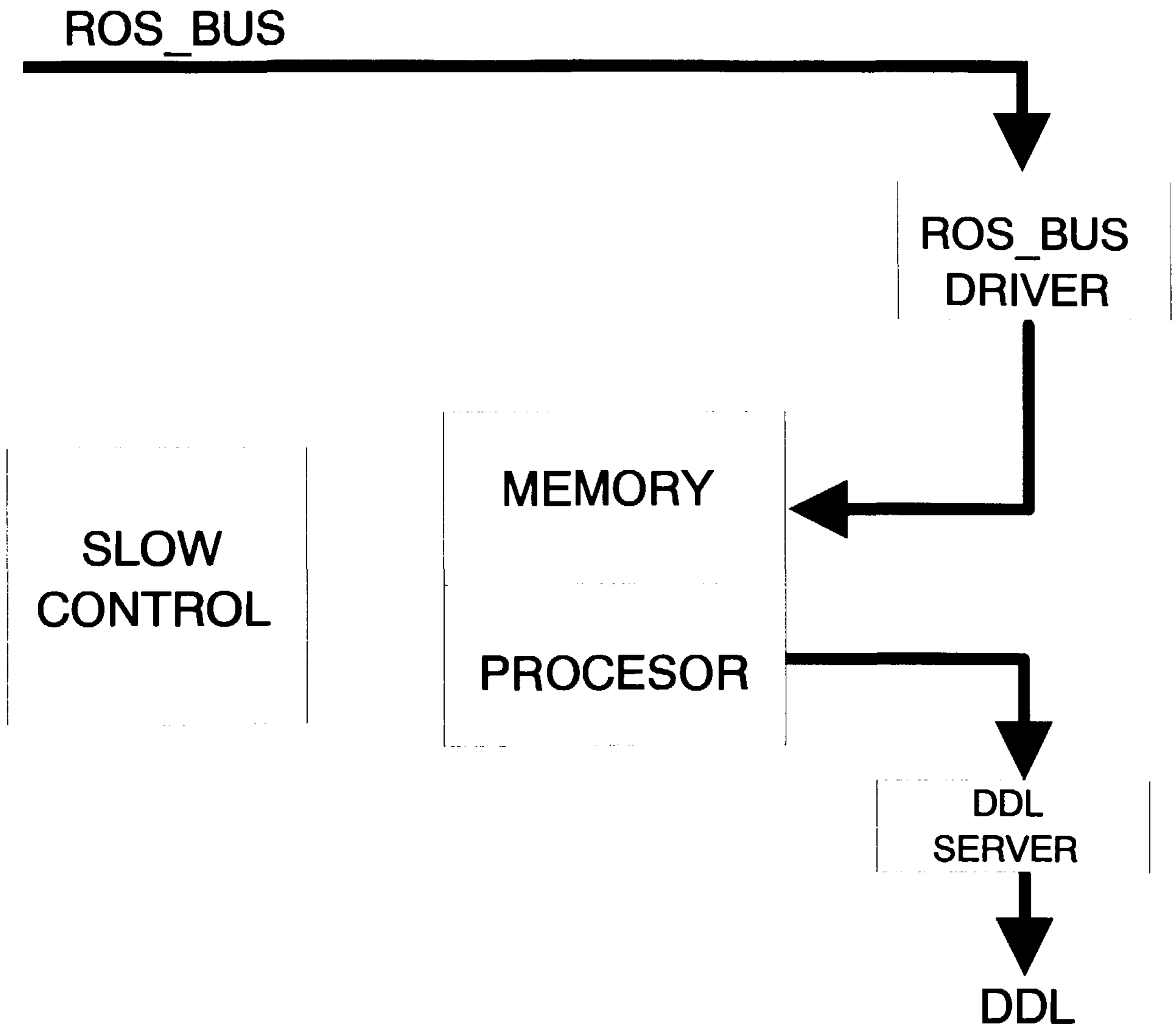

Figure 13 : ROS Board block diagram