Paper presented at Eighth Conference on Real-Time Computer Applications in Nuclear, Particle and Plasma Physics, Vancouver, June 8–11.

TRI-PP-93-65
June 1993

SYSTEM TESTING FOR A HIGH SPEED 1024 CHANNEL TRANSIENT DIGITIZER SYSTEM

S. Daviel, O. Belmont, A. Daviel, R. Poutissou
TRIUMF, 4004 Wesbrook Mall, Vancouver BC, V6Y 2S1, Canada

Abstract

A test system for a 1024 channel high speed (500MHz) transient digitizer system is described. Each channel consists of a 128 element gallium arsenide charge coupled device which is read out (at 32MHz) into a FASTBUS module incorporating a custom gate array for data compaction. The transient digitizer is designed for use in Experiment 787 at Brookhaven National Laboratory. Results are presented from both prototype and production testing.

I. INTRODUCTION

Digitizing of fast detector signals at high speed is essential in many detector systems for high energy physics experiments. This results in improved time resolution measurements and background rejection by pulse shape discrimination. The transient digitizer (TD) system described here was developed for studying rare kaon decays in Experiment 787 at Brookhaven National Laboratory (BNL). A 1024 channel high speed TD system based on a gallium arsenide charge coupled device (CCD) [1] is being developed at TRIUMF. This paper describes system testing methods.

II. SYSTEM DESCRIPTION

The digitizer system operates as follows: the output from a photomultiplier tube is sampled by a 128 element (bin) CCD at a rate of 500 MHz. Upon receipt of a valid trigger, the CCD sampling rate is reduced to 32MHz, and data output from the CCD is digitized into 8 bits. This data is then fed to one channel of a 16-channel FASTBUS data compactor module [2], which uses a custom gate array to perform pedestal subtraction, suppression of data below threshold, and compaction of the data into 32-bit words. The compacted data is read out and buffered in an SSP (SLAC Scanner Processor) [3] also resident in FASTBUS. The data buffer is then transferred from the SSP to the host computer for analysis.

The CCDs and associated circuitry are mounted on triple-width FASTBUS boards (16 per board), with 8 boards per digitizer crate. The data compactors are mounted in separate readout crates, 16 per crate. This minimizes electronic pickup between the compactor and CCD modules. The TD system can be easily expanded, since it is modular in design, with each 256 channels requiring 3 FASTBUS crates, forming 1 rack. One Master Trigger board per rack is required to synchronize the readout data from the CCD modules into the data compactors.

Prototype CCDs have been tested previously in E787 [1]. The readout system is now based on a custom-built FASTBUS data compactor system, that features a dead time better than 50 microseconds, individually programmable data threshold and skirt width for each channel, and pedestal subtraction programmable for every bin within each channel.

During the August 1992 run of Experiment 787 at BNL, scintillating fibres from the target were connected to a 16-channel TD system. Each channel of the TD consisted of a prototype CCD with its associated RF distribution system, connected to one channel of a prototype data compaction module.

III. TEST PROCEDURES FOR THE PRODUCTION VERSIONS

An extensive test procedure for the TD is required, which must be automated due to the size of the system (1024 channels). The testing is done within the SSP, taking advantage of its high processing speed.

The test results shown below have been produced using a 15-channel TD system consisting of a production version data compactor and a prototype CCD (production CCDs will soon be available).

A. *Preliminary Tests of the Data Compactors*

The data compactor modules are exercised in the FASTBUS crate (a maximum of 16 at a time) using both the Internal Test Mode and the Test Data Generator provided [2]. The SSP performs all the testing, updating a bank of error counters, which is read by the host computer at the end of the test procedure.

B. *System Tests*

System tests of prototype CCD digitizers and production data compactor modules are performed, using a programmable pulse generator to provide input signals to the CCD. A block diagram of the system used for testing is shown in Fig. 1.

The pulse generator provides the input signals to the CCD, a trigger signal to the Master Trigger, and a delayed trigger to start the readout of the SSP. The pulse generator may be either self-triggered, or triggered by random pulses from a scintillator excited by a source.

The test program is run on the host computer. It downloads a program to the SSP that accumulates the

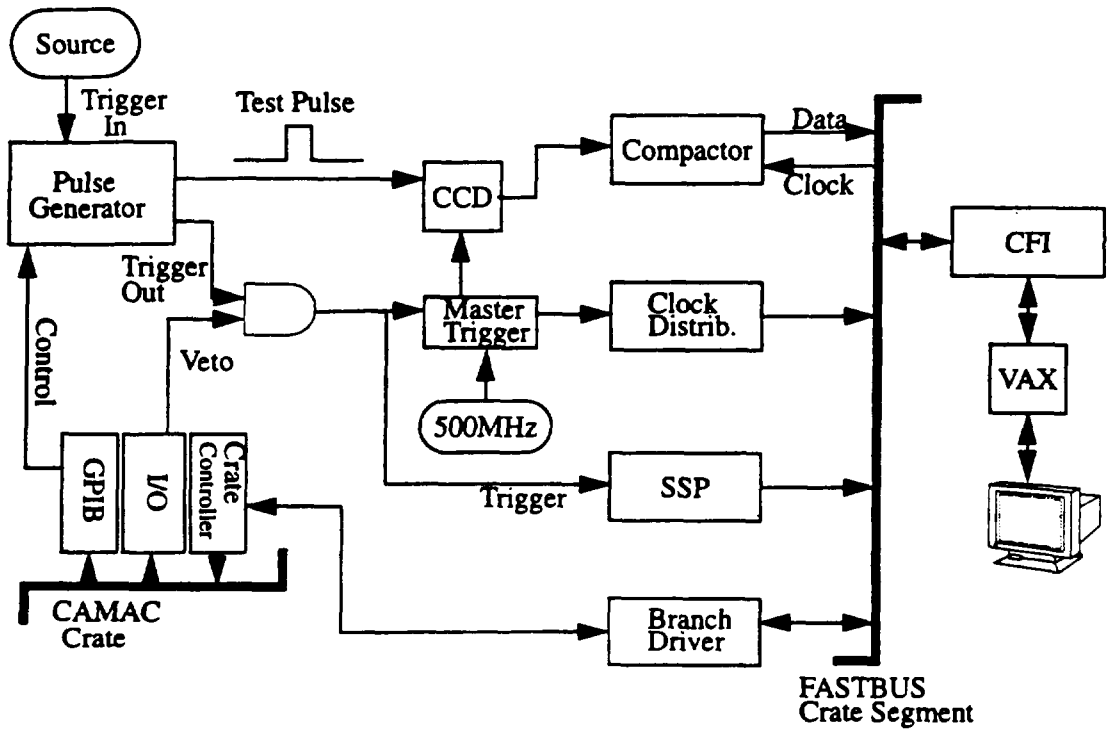

Figure 1 Block Diagram of test system for Transient Digitizer

sums and sums of squares of the input data for each bin of each channel. After the desired number of events, the host reads out the accumulated data, which are used to calculate the mean values and standard deviations. Six test procedures have been implemented. Tests 1 to 5 inclusive are performed one 16-channel TD module at a time. Test 6 can be performed on a fully loaded rack.

- Test 1 - Pedestal Check

A typical pedestal run (with CCD input signals of zero) is shown in Fig. 2. The mean values and standard deviations of each bin are compared with a maximum and minimum value. The pedestal values are downloaded into the compactor module, and pedestal subtraction is enabled.

- Test 2 - Crosstalk Check

A narrow pulse applied to one channel is used to check for any crosstalk. For the remaining channels, the mean values and standard deviations of each bin are compared with a maximum and minimum value. Any values exceeding these may indicate the presence of crosstalk between channels. A typical crosstalk run is shown in Fig. 3.

- Test 3 - Gain Test with wide pulses

A wide pulse (covering most of the range of the CCD) is applied to one channel in steps of increasing amplitude. For each step, a window is selected, consisting of a number of bins located in the flat top of the pulse. Averaging the bins in this window, the mean value and standard deviation of the pulse height are calculated, and the standard deviations compared with a maximum and minimum value. The mean values are plotted against the input pulse height, and a straight line fit performed. A plot of the gain is shown in Fig. 4. The slope and offset of the gain plot are calculated, with their associated errors. These are compared against maximum and minimum values.

- Test 4 - Gain Test with narrow pulses

This test is performed in exactly the same way as Test 3 above, except that a narrow pulse is used instead of a wide pulse.

- Test 5 - Pulse stepped across CCD

A narrow pulse is stepped across the range of the CCD (by increasing the delay). The mean value and standard deviation of the pulse height are calculated as in Test 3, and the standard deviations compared with a maximum and minimum value. The mean values are plotted against the delay of the input pulse, and a straight line fit performed. A typical plot of the stepped delay is shown in Fig. 5. The slope and offset with their associated errors are calculated. These are compared against maximum and minimum values.

- Test 6 - Stability Check

A stability check is performed over an extended time period (of several hours). The CCD input connection is removed, and, with pedestal subtraction enabled, a

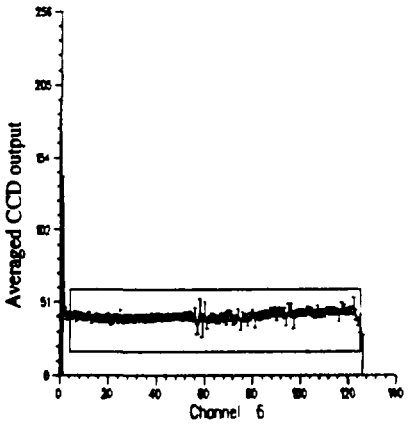

Figure 2 Pedestal measurement

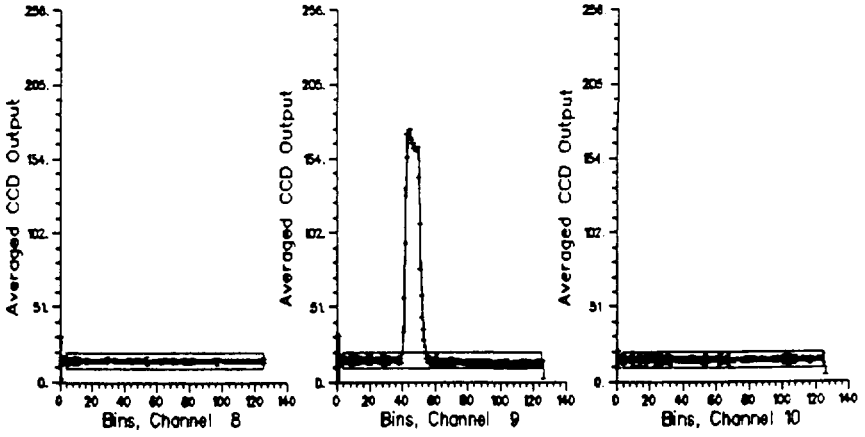

Figure 3 Crosstalk measurements

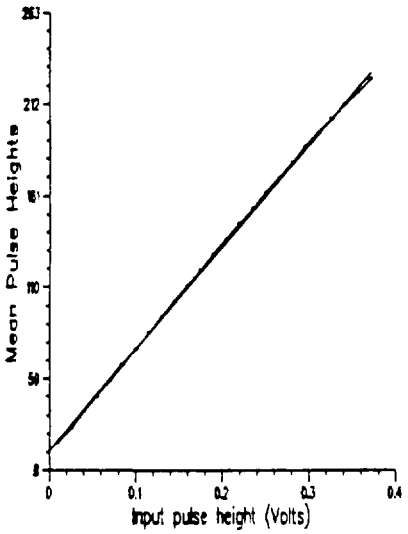

Figure 4 Gain (wide pulses)

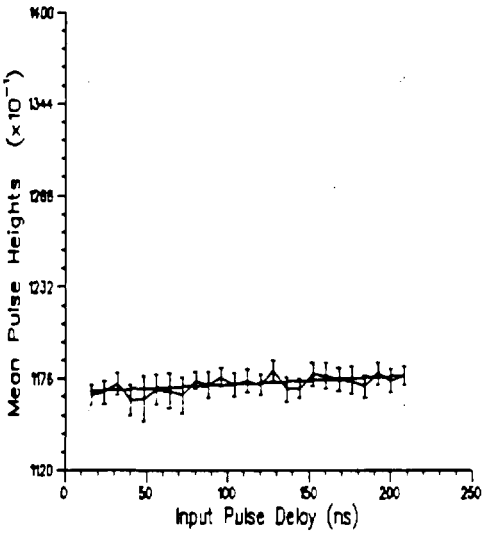

Figure 5 Delayed pulse

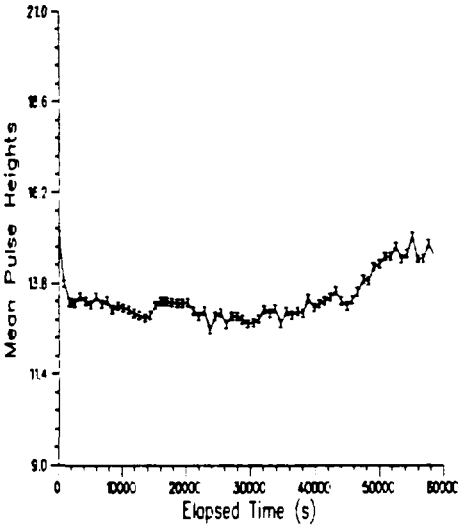

Figure 6 Pedestal Stability

number of events are collected at regular time intervals. The mean values of all valid bins are calculated, and from these a weighted mean and standard deviation are produced. These are compared with maximum and minimum values. The mean value at each time interval is plotted against elapsed time. A typical plot of the stability is shown in Fig. 6.

IV. CONCLUSIONS

A test system has been developed for a 1024 channel TD system. The test procedure was designed to require a maximum of 5 minutes per channel. This was achieved by programming the SSP to perform most of the calculation. The speed is presently limited by the host computer (a MicroVax II), which will shortly be replaced by a much faster SGI machine and FASTBUS interface [4]. The complete TD system (1024 channels) will be used to instrument the target during the January 1994 run of E787 at BNL.

V. ACKNOWLEDGEMENTS

We wish to thank the following people who developed the CCDs and associated circuitry: J. Cresswell, M. LeNoble, M. Constable. This work is supported by a major equipment grant from the Natural Sciences and Engineering Research Council of Canada.

VI. REFERENCES

[1] D. Bryman et al. IEEE Trans. Nuc. Science, Vol.38, 2, 1991
[2] A. Daviel IEEE Trans. Nuc. Science in press, 1993
[3] H. Brafman et al. IEEE Trans. Nuc. Science, Vol.32, 1,1985
[4] C.Zein et al. "A High Speed FASTBUS Interface to VME" in Proceedings of this Conference (RT93), Paper P1-16