Paper presented at 9th International Pulsed Power Conference
Albuquerque, June 21-23

TRI-PP-93-55
Jun 1993

PULSE WIDTH CONTROL AT 10^6 PULSES/SEC AND 15 kV FOR THE KAON FACTORY BEAM CHOPPER

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Abstract

A beam chopper is required in the transfer line between the 1 GeV/c TRIUMF cyclotron and the Accumulator ring of the proposed 30 GeV/c KAON Factory synchrotron. The beam chopper must generate pulses with a magnitude of at least 9.5 kV, with rise and fall times of less than 38 ns, at a repetition rate of 10^6 pulses per second, and at a 100% duty cycle. Precise control of grid timing and voltage is required at the driver tetrode to achieve deflector kick pulse widths of 48 ns and 92 ns while maintaining an interpulse and flattop ripple at less than ±10% of the deflector kick magnitude. Results of measurements are presented where all of the design criteria have been met, for the first time, over a wide range of pulse widths with subnanosecond precision. Rise and fall times of 18 ns to 31 ns have been achieved on 15 kV pulses at 0.93×10^6 pulses per second continuous operation.

Introduction

The TRIUMF cyclotron will be used as an injector for the KAON Factory synchrotron. A 1.025 MHz ($\simeq10^6$ discrete pulses/s) beam chopper is required for the injection line into the Accumulator ring [1]. The chopper will create holes of 108 ns duration in the 1 GeV/c H^- beam, by deflecting the beam to be removed, to allow enough time for the magnetic field to be established in the kicker magnets [4,3] in each of the 5 rings.

The angle of deflection Θ_e due to the electric field in the 1 MHz chopper deflector plates is given by

$$\Theta_e[rads] = arctan\left[\frac{V\times\ell}{d\times p\times\beta}\right] \quad \left[10^9 V/GeV/c\right] \qquad (1)$$

where $\beta \times c$ is the particle velocity and p is the beam momentum. The required deflection of 1 mrad can be achieved with a set of plates 5 cm (d) apart in which the product of voltage difference (V) and plate length (ℓ) is 37.7 kV·m. The deflected H^- beam bursts impinge on a stripper foil and emerge as H^+ and will be further separated from the un-deflected H^- beam by a downstream dipole magnet and directed to a 10 μA beam dump. The chopper "kick" must have a rise and fall duration (10% to 90%) of less than 39 ns on alternate narrow and wide pulses at approximately 1 μs intervals. This can be achieved if the voltage rise and fall duration (10% to 90%) is less than 38 ns [8] with 4 meter long deflector plates.

Chopper Design Concept

The beam chopper must operate continuously at a 100% duty cycle with the pulse pattern shown in Figure 1. At TRIUMF a novel design concept was developed [8,6,2] in which a 100% duty factor is made possible by employing an energy storage scheme such that the

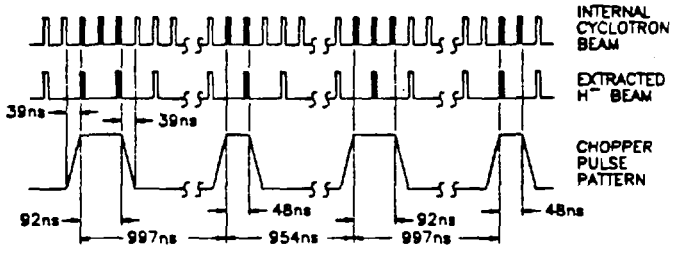

Figure 1: Beam Chopper pulse pattern synchronized with internal cyclotron beam and extracted beam

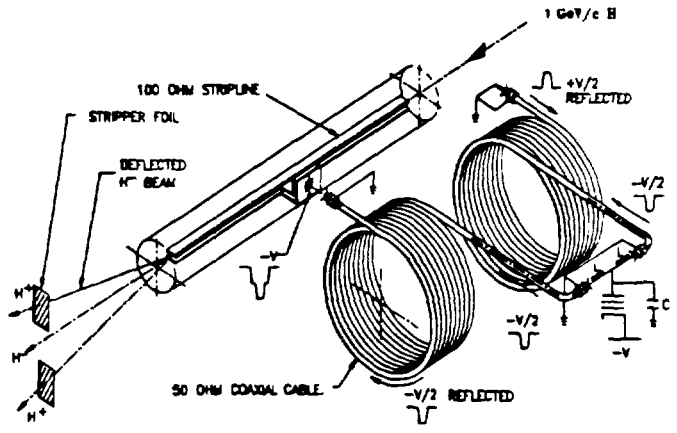

Figure 2: Schematic of prototype 1 MHz chopper

high voltage pulses can be re-used. In addition the deflector plates are open circuit, which increases the electric kick by a factor of 2, relative to terminated plates, without any consequent power dissipation due to a terminator. An alternate design concept (pulse quadrupling) has been tested in which an additional factor of 2 in pulse voltage has been achieved [9] by changing the pulse control timing.

The schematic for the latest single tetrode version of the prototype chopper is shown in Figure 2. The cathode of an EEV [7] CY1170J 75 kW tetrode is connected to a negative high voltage power supply. The anode of the tetrode is connected to two low loss 50 Ω storage cables of approximately equal delay. The storage cables are connected to the tetrode in such a way that the inductance of the connection and the stray capacitance of the tetrode appears as a segment of a lumped element transmission line with an impedance of approximately 50 Ω, ie;

$$\sqrt{\frac{2\times L}{C}} = 50\Omega \qquad (2)$$

where L and C are shown in Figure 2. The measured stray capacitance (C) from the anode to ground is 104 pF and the measured inductance of one cable connection is 127 nH. The inductance of the other able connection was assumed to be the same. This leads to an impedance of 50.9 Ω and a delay of $\sqrt{2\times L\times C} = 5.0$ ns. The remote end of one cable is short circuited and the remote end of the other cable is connected to the center of a set of open circuit deflector plates which are configured as a 100 Ω strip-line. The propagation delay in two cables can differ by ±3 ns without any significant degradation in rise time or pulse timing jitter [6,2]. Thus the system can be tuned precisely to the cyclotron frequency by simply changing the position of the short circuit stub. However once the system is tuned, the sum of the single way delays of the two cables must be constant to within about 0.2 ns.

Figure 3 shows the lattice diagram of the ideal pulse pattern at the center and at the open circuit end of the pulse storage cable for a single width pulse. Stripper foils will be mounted above and below the beam axis as shown in Figure 2 so that the polarity of the deflector voltage is not important. The control system and the measurements obtained when two widths of pulse are stored on the cable are described in references [6,5].

In this paper we are only concerned with the control of a single width of pulse in which case there are only two pulses, of the same width, travelling in opposite directions in the storage cable. In Figure 3 the path of negative pulses is indicated by dashed lines and the

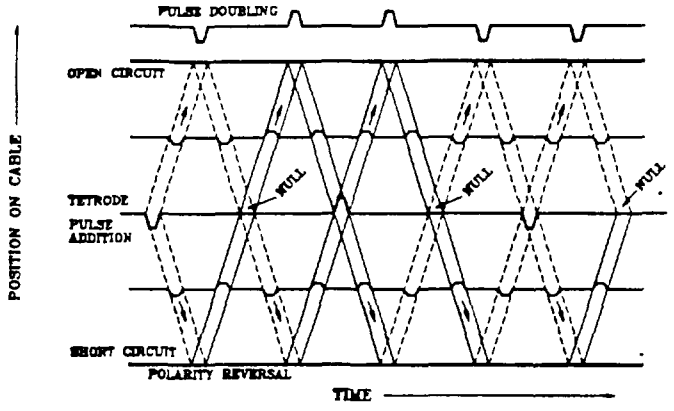

Figure 3: Lattice diagram for 1 MHz chopper

path of positive pulses is indicated by solid lines. The pulses reflected from the short circuit are reversed in polarity and those reflected from the open circuit maintain the same polarity. Alternate reflections from the remote ends of the cables cause a voltage null at the tetrode due to equal magnitude but opposite polarity pulses passing each other. When the two pulses add together as a single negative pulse at the anode of the tetrode, the tetrode is switched on to restore the leading edges (charge). When the two pulses add together as a single positive pulse, the tetrode is switched on near the tail of the pulse, to restore the trailing edges (clip). The magnitude of the stored pulses double at the deflector plates. For the final design, storage cables which have a total single way delay of 2 μs are required so that four pulses (2 wide and 2 narrow) can be stored to give a repetition rate at the deflector plates of 1 MHz. Note that the repetition rate at the tetrode is 1/2 of the repetition rate at the deflector plates due to voltage nulls.

The grid pulser consists of 8 parallel FETs that are controlled in pairs through 4 sets of fiber optic links from a computer controlled pulse sequencer [5]. Each pair of FETS drives one of four 80 ns long 75 Ω cables that are connected to the control grid of the tetrode. The measured grid capacitance is 560 pF so the time constant is about 10 ns. The coarse magnitude of the grid pulse is controlled by selecting the number of FET drivers (1 to 4) to switch on. If the pulse width from the FET pulser is less than about 30 ns (3 time constants at the grid) then fine control of the magnitude can be achieved by altering the pulse width of one or more of the FET pulsers. When the pulse width from the FET driver exceeds about 30 ns then the pulse width (at full magnitude) starts to increase at the grid. Adjustments of the grid bias D.C. power supply voltage provides further fine control.

There has been a careful examination of the circuit parameters

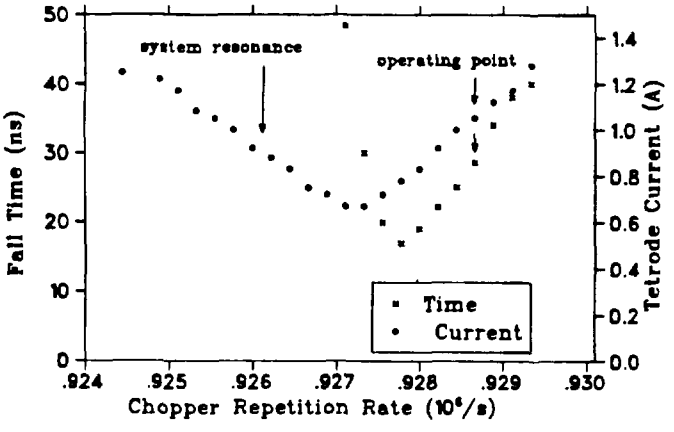

Figure 4: Measured fall time and average tetrode current vs. repetition rate

over the past year and several parasitic resonances have been identified and eliminated one by one. These resonances occurred in the filter network of the 15 kV cathode power supply, the screen grid filtering capacitors, and the charge storage capacitors for the cathode power supply which are mounted on the tube base. Extensive impedance bridge measurements and PSpice simulations provided potential solutions to eliminate the resonances. The solutions consisted of reducing stray inductances by appropriate mounting of components and installing suitable resistors to provide significant damping.

Pulse Width Control Measurements

The prototype tests on the pulse width control were carried out at a 100 % macro duty factor at a frequency of 928.7 kHz at the deflector plates. The total one way delay of the storage cables, including the 4 m long deflector plates and the tetrode connection, was 1079.8 ns when the short circuit position was adjusted so that the delays on either side of the tetrode were equal. This corresponds to a fundamental resonant frequency of 926.1 kHz when the tetrode is not operating. Figure 4 shows a plot of repetition rate vs average tetrode current and fall time of the negative anode pulse. Minimum tetrode current occurs at 927.2 kHz, and minimum fall time occurs at 927.8 kHz. The fall time of the leading edge increases sharply below 927.8 kHz. It is preferable to operate at a frequency slightly above 927.8 kHz to reduce the interpulse ripple while maintaining good rise and fall times. During operation it was noted that both the tetrode current and the transition time increased as the cable expanded in length due to heating. This is consistent with the results in Figure 4. At 18 kW the cable increased by 0.3 ns after several hours of operation corresponding to a temperature rise of 17 degrees C.

The two different pulses shown in the lower traces in Figure 5 were measured at the anode. The corresponding control grid pulses are shown in the upper traces in Figure 5 on the same time scale. The pulse width is controlled by setting the delay of the clip pulse relative to the timing of the front edge of the charge pulse and by setting the duration of the charge pulse. Thus the charge pulse is timed to restore the leading edge of the negative anode pulse and the clip pulse is timed to restore the trailing edge of the positive anode pulse. Results for various widths of deflector pulses are shown in Figure 6.

Control of the flattop of the stored pulse is carried out by adjusting the shape of the charge pulse on the grid. The voltage across the tetrode for the flattop of negative pulses is essentially zero and care is taken not to overdrive the control grid during the flattop or the screen power dissipation will be excessive.

As the pulse width is increased it is also necessary to make small adjustments in the magnitude of the clip pulse to minimize a ringing

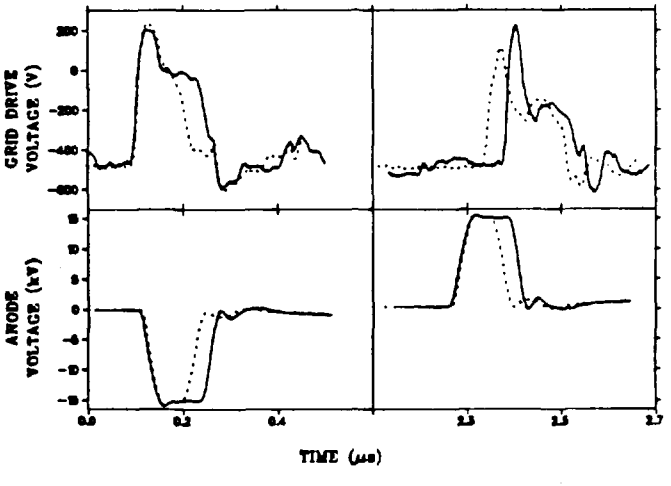

Figure 5: Measured grid pulses and anode pulses for two anode pulse widths.

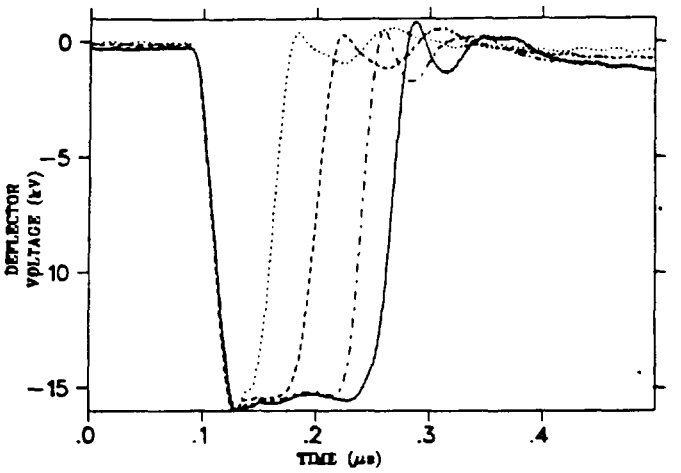

Figure 6: Measured deflector plate pulses for various control grid patterns.

effect (see Figure 6) observed at the trailing edge of the pulses. One of the goals is to reduce the interpulse ripple to less than ± 10 % of the peak pulse magnitude As the pulse becomes wider the ripple increases from ±1.25 kV with the 25 ns wide pulses to ±2.4 kV for the 120 ns wide pulses. The measured ripple is dominated by two components. One component is the overshoot and ringing at the end of each pulse, and the other component is a 232 kHz oscillation observed in the baseline of the pulses, due to excitation of the $\lambda/4$ resonance of the total delay of the cables.

Control of the back edge of each pulse is a delicate balance between an unacceptably large transition time and excessive overshoot. The balance is delicate since the voltage across the tetrode at the top of the positive flattop is about 30 kV and must swing to 15 kV and stop. The overshoot at the end of the pulses seen in Figure 6 has been reduced considerably in the past year by improving the control of the grid drive and eliminating resonances in the screen circuit. It might appear that there is still a resonance somewhere in the circuit causing the overshoot, however impedance measurements do not confirm this. The ringing is a result of manipulation of three different clip pulse delays to minimize the overshoot which otherwise appears as a single larger overshoot when the clip pulses are simultaneous.

The measured overshoot is believed to be a consequence of attenuation and dispersion in the storage cable. In order to confirm this hypothesis the chopper was operated with a charge pulse only (i.e. without a clip pulse) and the resulting voltage waveform observed at the anode is shown as a dashed line in Figure 8. Figure 8 also shows the waveform observed with a clip pulse only (i.e. without a charge pulse). In both cases the trailing edge of each pulse shows an exponential decay. However the tail of the wide charge pulse decays at a slower rate than the tail of the narrow clip pulse. The solid line is the algebraic sum of the two waveforms. Thus the overshoot is a natural consequence of the difference between two exponentials, with different decay time constants, displaced in time.

A PSpice [10] calculation was performed in which ideal pulses of differing widths were allowed to propagate through a realistic cable that has a single way delay of 4.2 μs. The lower traces in Figure 7 show three pulses of differing widths that have all been simulated as passing through identical cables. The narrow pulse simulates a clip pulse and the two wide pulses simulate charge pulses of nominal width (48 ns and 92 ns) when the clip pulse is subtracted. The decay time constant of the tail of individual pulses increases as the width of the pulse increases. The upper traces in Figure 7 were generated by subtracting a normalized clip pulse from the two simulated charge pulses so that the voltage levels of the difference between pulses were about the same (230 V chosen arbitrarily, see Figure 7) beyond the negative overshoot. The clip pulse amplitude was multiplied by a factor of 1.21 (1.1) before subtracting from the wide (narrow) charge

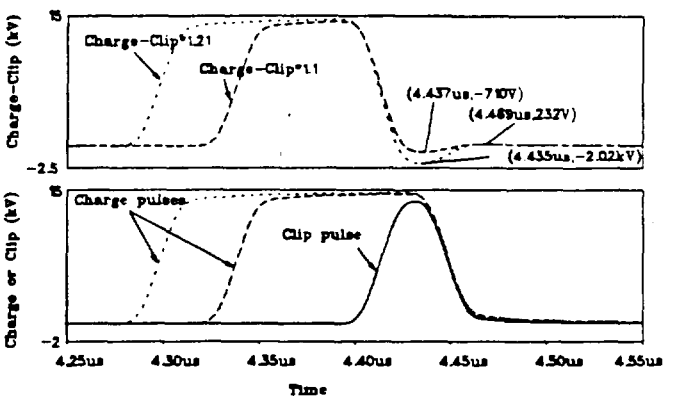

Figure 7: Calculated difference in ideal dispersed pulses of different widths.

pulse. The resultant negative overshoot is much worse for the wide pulse than for the narrow pulse in the simulation and this was what we observed in our measurements as shown in Figure 6. This simplified model demonstrates that wide and narrow pulses will have tails with differing decays and that this can account for the overshoot.

The exponential behaviour is more complicated than that described above. The shape of the tail in the measurements shown in Figure 8 is the cumulative result of 100's of reflections in the cable. Consider that each charge pulse is timed to occur at a few ns before the pulse on the cable arrives at the anode. Thus the tail of the pulse can be considered to be a superposition of hundreds of attenuated and dispersed pulse tails displaced by a few ns each; if there was no attenuation then the exponential tail would become a DC voltage with no droop, so the sum of the charge only and clip only waveforms in Figure 8 would have no overshoot. The overshoot is reduced as the operating frequency is increased above the operating frequency because this has the effect of increasing the delay of the superimposed pulses and thus flattens the exponential tail. However the rise and fall times are increased and the power dissipation is increased as the frequency is increased above the operating point so that the results shown in Figure 6 are about the optimum.

The pulse patterns for the nominal widths are shown in Figure 9, as measured at the deflector plates with the charge and clip operating together. The magnitude of the pulse heights of the four pulses in Figure 9 at the deflector plates vary by as much as 2.5 kV. The pulse patterns at the deflector plates are due to two pulses stored in the cable. It can be seen that these two pulses are of different magnitudes, ie; alternate pulse pairs are of about equal magnitudes and

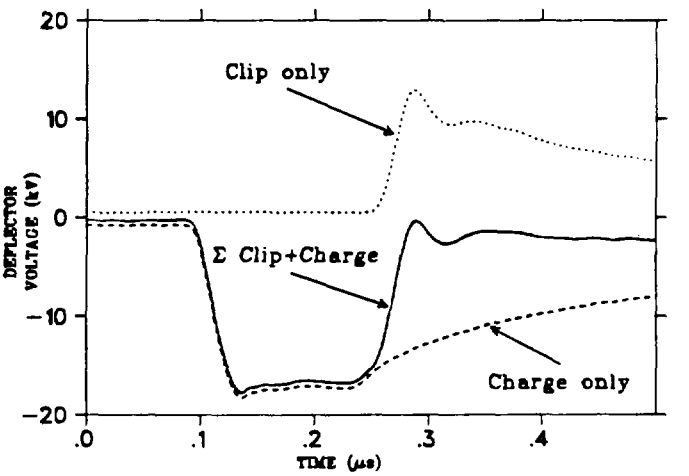

Figure 8: Measured pulses with charge only, clip only and arithmetic sum.

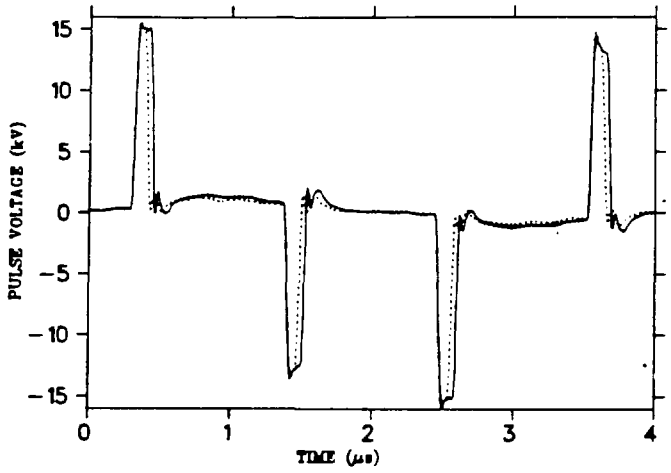

Figure 9: Measured deflector plate pulse pattern

opposite polarities but of different magnitude to the other pair. The first and third pulses in Figure 9 are actually one pulse delayed by twice the total cable delay. The second and fourth pulses in Figure 9 are another pulse delayed by twice the total cable delay (see Figure 3). These two pulses differ in magnitude by about 2.5 kV at the deflector plates. Part of this is due to a baseline 2.5 kV peak to peak, 232 kHz oscillation which results from excitation of the $\lambda/4$ resonance of the total delay of the cables. However there is still an asymmetry in pulse magnitudes of about 1 kV. This asymmetry in pulse magnitudes is being investigated and it has been determined that there is a small asymmetry in the mechanical connection of the storage cable to the tetrode which causes an asymmetry in the anode inductance. PSpice has been used to demonstrate that over a period which corresponds to several hundred pulses, an asymmetry in the anode coupling inductance causes an asymmetry in the pulses at the deflector plates.

Table 1.
Measured rise and fall times to ±12 kV of the wide and narrow pulses independently.

Pulse Edge	Measured Pulse Timing (ns)		
	δt (ns) 15-90%	Phase 15-15%	|Phase| + δt (ns)
2nd neg Narrow			
Lead	20.0	0	20.0
Trail	21.5	0	21.5
1st pos Narrow			
Lead	21.5	2.4	23.9
Trail	22.2	-3.0	25.9
2nd pos Narrow			
Lead	21.8	2.4	24.2
Trail	20.2	-3.0	23.2
1st neg Narrow			
Lead	23.2	5.9	29.1
Trail	22.0	-6.9	28.9
2nd neg Wide			
Lead	21.0	0	21.0
Trail	17.5	0	17.5
1st pos Wide			
Lead	22.0	3.0	25.0
Trail	17.5	-3.3	20.8
2nd pos Wide			
Lead	22.8	2.2	25.0
Trail	17.1	-3.9	22.0
1st neg Wide			
Lead	24.1	7.0	31.1
Trail	18.4	-7.5	25.5

Table 1 shows a summary of the leading and trailing edge durations of 4 measured voltage pulses at one end of the deflector plates for the nominal widths of the narrow and wide pulse patterns. The voltage transition (rise/fall) times (δt) shown in Table 1 are all less than 25 ns but the 'phase shifts' of the four different pulses in the pattern relative to the reference frequency of 928.7 kHz are non-zero. It is necessary for the sum of the rise(fall) time and the absolute value of the phase shift to be less than 38 ns. This sum is shown as the last column in Table 1 and it can be seen that all of the total times are less than 32 ns.

Conclusion

15 kV pulses have been generated at 0.93 MHz continuous operation with various pulse widths from 25 ns to 120 ns at the flattop. Since we require 9.5 kV for 4 meter plates it will be feasible to reduce the deflector plate length. There is an asymmetry of 2.5 kV in alternate pulses for a single width of pulse at the deflector plates which is being investigated. The rise and fall times (including phase shifts) are all less than 32 ns which is quite satisfactory compared with a maximum allowed 38 ns. The interpulse ripple is ±11% for 92 ns pulses and ±8% for 48 ns pulses. In the final version wide and narrow pulses must be interleaved for an effective repetition rate of 10^6 pulses per second. Thus the chopper will require twice the cable delay used here with less attenuation per unit length, The results of interleaving pulses were very successful as has been described for the PAC Conference in Washington D.C. in May of this year [6]. The design concept has been proven to be a success and is very close to meeting the design specifications for the KAON Factory.

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