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21 pp. 9 figs. 5 refs.

Abstract

The operation and behaviour of the RICH prototype electronics developed for the AMS-02 experiment is presented. It includes results and conclusions obtained from experimental tests data with cosmic rays.

Comportamiento de la Electrónica para el Prototipo del Detector RICH de AMS-02

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Resumen

Se describe el funcionamiento del sistema electrónico construido para el prototipo del detector RICH del experimento AMS-02. También se presentan los resultados y conclusiones de las pruebas realizadas con rayos cósmicos al prototipo.

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1. Introduction

The purpose of AMS experiment [1] is the search of primary antimatter and the analysis of extra solar primary cosmic rays spectra. In order to reach this purpose, a particle detector similar to those used in High Energy Physics terrestrial laboratories is being developed, but with the feature that it will be able to operate at a 400 km altitude orbit.

AMS comprises two missions in space. In the first one, AMS-01, the detector registered 100 hours of data on board the Discovery space shuttle in June 1998. During this stage, the detector configuration consisted in a high precision magnetic spectrometer able to identify and measure the energy of any particle going through it.

The second version of the detector, AMS-02, will be located at the International Space Station (ISS) for at least three years. One of the improvements with respect to AMS-01 is the inclusion of a Ring Imaging Cherenkov (RICH) counter, which detecting the emitted radiation of a charged particle going through a dielectric medium (Cherenkov effect) allows the measurement of the charged particles velocity and as a consequence it will improve the particle identification capability.

At present a RICH detector prototype has been built with the aim of testing on the one hand the efficiency of some components: aerogel, light guides and photomultipliers, and on the other hand the design of the data acquisition system which is going to be validated for the detector final construction.

In this document we describe the electronic system designed for the data acquisition and prototype control. We also present the results obtained during the tests made in the ISN laboratories (Grenoble) with cosmic rays.

2. Description of the prototype configuration.

In figure 1 it is shown a scheme of the configuration used in the prototype tests. Three basic blocks are distinguished:

a) Trigger system module, consisting on scintillator detectors. It provides a trigger signal to the system when a particle goes through it (event).

b) The prototype is located inside a vacuum chamber, where there are the following components:

- Aerogel: is the radiator that generates the photons when a particle goes through it.
- Light guides: they lead the photons to the photomultipliers photocathodes.
- Photomultipliers (PM´s): they pick up the photons in the input electrode (photocathode) and generate in the output electrode, anode, an electrical current proportional to the luminous intensity received. The prototype can deal with up to 99 PM´s with 16 pixels each, that is, 1584 pixels.
- Front-end electronics: consisting on the preamplifiers, that integrate the generated current and convert the integrated charge in voltage, and the ADC's that perform the digitalization. Each set preamplifier-ADC manages the signals of one PM.
- Low voltage panel: it consists of voltage regulators that supply the front-end electronics, as well as the controllers for the front-end control and data signals.
- High voltage panel: its task is to regulate the high voltage supply for the photomultipliers.
- Readout system: it consists on three boards (*Model S9007 DAQ for the AMS/Pamela experiment*) that generate the signals for the digitalization, perform the read out, process the digitalized data and store the results in memory so they can be read from the external control. Each board is connected to 33 PM´s so it manages 528 channels.
- *Piggyback* boards: They are responsible of adapting the signals to allow the interface between the readout boards and the external control. As the external control is 40 meters away from the vacuum chamber, a LVDS link has been chosen. This link consists on two 16 bits buses: a data bus (bi-directional), and a control bus (unidirectional) that allows addressing the different readout boards and each of their components, as well as the distribution of the control signals (*trigger*, read signal, write signal, bus arbitration signal).

c) Outside the vacuum chamber there is the external control that consists on:

- Personal Computer: where the control programs for the different devices of the *Guido-board* (basically FPGA's and DSP's) are running. The control program has been developed in LabView and allows FPGA's access to consult the Readout system status, to execute commands, etc. It also allows DSP's initial booting, access to internal memories for writing and reading the control variables and also depuration of the programme booted on the DSP.
- VME module: dedicated to read the registered events from the RAM memories and store the data in the hard disk for later analysis.
- Power supplies: high and low voltage, they feed the *Patch-panel*, the *Readout* boards and the *Piggyback* boards.

An important part of the work developed at Ciemat has been to set up the Readout electronics. The functionality of each component of the Readout boards is now described, with the aim of presenting the operation of the global system.

3. Basic module of reading and processing.

The Readout system consists on three CAEN boards model S9007 [2]. This is a general purpose data acquisition development board that has already been used in Pamela experiment. Each of these boards has an Altera FPGA of the APEX20KE family [3] whose main task is to control the front-end electronics and the communications between the different devices on the board, as well as the interface with the external system. Moreover it has an Analog Devices DSP of the serie ADSP2187 [4] that performs the data processing and calibrates the detector.

3.1 FPGA. Control logic of the frontal electronics and communications protocol.

An FPGA is a programmable device that allows the integration of different logic functions. Its programmable resources (logic gates and registers) are limited but can be configured with great flexibility. In the prototype design, it is responsible of the following tasks:

- **Front-end control sequence and data parallelization**. The control of the front-end electronics consists on the generation of a sequence of signals adequate to perform data conversion. Some parallelization operations and multiplexation of the 33 sets of data serialized coming from the ADCs are part of this control.

- **DSP communication protocol**. The FPGA and the DSP communicate through two protocols and dedicated buses depending on the operation to be performed:

1. External data memory. *(External Memory Overlay bus)*. When the DSP is reading digitalized data or when the results are written on the external memory through the FPGA.
2. Direct access to the internal DSP memory from an external *device (IDMA Port Bus)*. To boot the initialisation program in the DSP and accessing data and program memory to write or read parameters.

- **Communication protocol with the external control unit (PC).** The FPGA has status and control registers for the execution of commands coming from the external control. It performs also interface tasks between the external control unit and the memory (reading results, writing initial values).

3.2 DSP. Basic operational features.

A DSP is a programmable device optimised for intensive numeric processing operations. As a consequence, its architecture is less flexible that in a FPGA but it can make complex calculations in very short time.

In this prototype the DSP is responsible of processing the data that has already been digitalized by the front-end electronics. Its operation is divided in two stages clearly differentiated. The first one for data input and the second one, that is configurable, for the processing and results output.

3.2.1 Data input

Data parallelised in the FPGA are read by the DSP through the external data bus. The FPGA generates an interruption signal each time it has read the digitalized data of one pixel. The DSP performs 33 read access per interruption and needs 32 interruptions to read the data corresponding to a whole digitalization of one event. It is important to indicate that the DSP does not perform any addressing in these reading operations, but it is the FPGA that addresses the adequate register in each access.

The duration of the read cycle is 20 ns, taking place one access every 40 ns. Read data are stored in the internal memory of the DSP in a reserved zone as input buffer, that is able to store up to 4 complete events, that is, 1056x4 = 4224 words.

3.2.2 Processing and data output

There are five operation modes for the DSP: *Normal*, *Rawdata*, *Calibration*, *Wait* and *Test*. The operation mode can be selected from the external control (PC), accessing to the *mode of operation* variable in the internal memory of the DSP. Data are processed in different ways depending on the value of this variable:

- *Normal* mode: In this operation mode the DSP makes a data reduction, that is, ignores those pixels whose amplitude is below a certain threshold and eliminates the pedestal of those pixels that are over that threshold. This mode is necessary because from all data generated after a trigger only a few pixels will give information of the particle. The average value of illuminated pixels estimated in simulations for an aerogel radiator with a refraction index of 1.03 and 3 cm width is of 11.4. Using data reduction, the necessary time for the external control to read an event decreases considerably.
  Moreover this mode performs a selection of gain. The front end applies two different gains to the input signal of each pixel. We call them gain x1 and gain x5. Initially, the output data corresponds to a x5 gain. Only if the pixel is saturated at this gain, that is, the maximum range of the ADC has been reached, the output data will have gain x1. The maximum time necessary for the processing of one event is 250 μs in the worst case (every channel is above the threshold).

Once processed one pixel, the DSP writes the results in the external RAM memory.

- *Rawdata* mode: In this case there is nor data reductions neither gain selection, every pixel is directly written in the external memory. The DSP reads the data as it has already been explained, and writes them in the external memory according to a particular format. The processing time is in this case of 100 μs.

- *Calibration* mode: In this mode the pedestal and threshold tables that are used in the normal mode are calculated. Basically it calculates the average and the standard deviation of every channel when there is no signal. To make that, it is necessary a two stage calibration. First of all, 256 samples are taken and a "preliminary threshold" is calculated. In the second stage, every datum above that threshold will be ignored, as it would be data generated by a real signal and would influence the pedestal calculation. In the second stage 1024 samples are taken with a value below the threshold. This operation is performed independently for each channel. The triggers used for the calibration can be physical triggers generated by the trigger system or software triggers, generated by the external control.

- *Wait* mode: This is a non-activity mode more than an operation mode. The DSP waits until other mode is selected from the external control to start with the calculations.

- *Test* mode: In this mode the same algorithm as in the normal mode is used, nevertheless the processed data do not come from the ADC's but from the buffer where they are stored by the external control input (PC). In this mode we can check that the DSP processed data are correct.

In the first three operation modes data input is done as we have described before while in the other two modes triggers arriving to the system are ignored.

3.2.3 Initialization and DSP access.

The program and the operation parameters of the DSP are loaded from the external control (PC) in the internal memory of the DSP, using the IDMA port.

Once the execution of the program has started, the IDMA port can be used for reading or writing any position of the internal DSP memory without interrupting any of the running operations. This allows the access to the variables that are used for the different processing algorithms as well as to the threshold or pedestal tables, input *buffer*, etc. The necessary logic to operate the access through this port is implemented in the FPGA.

4. General operation of the system

As it can be seen in figure 1, the two external control modules (PC and VME) share the communication buses with the *Readout* system boards. In order to avoid conflicts, there has been established an arbitration with the PC as the master, forbidding the VME module accesses when the bus is busy. When the PC releases the bus, the VME module can use it.

At the initialisation of the system, the PC loads the *Boot* program into the DSP as well as certain configuration variables in the DSP and in the FPGA. Once the initialisation sequence has finished (*Boot* and variables), the bus is released and the system is ready for the data acquisition.

When a particle is detected a trigger signal is sent from the trigger system to the VME module, where it is distributed to the rest of the system via the control bus. From that moment the typical operation sequence is the following:

- Data acquisition
- Digitalized data transference to the DSP.
- Data processing and writing results on memory.
- Data reading by the VME module of the external control.

4.1 Data acquisition

The process of data reading is related to a control sequence of the preamplifiers and of the ADC digitalizers:

- The operations in the preamplifier start with the activation of the trigger signal and after a programmable time, with the *Hold* signal and a sequence of pulses to indicate the discharge of each preamplifier channel. Hence, it is necessary to generate a sequence with 2 initialisation pulses + 32 digitalizations.

- The whole sequence of ADCs digitalization is determined by the acquisition process and the data conversion, and also a starting up and turning off sequence of the ADC to minimise the system consumption [5]. The acquisition is a process of double sampling the analogue signal picked up at the sensors: first with a gain of x1 and then x5, so there are data related to 32 channels of the preamplifier (16 x 2 gains). In total: 1 sequence of starting up, 32 digitalizations and a turning off sequence.

After the digitalization of one channel, the FPGA stores the digitalized data in a 12-bits register. This process is in parallel for the 33 PMs connected to each board, so there are 33 registers for the ADC data.

4.2 Transference of the digitalized data to the DSP.

To begin the reading of the data coming from the ADC, the FPGA generates an interrupt signal to the DSP after each digitalization. The DSP answers with a reading data sequence over the 33 PMs. The read data are stored in the input buffer of the DSP, waiting to be processed. This process is repeated for the 32 channels of data that perform a whole event.

The read data are stored in the input buffer, located in the DSP internal memory. It is dimensioned to store up to 4 events, that is 4224 (1056x4) words. When the buffer is full, the FPGA does not accept any more triggers (so it will not generate more interruptions) and waits until the DSP releases positions of the memory as it processes data before accepting new triggers.

4.3 Data Processing in the DSP and results writing.

The DSP has to wait for the arrival of every data of one event to start the processing. This is because the ADC gives first the data relative to gain x1 and then gain x5, and both of them are necessary to perform the gain selection.

Once the DSP has processed the data according to the selected operation mode, it writes the results in the external data bus, forcing the intermediate FPGA to generate the memory writing signals.

4.4 Reading of the results via external control

The FPGA registers the activity of the system in a status register to inform the external control of the existence of relevant data in the memory. To accomplish that it activates the *Data_ready* signal when there are pending data to be read and deactivates it once they have been read by the external control.

5. Test bench and results

The prototype has been tested with cosmic rays, as they are a relative comfortable data source to test the operation of a Cherenkov radiation detector.

When a particle goes through the detector radiator it emits a certain amount of Cherenkov radiation with a well-defined angle. This angle is related to the particle velocity and to the refraction index through the following equation:

$$\beta = \frac{1}{n\,Cos\theta} \qquad (1)$$

Where:

- n is the refraction index of the radiator medium. In our case, the refraction index of aerogel is 1.03.
- θ is the emission angle of the photons of the Cherenkov radiation with respect to the direction of the particle that goes through the radiator.
- β is the particle velocity in units referred to the light velocity.

Hence, knowing the optical properties of the radiator and measuring the geometric distribution of the emitted Cherenkov photons, we can have a direct measurement of the particle velocity that has gone through the detector, as it is shown in the reconstruction diagram of the particle track in figure 2.

The first test of the detector made at ISN in Grenoble consisted on data acquisition for a period of 3 days with a trigger rate of 30 events per minute (0.5 Hz), obtaining about

200,000 registered events. Only those events without noisy information are used in the reconstruction of the particle track for the study of the prototype.

Figure 3 shows the relative position of the *hits* with respect to the intersection point of the particle measured by the track chambers. It can be confirmed in this figure the existence of rings from the accumulation of illuminated pixels to a distance from the centre of about 13 cm. as it would be expected when taking β equal to 1 in the equation (1), and assuming a distance of 43 cm between the radiator and the PM's plane. At the same time it can be observed a central peak due to the generation of Cherenkov light when the particle goes through the light guides.

The typical event contributing to this distribution consists of about 14 illuminated pixels, from which 9 are due to light produced by the track of the particle through the PM's plane. In figure 4 it is shown one of this typical events with its reconstruction. The arrow corresponds to the track of the particle reconstructed in the track chamber while the reconstructed ring is represented by the dotted line.

The analysis of the results for this first test has been satisfactory. On the one hand, the detection of Cherenkov rings confirms that the detector is operating properly. On the other hand, the agreement between the simulated behaviour and the real one is good enough to perform extrapolations for the final RICH that will be installed in AMS-02. This agreement is illustrated in figure 5, it is shown the simulated results and also the distribution of the Cherenkov angles reconstructed with the pixels identified as belonging to the ring according to the experimental data. A muon incidence spectra for sea level has been supposed. The data distribution turns to be somewhat wider than the simulation results. With respect to the measured resolution of the particle velocity per pixel belonging to the ring, the agreement between data and simulation is within 30%.

The tested prototype consists on various optical, mechanics and electronic components as it is shown in figure 6. The trigger system is made up of track chambers. Inside the vacuum chamber it can be distinguished the metallic structure that holds the front-end electronic components. This structure is done with the matrix of PM's that can be seen in figure 7. Each PM has a light guide associated and its own electronics, which has to be carefully assembled to insulate the high and low voltage supplies. In figure 8 it is shown a partial view of the final assembly of a PM, and finally figure 9 is a partial view of the three Guido-boards that constitute the data acquisition system of the prototype front-end.

6. Conclusions

At first glance, the prototype has been useful to verify the consistency of the theoretical study before beginning the construction of the final system.

On the other hand, processing of obtained data has allowed us to validate the electronics design and to make an estimation of the detector resolution.

Concerning the electronic specific objectives it has been proved the proper operation of certain modules of the data acquisition system as the front-end electronics, low voltage

Patch-panel, FPGA digitalisation logic and the processing and calibration algorithms of the DSP.

Finally, the present work has reached its objective of setting up and tuning the prototype electronics for the AMS-02 experiment RICH subdetector.

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[3] "*APEX 20K Programmable Logic Device Family*". Altera datasheet. November 1999, ver 2.05.

[4] "*DSP Microcomputer ADSP-2187L*". Analog Devices datasheet. 1998.

[5] "*AD7476/AD7477 1 MSPS, 12-/10 Bit ADCs in 6-Lead SOT-23*". Analog Devices datasheet. 2000.

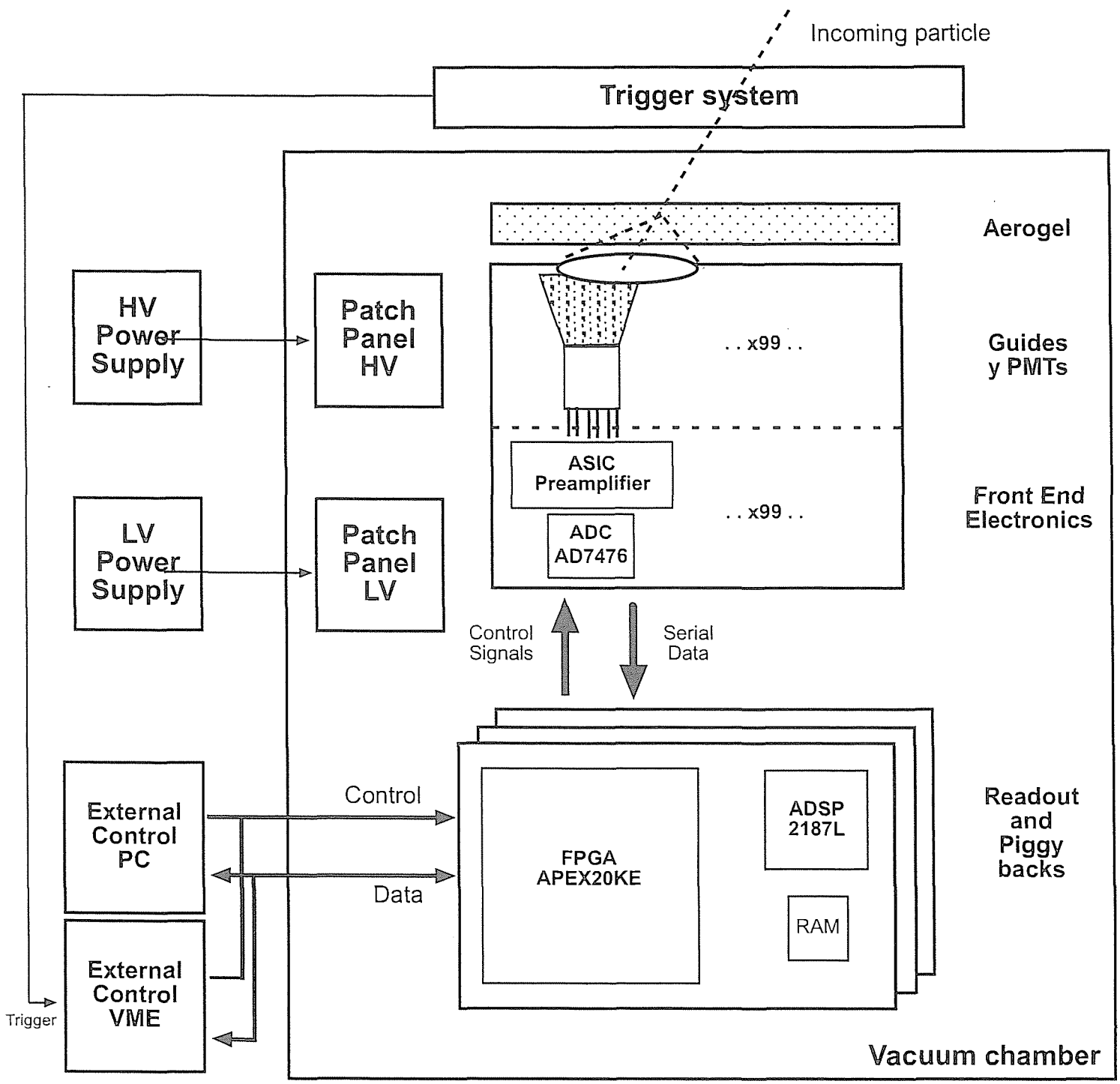

Figure 1: Block diagram of the RICH prototype test setup

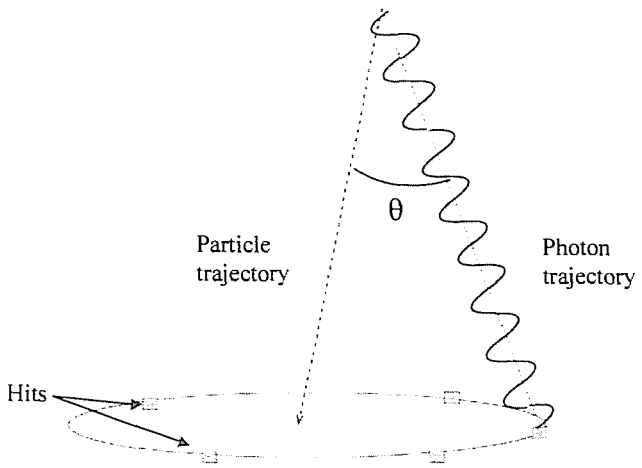

Figure 2: Reconstruction diagram

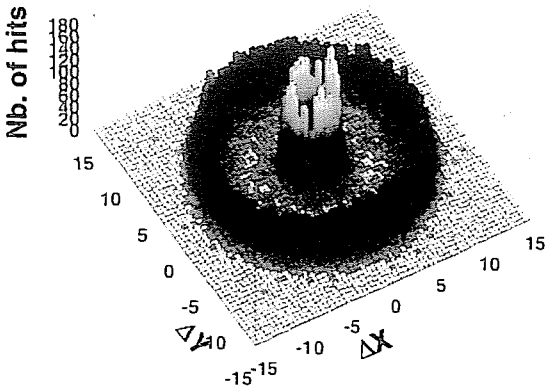

Figure 3: Accumulated statistics for the Cherenkov rings

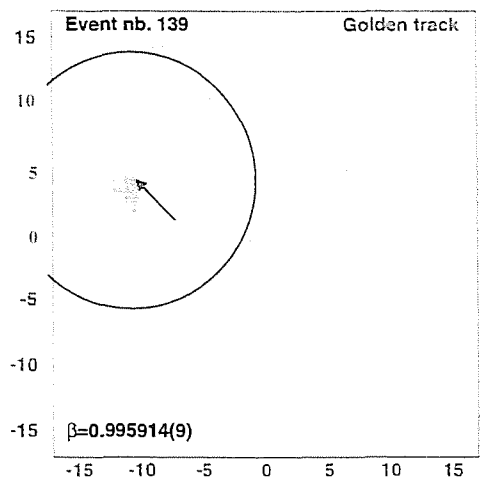

Figure 4: Typical event of the prototype.

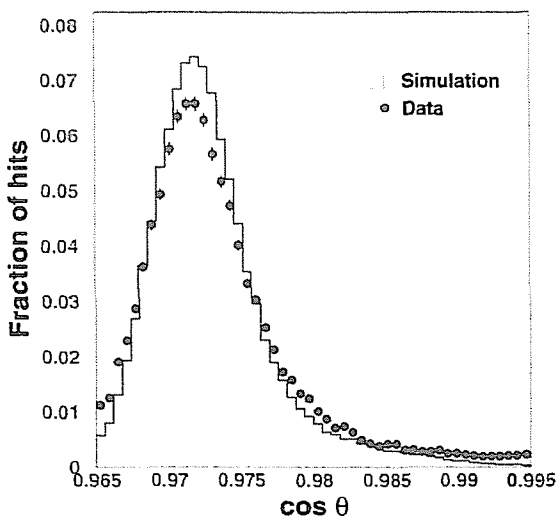

Figure 5: Reconstructed angles distribution.

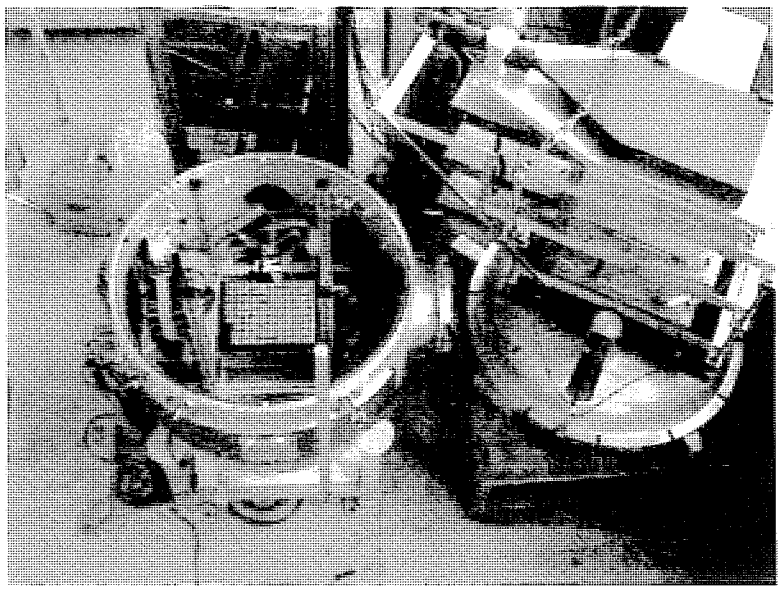

Figure 6: Global view of the RICH prototype test setup

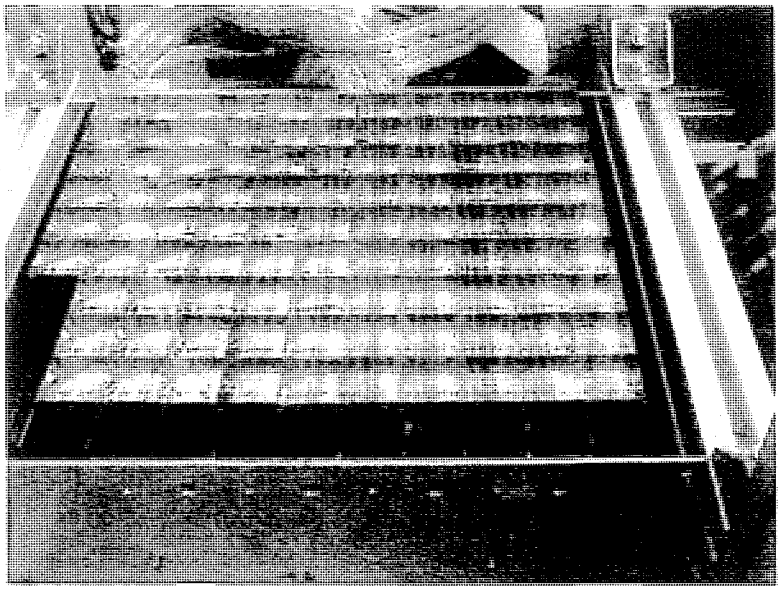

Figure 7: Global view of the photomultipliers matrix

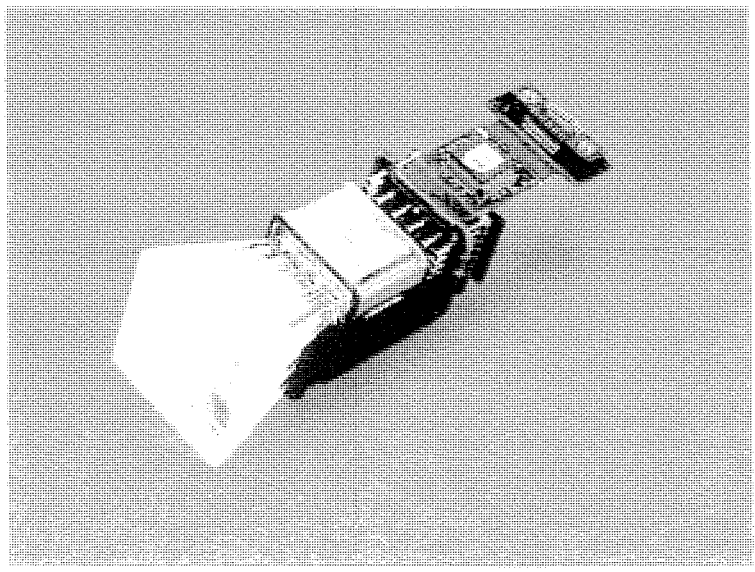

Figure 8: Detailed view of the final assembly of a photomultiplier

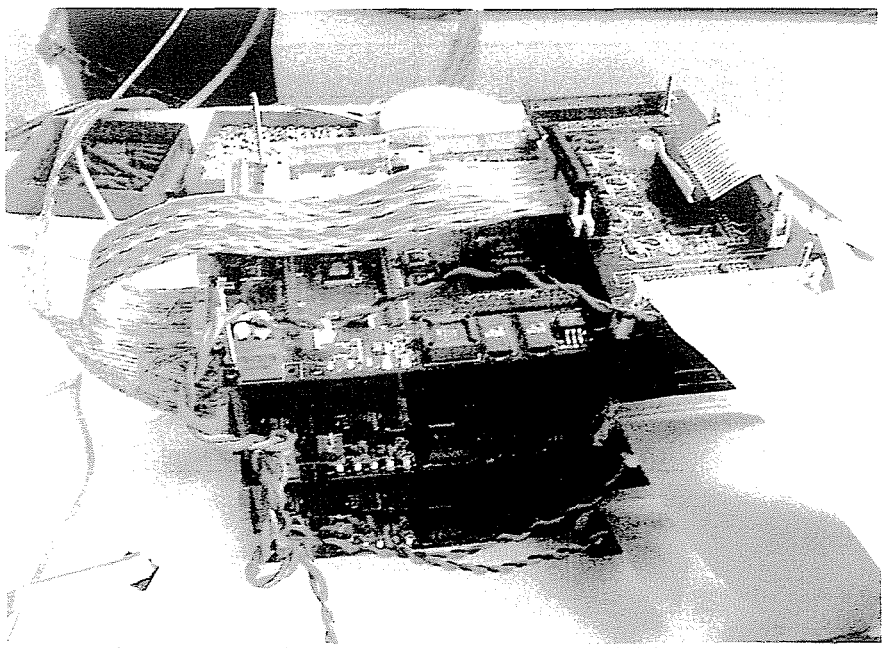

Figure 9: Detailed view of the data acquisition system