10.11 A New RF System for the CEBAF Normal Conducting Cavities

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Abstract

The CEBAF Accelerator at Jefferson Lab is a 6 GeV five pass electron accelerator consisting of two superconducting linacs joined by independent magnetic transport arcs. CEBAF also has numerous normal conducting 499 MHz cavities for beam conditioning in the injector and for RF extraction to the experimental halls. For these cavities, a new, digital RF system is under development, using an FPGA containing the feedback algorithm. The system is based on digital down-conversion, quadrature under-sampling of 70 MHz IF frequency with 56 MHz clock. Long studies demonstrated effectiveness of this method. The VXI bus/crates were chosen as the operating platform.

RF System

The new RF system will control the chopper and separator, (both beam deflecting) cavities. The field control requirement is relatively undemanding at 1% and 1 ps phase accuracy. In the case of the chopping cavities, the field is rarely changed in contrast to the separator where amplitude is adjusted according to the deflection needed for different beam energies. Figure 1 shows a block diagram of the low level RF control system (LLRF). This type of architecture has become a common model for single cavity control system equipped with a number of RF inputs and outputs, utilizing a modern field programmable gate array (FPGA). VXI platform was chosen because of good RFI/EMI properties and EPICS (software) control system compatibility. In RF front/end system 499 MHz cavity frequency is converted down to IF=70 MHz. This assures compatibility with existing CEBAF LLRF system. The IF signal is quadrature demodulated using harmonic under-sampling 56 MHz, processing in the FPGA, digitally recombined, filtered and up-converted to the cavity frequency. The feedback loop is equipped with PI algorithm and the entire system operates as a digital generator driven resonator (GDR). To assure system stability over 360 deg phase range, rotation matrix for I and Q vector is implemented.

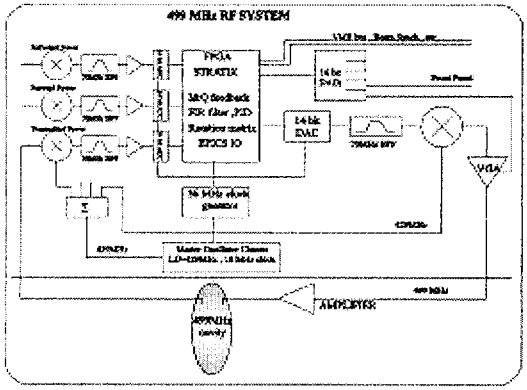

Fig. 1 RF system block diagram.

RF Receiver/transmitter

RF front/end had to fulfill number of strict requirements concerning linearity, dynamic range, temperature drift, noise, group delay. Thus, high IP3 and high dynamic range FET mixer WJ HMJ5 was chosen. To minimize temperature related drifts a product called Thermopads is being considered (attenuator with selectable tempcos). 70MHz commercial bandpass filter, was selected for its low~80 ns group delay. Isolation channel is also a concern; we specified this to be at least 60 dB for the cavity transmitted power and 50 dB for all other channels. The receiver has been modeled and tested in a variety of ways e.g. with System View (commercial software for RF design).

VXI Motherboard

The VXI motherboard contains the electronics necessary to process digital signals, interface to VXI bus and 10/100 Ethernet. The board features one Altera Startix FPGA, 64x16 DPRAM, 1Mx32 RAM, 1Mx32 FLASH, 56 MHZ PLL based clock generator, 6 x 16 –bits/ 500 Ksamp. DACs, 10/100 Ethernet, digital I/O, Infrared I/O. We chose Altera Stratix FPGA with 18000-25000 logic elements (basic electronics building blocks), 80–8 bit multiplier/accumulator, supporting both hard coding and a soft microprocessor core (NIOS). Various operating systems including Linux can be loaded and with Ethernet support, the board can communicate with EPICS directly. Care was taken in the design of the 56 MHz clock /PLL The characterization of phase noise (timing jitter) of clocking sources has become crucial due to their direct impact on the performance of the data conversion devices (ADC and DAC). Special phase noise measurement with Vector Signal Analyzer was developed and tested [2].

Model & system control

System control was modeled and tested for a variety of cavity scenarios e.g. separator cavity with Q_L=2500 or chopper cavity with Q_L=10^4. This ultimately affects the loop bandwidth and hence the gain parameters of the LLRF system. We used Matlab and Simulink to model the step response of RF system. The model of warm cavity contains a controller, a cavity and cable/digital delay. The cavity is modeled by its fundamental mode using the resonant cavity equivalent circuits equations.

[1] C.Hovater et al., "A New RF System for the CEBAF Normal Conducting Cavities", 2004 LINAC Conf. Proc. Luebeck ,Germany

[2] T.Pławski, C.Hovater, "Precision Phase Noise Measurement Using Agilent 89410A Vector Signal Analyzer", 2005 JLAB-TN-05-001

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