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MEASUREMENTS ON A FET BASED 1MHz, 10 kV PULSE GENERATOR

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Abstract

A prototype pulser, which incorporates thirty-two 1 kV Field-Effect Transistor (FET) modules, has been built and tested at TRIUMF. The pulser has been developed for application in a scheme for pulsed extraction from the TRIUMF 500 MeV cyclotron. Deflection of the beam will be provided by an electric field between a set of 1 m long deflector plates. The pulser generates a continuous, unipolar, pulse train at a fundamental frequency of approximately 1 MHz and a magnitude of 10 kV. The pulses have 38 ns rise and fall times and are stored on a low-loss coaxial cable which interconnects the pulse generator and the deflector plates. The circuit performance was evaluated with the aid of PSpice in the design stage and confirmed by measurements on the prototype. Temperature measurements have been performed on 1 kV FET modules under DC conditions and compared with temperatures under operating conditions to ensure that switching losses are acceptable. Results of various measurements are presented and compared with simulations.

I. Introduction

There is an application at TRIUMF for a kicker system operating with 9 kV unipolar pulses at approximately 1 million pulses per second (referred to as 1 MHz in this paper) continuous for a $\mu \rightarrow$e conversion experiment[1]. The present proton beam from the 500 MeV cyclotron consists of pulses with a period of 43.4 ns and a width of 4 ns. The modulator specifications[1] call for a deflection voltage up to 10 kV, a pulse flat-top duration of 178 ns and a repetition rate of 922.6 kHz (23.065MHz/25) which is synchronized to the 23.065 MHz RF which drives the Dee-gap of the TRIUMF 500 MeV cyclotron. The rise and fall times (10 % $\rightarrow$ 90 %) are not to exceed 40 ns. The deflector will consist of two plates, 1 m long, with a separation of 30 mm. The deflector plates will have an impedance of 100 Ω, and will be center fed to match the impedance of the storage cable.

Various versions of a prototype 1 MHz beam chopper were designed and built for the now defunct KAON Factory using 50 Ω energy storage cables to improve efficiency. A bipolar 15 kV pulser[6] was built in which rise and fall times of less than 40 ns were achieved. However the requirements for the present application are for a unipolar pulse pattern. In another version[5] unipolar 7 kV pulses were generated at 1 MHz, using two 150 kW tetrodes in push-pull, and stored on a 50 Ω cable. However the rise and fall times (~100 ns) were limited by the excessive stray capacitance of the tetrode driver circuit. A 6 kV 20 kHz FET pulser[3],[4],[10] was designed, built and installed in the TRIUMF injection line in 1994. A FET pulser has a much reduced stray capacitance compared with the tetrode version and permits the storage of unipolar pulses on a cable without excessive power drain, while maintaining good rise and fall times. A new FET pulse generator has been developed which is based on previous TRIUMF designs: namely the 6 kV 20 kHz FET pulser and the 1 MHz beam chopper that was developed for the KAON Factory.

II. Design

The pulser consists of a high-voltage modulator installed in a large metal cabinet, incorporating two stacks of 1 kV modules operating in push-pull mode. Each stack has 14 FET modules in series. The high-voltage FET utilized in each module of the pulser is the APT1004RBN[8]. There is a single turn pulse transformer on each final stage module consisting of two series Amidon FT240-43[9] ferrite transformer cores. The pulser drives a low loss 50 Ω storage cable which serves as a broad band resonator. The storage cable also serves to transmit the voltage pulses to the deflector plates which will be installed in the cyclotron, thus keeping the sensitive electronics out of the high radiation environment in the cyclotron vault. The operation of the pulser system was simulated extensively with PSpice[11] for various circuit configurations before a feasible design could be found[2].

The solid state modulator consists of a signal conditioner and three stages (see Figs. in reference[2]) to

convert a 5 V, 23 MHz RF signal to 10 kV pulses at 922.6 kHz. The signal conditioner divides the frequency of the cyclotron RF signal by 25 to provide a TTL signal at 922.6 kHz. The first stage converts the TTL signal to 5A, 130 V to drive two second stages in parallel. The second stages each consist of two modules operating in push-pull, which are identical to the cards in the high voltage stacks except that there is one ferrite transformer core per card in the second stage and two ferrite transformer cores per card in the final stage. Each of the second stages convert the 130 V signal to ± 3 A at ± 500 V to drive the primary transformer windings of each of the two final stage stacks of high voltage FETs. The final stage generates a -10 kV pulse at the input to a 10 cm diameter low loss 50 Ω coaxial storage cable. The remote end of the storage cable is an open circuit and the pulses are reflected back to the modulator. The length of the storage cable must be adjusted such that the returning pulses are properly timed with the modulator pulses to optimize the rise and fall times. The optimum operating frequency of the prototype is 924.8 kHz rather than 922.6 kHz due to the fixed length of the storage cable. A coaxial trombone will be installed in line with the storage cable to permit precise tuning relative to the cyclotron RF.

The two stacks of the final stage each consist of 14 modules. The 14 modules of the pull-up stack are labelled UP1 through to UP14 (see Fig. 1 of reference[2]). UP1 is at the ground end of the stack, and UP14 is at the output end. The 14 modules of the pull-down stack are labelled DN1 through to DN14. DN1 is at the HVDC end of the stack, and DN14 is at the output end.

A grading resistor network connected between the drain and source of the APT1004 FET ensures that the DC voltage grading down the stack of FETs is adequate. A grading resistor of value 330 kΩ (four series/parallel 330 kΩ resistors, each of 2 W) provides adequate current ($\sim$ 2.2mA) for LEDs, which are connected in series with the DC grading resistors for diagnostic purposes (see Fig. [2]) of reference[2]). Provision has also been made on the PCB cards for high-speed fibre optic transmitters which could be used for diagnostic purposes.

III. Parasitic Capacitance

The parasitic capacitance of each module is comprised of several components. The predominant components being: the linearized drain-source capacitance of each APT1004, during pulsing, which is 90 pF[3], the capacitance between the primary and secondary of the pulse transformers, and the capacitance between the stacks and the cabinet. The parasitic capacitance significantly affects the transient voltage and power distribution down the high-voltage stacks as well as the rise and fall times of the pulses. The parasitic capacitance from each card to ground can result in a drain-source voltage at the output end of the FET stack that is more than 4 times larger in magnitude than that at the 'DC' end of the stack, if corrective measures are not taken[2]. The voltage transients in the stack are approximately equalized by connecting fast-grading capacitors with a range of values (C_{fg}) between the drain and source of the APT1004 FET at each module. The calculated values of the fast-grading capacitors which would give good power distribution in the stacks are given in reference[2]. The fast grading capacitors vary from 6 pF to 206 pF.

In order to avoid excessive drain current in the APT1004 FET during turn-on it is necessary to connect a fast-grading resistor (R_{fg}) in series with each fast-grading capacitor. The nominal value of this resistor is 200 Ω for levels 1 to 12 in both stacks. The commercial batch of resistors were sorted such that the resistance values decrease towards the output end of the stacks. The upper two modules have even lower valued fast-grading resistors[2]. The fast-grading capacitor and a 90W fast grading resistor are mounted adjacent to the corresponding PCB card and are electrically connected on the back-plane.

The size and geometry of both the FET modules and metal cabinet, which houses the FET stacks, were chosen such that the parasitic capacitance from each module to ground is reasonably low. The spacing of the modules within a FET stack is a compromise between the length of the stack, and hence the parasitic capacitance to ground, and the need to cool the modules and associated resistors, and electrically isolate the modules from one another. The approach utilized to estimate the total parasitic capacitance (C_{stacks}) of the FET stacks to ground, was to determine the volume of both the stacks and cabinet, and then calculate the equivalent radii of spheres which have the same volumes. The total parasitic capacitance of the FET stacks, approximated as two concentric spheres, without the primary winding of the pulse transformers present, is then determined from:

$$C_{stacks} = 4 \times \pi \times \epsilon_0 \times \frac{r_1 \times r_2}{r_2 - r_1} \tag{1}$$

where r_1 and r_2 are the equivalent radii of spheres which have the same volume as the FET stacks and the

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ground planes inside of the metal cabinet, respectively.

In order to confirm that the approach proposed for estimating parasitic capacitance of the FET stack to ground was valid, Eqn. 1 was utilized to determine the total parasitic capacitance to ground, without the primary winding of the pulse transformers present, for the 6 kV[3],[4] modulator: the total stray capacitance calculated from Eqn. 1 was only 7% (1.5pF) lower than measured.

The size of the metal cabinet which houses the FET stacks is quite large, such that the parasitic capacitance from each module to ground is a small fraction of the drain-source capacitance. The outside dimensions of conducting material of the two stacks is 0.25 m × 0.45 m × 0.70 m and the approximate dimensions of the location of the ground planes which are close to the two stacks are 0.8 m × 1.7 m × 1.7 m. This leads to a calculated capacitance from Eqn. 1 of 44 pF or 1.6 pF per level, not including the capacitance through the transformer: a value of 1.5 pF per level was used in the PSpice simulations several months before the system was built. The capacitance to ground through the ferrite transformer cores was 0.75 pF[2] per level for the PSpice simulations.

When the system was built the measured capacitance from the stacks to ground was 50 pF with all 28 modules shorted together and the primary transformer winding removed. Thus the calculated capacitance was only 10% lower than the measured capacitance. The capacitance measured with the primary transformer windings connected to ground is 67 pF. Thus the capacitance of the transformer windings adds 0.6 pF per module for a total capacitance of 2.2 pF per module. However since there is a re-distribution of the charge the actual capacitance through the transformer is slightly higher than 0.6 pF.

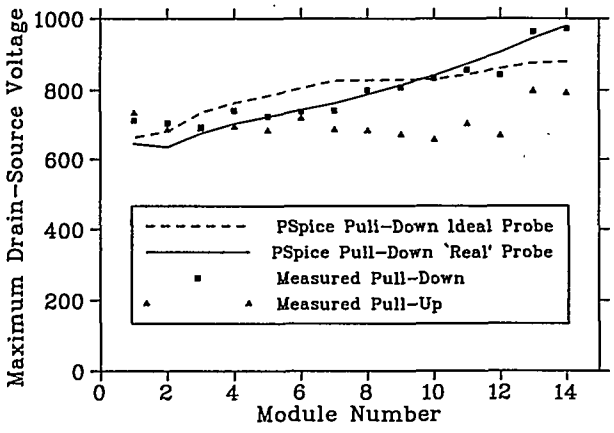

Fig. 1. Maximum calculated and measured drain to source Voltages for 10kV pulse operation.

The capacitance (~3pF) associated with a high-voltage measurement probe results in an apparent voltage distribution in the FET stacks which is different from the actual distribution when the probe is not present. Hence PSpice simulations were carried out to assess the effect of the capacitance of a single 3pF probe upon the maximum voltage of a module in the FET stacks. The PSpice simulations were run with the 3pF probe capacitance first on the drain and then on the source of each module. The predicted maximum voltage distribution in the pull-down stack for a 'real' probe (3pF) is plotted as a solid line in Fig. 1, together with the predicted voltage with an ideal probe (0pF) present, shown as a dashed line. The calculated change in voltage due to the 3 pF of the measurement probe decreases with module number from ~100 V across module UP14 to 0 V across module UP10: and is approximately 70 V low for most of the modules (UP3 to UP8) towards the DC end of the FET stack.

The pulse voltage was set to 7.5 kV for the voltage grading measurements, and the nominal pulse width was 178 ns at 924.8 kHz. 7.5 kV pulses were considered to be large enough such that the drain to source small signal capacitance would be in a linear region and hence permit a reasonable extrapolation to 10 kV pulses. The data shown in Fig. 1 was normalized to 10 kV. The measured voltage distribution in the pull-down stack is shown as solid boxes and in the pull-up stack is shown as solid triangles (un-corrected for the influence of the probe). The measured voltage data points are in reasonable agreement with the calculated voltages with the 'real' probe. The maximum (un-corrected) transient voltage (970 V), immediately following turn-off of the pull-down stack, occurs across the APT1004 FET in module DN14. By inspection of Fig. 1, the actual voltage distribution is very close to the PSpice predictions. None of the FET voltages exceed 900 V when operating with 10 kV pulses without a probe present.

IV. Heat Dissipation

The pulse generator has been tested at 925 kHz with pulsed voltages up to 10 kV. The rms current through the FETs, the fast grading components and the current limiting resistors is proportional to frequency and

proportional to the square of the pulse voltage.

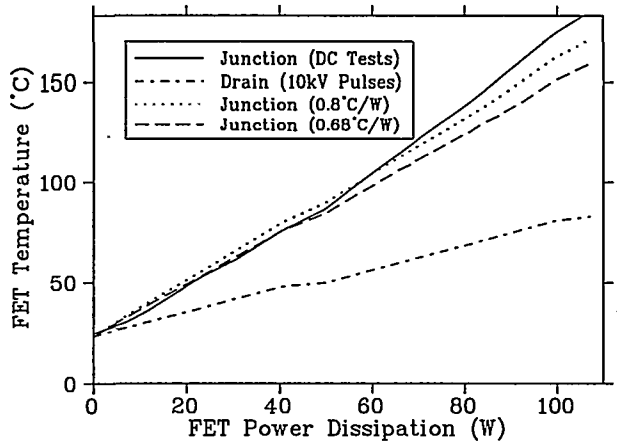

Fig. 2. Measurement of FET junction temperature vs power

The fast-grading capacitors are ceramic capacitors which are rated at 3 kV. Pulse tests on the capacitors show that with an RMS current of 1 A and 1.2 A the case temperature rose by approximately 20°C and 30°C above ambient, respectively. In order to ensure a long reliable life for the fast grading capacitors, they are connected in parallel such that the RMS current through an individual capacitor does not exceed 0.5 A.

At 25°C the APT1004 FET is rated at 1 kV, a pulsed drain current of 17.6 A and a power dissipation of 180 W (providing the case temperature is at 25°C). PSpice calculations showed that the power dissipation per module could be as high as 80 W[2]. A series of tests were performed on copper and aluminum heat sinks with various geometries and surface areas. The size of the heat sinks could not be too large since the physical size of the FET stacks has too be kept small in order to minimize the stray capacitance. In the final design a copper heat sink was chosen with dimensions of 1" x 2.5" x 3" and a surface area of 77 in^2. The FET stacks were cooled with a bank of twelve 235 cfm fans placed 18" away. The air flow was measured to be at least 600'/min. past each of the heat sinks and the power resistors.

There are two sets of 14 resistors whose value is 36 Ω on the pull-up stack and 24 Ω on the pull-down stack[2]. These are rated at 180 W in still air and interconnect the source of one module with the drain of the adjacent module: the power ratings increase by a factor of 4 with an air flow of 600'/min. The 180 W resistors are mounted adjacent to the corresponding module and are electrically connected on the back-plane. The purpose of these resistors is to limit the power dissipation and the peak drain current through the power FET's to within the rated values. The fast-grading resistors are rated at 90 W in still air and are also mounted adjacent to the corresponding module. The calculated power dissipation in some of these resistors is as high as 150 W[2].

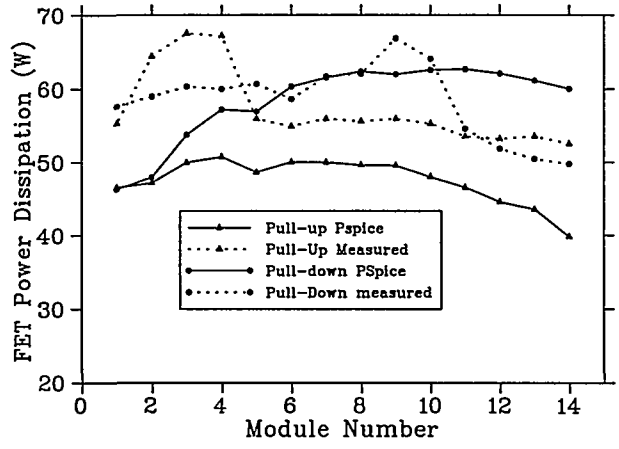

Fig. 3. Measured and Calculated FET power dissipation for 10 kV pulses at 925 kHz

The current in each FET stack was determined for 7 kV, 177 ns wide pulses, by measuring the voltage drop across the 24 Ω and the 36 Ω resistors. The measured peak current extrapolated for 10 kV pulses is approximately 10 A, well within the rating of the APT1004[8].

The second stage resistors consist of four banks of 6*180 W resistors. Each of the banks dissipate up to 500 W and are mounted below the two main stacks in an air flow of 600'/min. Due to the pulse width the power dissipation is 4 times higher in two of the banks than in the other two banks. The 'cold' resistor values of all 4 banks were selected appropriately such that the 'hot' resistor values are correct.

The thermal properties of the FETs were determined under controlled DC operating conditions and are shown in Fig. 2 for a FET installed in the cabinet with the proper air flow (600'/min). The drain to source resistance was measured as a function of power dissipation. The FET junction temperature was then determined from the temperature and current dependence of the drain to source resistance[8] and is shown in Fig. 2 as a solid line. The temperature of the drain was also measured as a function of FET dissipation and is shown in Fig. 2 as a dot-dashed line. The APT specifications[8] for the drain to junction thermal resistance is 0.68°C/W. The dashed line

is the junction temperature calculated from the drain temperature with a thermal resistance of 0.68°C/W. The dotted curve is calculated with a thermal resistance of 0.8°C/W which is consistent with the junction temperature determined from the drain to source resistance for our measurement setup.

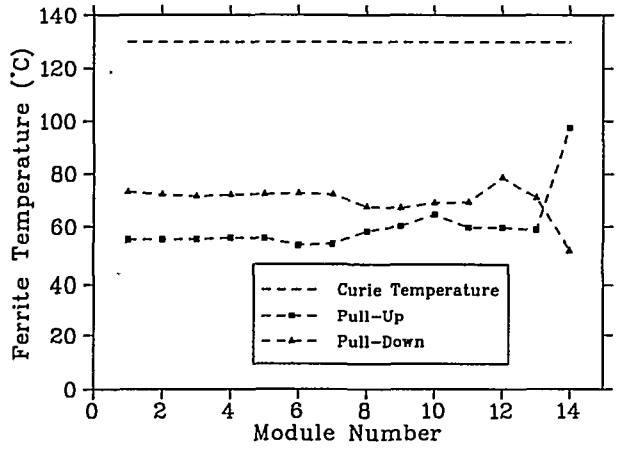

Fig. 4. Measured ferrite temperatures for 10 kV pulse operation

It is not feasible to measure the temperature of the FETs when the system is pulsing but it is quite easy to measure the drain temperature for a period of time after turning off the pulser and the fans and extrapolate back to the time of turn-off. A set of calibration measurements were made under DC conditions at different power levels as a function of time after turning off. The results showed that the drain temperature changes very slowly 60 sec after turn-off. A calibration factor was measured which permits the temperature rise above ambient after turn-off to be extrapolated back to the temperature rise during operation. The calibration factor is $3.33W/°C$, 60 s after turn-off, and is independent of the power level in the 40W to 100W range. Thus we were able to obtain an indirect measurement of the FET power dissipation by measuring the drain temperatures after turn-off. The measured results are shown in Fig. 3 as dotted lines for 10 kV pulse operation. The power dissipation in the FETs in each stack is quite uniform and varies from 50W to 68W. At 68W the junction temperature would be 120°C (see Fig. 2). The mean life time of a FET with a junction temperature of 120°C would be an order of magnitude longer[12] than a FET with a junction temperature of 150°C. The PSpice calculations on the distribution of power in the FET stacks are also shown in Fig. 3 as solid lines. The average of the calculated and measured losses were the same for the pull-down stack but the calculated losses were approximately 10 W lower, per module, for the pull-up stack. There were also some voltage and current measurements which were made to cross-check the power dissipation, and there was good agreement for modules 1 and 2, where the signals are relatively easy to measure.

One of the critical elements for which heating could be a problem is the ferrite transformers. In order study the ferrite losses, the Q of the ferrite and the dielectric losses were measured using a vector impedance meter. The Amidon FT240-43[9] ferrite cores were obtained from two different batches and one batch is more lossy than the other. When the high voltage is off the ferrites do not heat up appreciably so ferrite losses due to the magnetic components of the primary drive are not a problem at 1 MHz.

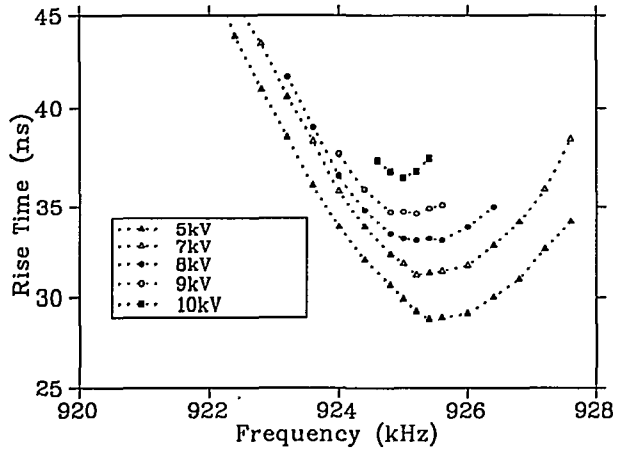

Fig. 5. Rise time vs pulse voltage and frequency

The dielectric losses however, could be quite serious. When a pulse from the storage cable is imposed on the source of the FET a displacement current flows through the capacitance of the ferrite core, causing dielectric heating. In order to reduce this stray capacitance there are two ferrite cores in series. The largest dielectric losses occur in modules closest to the output end of the stacks and thus ferrites from the batch with the lowest losses were installed in these locations. The ferrites in module UP14 get much hotter than all of the other modules as shown in Fig. 4. The heating on the UP14 ferrites was controlled by increasing the air flow in this region and also by electrically connecting an aluminum plate to the source of UP14 and mounting the plate over the ferrites. When the plate is positioned correctly the electrical field distribution above the ferrites is altered such that the displacement current through the ferrites is reduced. Fig. 4 shows the ferrite temperatures on each module after 20 minutes of 10 kV pulse operation. The maximum ferrite temperature was 97°C on UP14 and the next highest temperature was only 80°C. The Curie temperature for FT240 ferrites

is 130°C which is well above the highest measured ferrite temperature for 10 kV pulse operation. In addition the temperature of the ferrite on UP14 is only 83°C for 9 kV operation which is the expected operating voltage.

V. Pulse Measurements

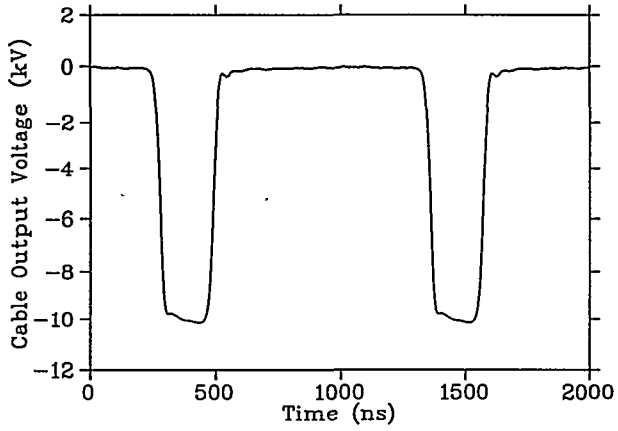

Fig. 6. -10 kV pulses at 924.8 kHz with 38 ns rise and fall time

The measured voltage waveform at the open circuit end of the storage cable is shown in Fig. 6. The pulse height is -10kV at 924.8 kHz, and the flat-top duration of the pulse is 177 ns. The voltage probe was calibrated and the measured results were compared with measurements performed with a capacitive pickup and calibrated integrator[7]. The results of the two measurements were within 1 ns for the rise and fall time.

The measured rise and fall time of the pulse voltage is 38 ns and is virtually independent of flat-top duration in the range from 50ns to 500ns. Fig. 5 shows the rise time as a function of pulse voltage and driving frequency. Since the rise and fall times degrade with increasing voltage, the frequency range which gives acceptable rise and fall times becomes smaller as the voltage is increased. For 9kV pulses the operating range is from 924.0 kHz to 925.6 kHz which corresponds to a change in the trombone tuning range of ± 0.9 ns.

VI. Conclusion

A pulse magnitude of 10 kV has been obtained in a prototype pulser at a frequency of 924.8 kHz with rise and fall times of 38 ns at the open circuit end of a low loss 50 Ω coaxial cable. Measurements on the basic 1 kV FET module at 1 MHz as well as calorimetric measurements on the FET modules agree with PSpice calculations for the power dissipation, which is within the specifications of the FETs. The measured voltage grading is also in excellent agreement with the PSpice predictions. The storage cable improves the rise and fall times of the pulses[2]. The system will be connected to a set of deflector plates installed in the TRIUMF cyclotron for beam tests later this year.

Acknowledgements

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