DESIGN AND SIMULATION OF VOTING AND PROTECTIVE LOGIC SUB MODULES (V&PL) FOR NUCLEAR POWER PLANTS

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ABSTRACT

V&PL is one of the importance modules in Reactor Protection System (RPS). In Nuclear power plant, V&PL sub modules output is high when any two input of four inputs are high. This paper design and simulate V&PL sub modules using LTspice IV software. N-channel Metal Oxide Semiconductor (NMOS) and p-channel Metal Oxide Semiconductor(PMOS) were used to design Complementary Metal Oxide Semiconductor(CMOS) gated. Thus all the gated was applied to design V&PL sub modules. This design concept practiced bottom up design rule. At the end, this V&PL function correctly as expected.

OBJECTIVE

1) Designed V&PL sub modules for nuclear power plants.
   I. Produce truth table for V&PL
   II. Simplified V&PL designed using K-Map
2) Simulation V&PL using LTspice IV and verify using truth table.

INTRODUCTION

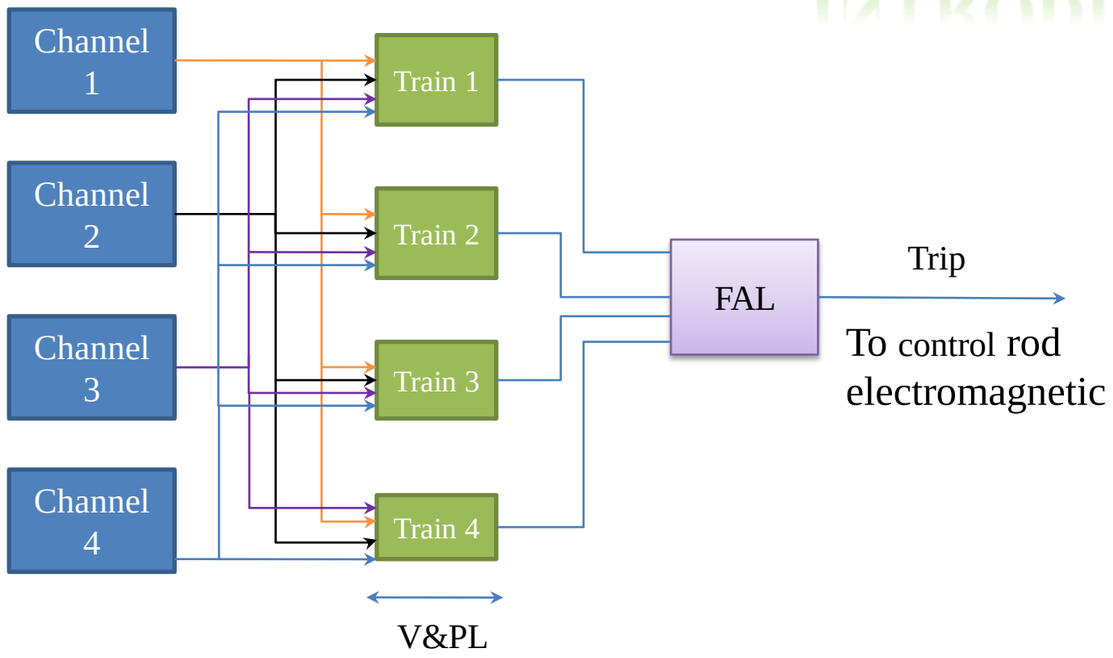

Figure 1 : Generic Architecture of RPS

Based on fig. 1, channel 1 up to channel 4 are the sensor or detector in the reactor power plant. Channel are the field signal that connected to RPS. RPS was designed to safety shutdown the reactor when anything gone wrongs. While Train 1 to train 4 are the V&PL of RPS. In addition, the implementation of 2 out of 4 are used. Meanwhile 1 out of 2 was used on Nuclear Malaysia Triga Puspati reactor. In the other words, when any of twos inputs are high, the train 1 or 2 or 3 or 4 will enable and trigger FAL. Thus, no current was past thru electromagnetic which can cause control rod to fall down and trip the whole system. FAL is the final actuation logic. V&PL are more safety and reliable control method which was been implemented on nuclear power plant. The trip or also know as SCRAM action was happen when in case of anticipated operation occurrences, incident condition or design basic incident. The protective action of RPS trip signal are the insertion of all control rods. Basically RPS was tripped by auto, operator, or based on safety parameters which was said as reach the limit set point . It is also know as Safety System Setting (SSS).

RESULT AND DISCUSSION

Table 1: Truth table of V&PL

Input				Output	
A	B	C	D	OP	Decimal #
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	0	2
0	0	1	1	1	3
0	1	0	0	0	4
0	1	0	1	1	5
0	1	1	0	1	6
0	1	1	1	1	7
1	0	0	0	0	8
1	0	0	1	1	9
1	0	1	0	1	10
1	0	1	1	1	11
1	1	0	0	1	12
1	1	0	1	1	13
1	1	1	0	1	14
1	1	1	1	1	15

Table 2: K-Map for V&PL

$$V\&PL = AB + AD + AC + BC + CD + BD \quad (1)$$

Fig. 3 shown the CMOS of NOR and NAND gate. To design a OR gate and AND gate we need to cascaded inverter as on fig. 3 (iii) with CMOS NOR and NAND. While fig. 4 is the final simulation result. The 0V is equivalent as "0" and 5V as "1" in digital world. Meanwhile, equation (1) is the V&PL equation using AND gate and OR gate.

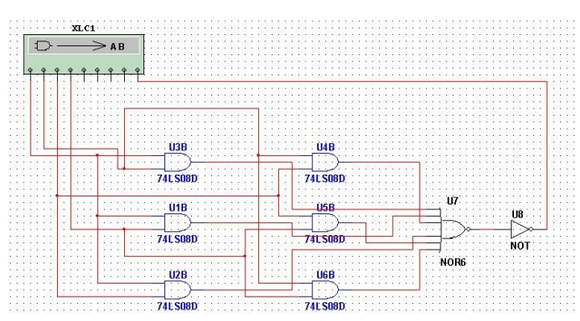

Figure 2: Schematic of V&PL

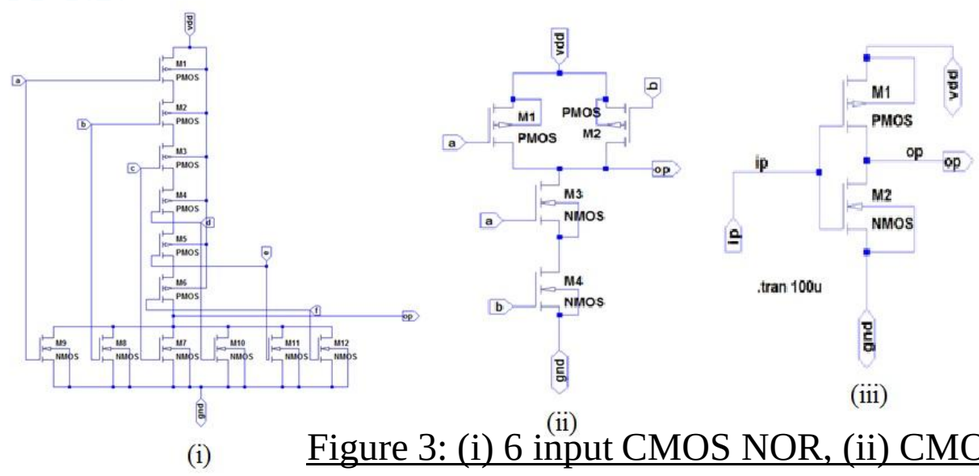

Figure 3: (i) 6 input CMOS NOR, (ii) CMOS NAND, (iii) CMOS Inverter

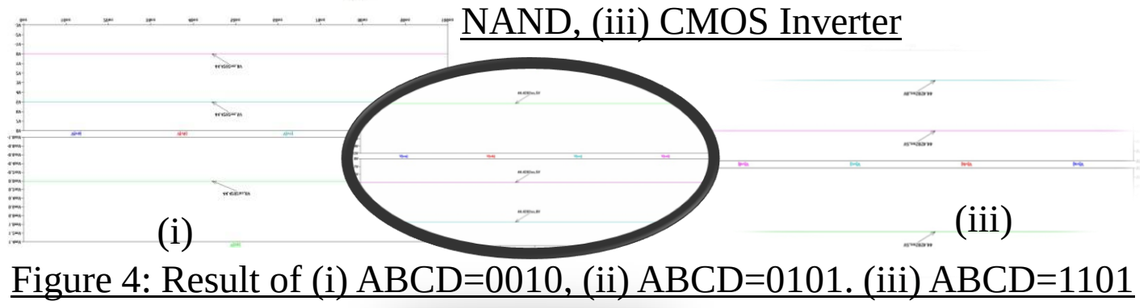

Figure 4: Result of (i) ABCD=0010, (ii) ABCD=0101. (iii) ABCD=1101

CONCLUSION

Finally, the objective had been meet. The design of V&PL sub modules which was applicable on Nuclear Power Plants. Moreover the production of truth table as on table 1 as do the K-Map as on table 2. Beside that, LTspice IV was used to design and simulate V&PL. The result show on fig. 4 can be compare thru table 1. However for the future work, the comparison of difference sort of gated can be design and compare.