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MODULAR CONTROL OF FUSION POWER HEATING APPLICATIONS

Phase 1
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Close-out Report
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1 Executive Summary

This work is motivated by the growing demand for auxiliary heating on small and large machines worldwide. Numerous present and planned RF experiments (EBW, Lower Hybrid, ICRF, and ECH) are increasingly complex systems. The operational challenges are indicative of a need for components of real-time control that can be implemented with a moderate amount of effort in a time- and cost-effective fashion. Such a system will improve experimental efficiency, enhance experimental quality, and expedite technological advancements.

The modular architecture of this control-suite serves multiple purposes. It facilitates construction on various scales from single to multiple controller systems. It enables expandability of control from basic to complex via the addition of modules with varying functionalities. It simplifies the control implementation process by reducing layers of software and electronic development. While conceived with fusion applications in mind, this suite has the potential to serve a broad range of scientific and industrial applications.

During the Phase-I research effort we established the overall feasibility of this modular control-suite concept. We developed the fundamental modules needed to implement open-loop active-control and demonstrated their use on a microwave power deposition experiment.

1.1 Phase-I Report

During Phase-I we achieved the five goals laid out for the project: (1) system-level study of microcontroller and interfacing electronic specifications, (2) microcontroller evaluation and selection, (3) open-loop control-software development, (4) interfacing control-electronics prototyping, and (5) system assembly and validation of an open-loop control system on the MST-EBW antenna. A detailed description of each effort is given in the following sections. Realization of these goals, (identification of the Phase-II system specifications,) and analysis of anticipated closed-loop system performance demonstrate feasibility of this closed-loop modular control concept.

1.1.1 System-Level Study

Our intent is to develop a control-suite that will meet the needs of the MST-EBW system, yet is flexible enough to serve the needs of other fusion applications. A system level survey was performed to identify the MST-EBW active open and closed-loop control requirements. These were complemented with those from broader sets of fusion related control applications; Table 1 synopsizes the results. From this survey we distilled a set of minimum system requirements shown in the last line of the grid. This information was considered in conjunction with microcontroller and interfacing electronics criteria to generate sets of characteristics that would suit the project goals. The microcontroller criteria and selection are discussed in the next section.

OPEN AND CLOSED LOOP										
	Driven/Ouput Signals							Sensed/Monitored Signals		
		Waveform			DAC			ADC		
Example	# Channels	Frequency	Waveform	# Steps per Period	Resultant Ouput Freq.	Resolution (no coarser than)	Drive V	# Channels	Sampling Rate	Sensed V
Antenna	5	1-10 kHz	Various	20	20-200 kHz	20 mV/step	6-15 V	8	20-200 kHz	-15 to +10 V
	2		DC		20 kHz		0-5 V			
Other	8	1-10 kHz	Various	10-20	10-200 kHz	20 mV/step	+/- 15 V	8	10-200 kHz	+/- 15 V
	8		DC		20 kHz		+/- 10 V			
Desired Minimum Specs.	8	1-10 kHz	DC, Various	20	10-200 kHz	20 mV/step	+/- 15 V	8	10-200 kHz	+/- 15 V

Table 1 Open and closed-loop system survey summary.

1.1.2 Microcontroller Evaluation and Selection

Care was taken during the microcontroller evaluation and selection phase to identify a unit suitable for both the Phase-I and II efforts. The characteristics identified from the survey suggest the DACs should have a minimum of 8-bit resolution (but 12-bit would be preferred) and a minimum output clocking of 100 kHz. Likewise, the required ADC resolution is 8-bit minimum with a desired input of 500ksps. The DACs, ADCs, and voltage reference should be on-chip to reduce the component count. Other conditions we imposed were: the chip architecture must be well supported and tested; the board must be economical and easy to use; and a user friendly development interface must exist. We found the following:

- Economical features
    - Development kits
        - available from most manufactures
        - costs range from less than $100 to several hundred
    - Compilers
        - Commercial full versions cost from $800-$3000 per copy
        - Demo versions have time/capability limits or licensing restrictions.
        - Open source compilers allows for future customer modifications at minimal costs; SDCC supports various architectures.
- Programming Environment
    - All the major microcontroller manufactures have programming environments and support.

Many suppliers were considered, but Silicon Laboratories (SiLabs), Microchip, Analog Devices, and Freescale stood out from the rest. Some general findings using the requirements and considerations listed above are:

- There are no more than 2 DAC channels on any of the 8-bit chips
- Many architectures are available (Microchip and SiLabs have 8051 chips)
- High resolution (16-32 bit) chips with digital signal processing or 2+ channels DAC exist, but they are more complex to operate and more costly.

A parametric template of microprocessor characteristics, such as the one shown in Table 2, guided our selection process. The SiLabs C8051F120, Microchip DSPic33FJxxGP802 and DSPic33FJxxGP804, and Analog Devices ARM7 were among our top choices. We chose the C8051F120 which provided the best balance of functionality with cost. Its specifications are highlighted with yellow in Table 2, its attributes include:

- The 8051 is a commonly used and well supported architecture
- There are on-chip DACs and ADCs, and onboard Vref
- An inexpensive development kit and integrated development environment exist
- An open source compiler is available
- Hardware serial ports include – UART, SPI, and SMB

Parametric Illustration of Microcontroller Specifications - Silicon Laboratories C8051F120 characteristics highlighted in yellow												
MIPS (peak)	100M	50	48	25	20							
Flash (kB)	128	64	32	16	8	4	2					
RAM (bytes)	8448	5376	3452	3328	2304	1536	1280	256				
Dig I/O	64	59	40	39	32	29	27	25	24			
Package (pin)	100	64	48	32	28	24	20	16x16 TQFP Main Chip				
Comparators	3	2	1									
Timers 16-bit)	5	4	3	2								
PWM Channels	6	5	3									
Internal Osc.	±20%	±2%	±1.5%	±0.5%								
ADC-1	24	16	12	10	8			12 bits at 100k samples/s				
ADC-2	24	16	12	10	8			8 bits at 500k samples/s				
DAC-1			12	10	8							
DAC-2			12	10	8							
Comparators	3	2	1									
VREF	yes	no										
Temp Sensor	yes	no										
Ext Mem I/F	yes	no										
Serial Buses	USB	UART	LIN	CAN	I2C	SPI	EMIF	2 available				
Other Analog	PGA	MAC	martcloc	LFO	DMA	VREG		available on the development board				

Table 2 - Parametric illustration of typical microcontroller specifications. The C8051F120 characteristics are highlighted in yellow.

1.1.3 Control-Software Development

The development of software to demonstrate open-loop control using the C8051F120 was a large portion of the Phase-I effort. In the following paragraphs we describe the method used for software development and implementation, the environment in which the software is developed, the software characteristics, the benefits realized by using the open source C compiler, and an overview of the software modules developed.

The software developed in this modular control application is executed on one or more microprocessors dedicated to the control application. Each microprocessor (chip) is located on a development board. The development board, purchased as shown in Figure 5 from SiLabs, also contains a serial port for communication with a PC, eight 8-pin digital I/O ports, a screw terminal interface, and a ribbon connector.

The development board interfaces with a PC via two USB ports – one of which transitions to a serial port on the development board. The control software developed in this application is downloaded to the microprocessor on the development board from a PC via the serial connection. The software is then resident and executed on the microprocessor for the open and closed-loop control applications. User keyboard input to the executing code is achieved via a universal asynchronous receiver transmitter (UART) on the development board and a hyper-terminal window on the PC. The SI software development interface maintains contact with the code execution on the microprocessor.

The microcontroller core of the C8051F120 contains a pipeline architecture that greatly increases its instruction throughput over the standard 8051 architecture. While it uses the standard MCS-51™ instruction it is capable of operating at speeds of up to 100 mega instructions per second (MIPS). It executes 70% of its instruction set in 1 or 2 system clock cycles and only four instructions take over four system clock cycles.

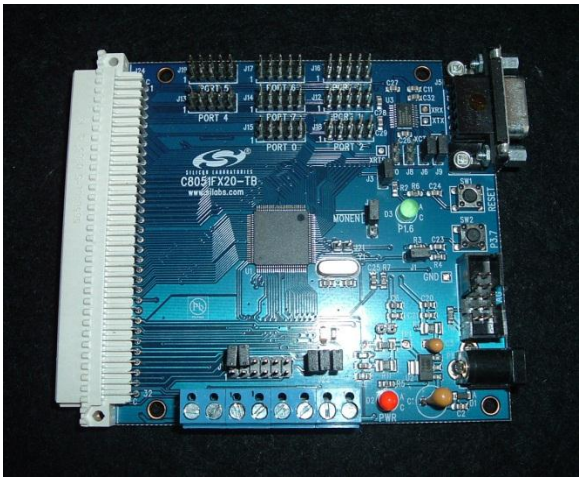

Fig. 5 The SiLabs C8051F120 micro-controller development board.

The SI-C8051F120 development board is available with a front end PC user interface that makes it simple to compile, link, and download code to the processor. All code is developed in standard C, uploaded into the SI user interface, and compiled, linked, and download to the microprocessor. The use of standard C, and the software modules (functions) developed in Phase-I, makes the process straightforward.

Since the C8051F120 uses the MCS-51™ instruction set it is compatible with standard 8051 assemblers and compilers. Thus, we have chosen to use the open source C compiler (SDCC) which frees the user from constraints sometimes imposed by manufacturer specific compilers. Its many attributes include: it is open source (free to users), updates are readily obtainable, online discussion and trouble-shooting resources are available, it is microprocessor manufacturer independent, it is an accepted standard. The

utility of this compiler is so recognized, that it is supported within the SiLabs IDE environment making its use straightforward.

The control and monitor signals of the open and closed-loop systems are available at various locations on the development board. Each of the 100 pins of the microprocessor chip is mapped to a pin of the ribbon connector making signal access and delivery simple. In addition, the ADC, DAC, ground, and Vref signals are also present at the screw terminal strip. The majority of port pins are mappable by the control software (developer).

The backbone of this modular system is the use of building blocks – a feature which will make it adaptable to a variety of applications (not just the MST EBW system). Thus, the majority of the code we have developed is in the form of functions. There are three basic categories – initialization (microprocessor control, peripheral control, header files), signals and processing (waveforms, data processing), and application specific (main, user interface). Those used for the open-loop MST-EBW control application include:

Initialization:

- Init_SYS: Initialize the C8051 (including the watchdog timer and global interrupts).
- Init_SYSCLK: System clock initialization (to use the external crystal oscillator, allowing it time to start and settle).
- Init_UART0: UART0 initialization (for serial communication with the PC).
- Init_PORT: PORT I/O initialization (via the port I/O Crossbar registers and an Output Mode register).
- Init_Timer4: Timer4 initialization (to auto-reload mode and to generate interrupts at specified time intervals to regulate the update rate of the DAC).
- ISR_Timer4: Waveform Output (interrupt service routine that is called when Timer4 overflows).
- Init_DAC0: Initialize the DAC (to a default voltage; set its voltage reference; set output update to occur on Timer4 overflow; set the gain of the voltage).
- Init_DAC1: Similar as Init_DAC0.
- ISR_ExternalInt1: Recognize an external trigger (and start waveform output).
- C8051F120.h: Special function register declarations (standard from SDCC)

Signals and Processing:

- Init_Waveforms: Initialize the voltage waveforms (with arrays stored in xdata.)
- Wform_Spec: Waveform specifications (including the update rate of the DAC in Hz and the number of points in one cycle of the waveform).

Application Specific:

- main(void);
- User_Query: Query the user for information.
- SignalControl.h: Signal control declarations (gathered for ease of use and modularity).

1.1.4 Interfacing Control Electronics

The second set of modular components is interfacing electronics; the bridge between the development board and hardware (or experimental apparatus). During Phase-I we prototyped an eight channel bipolar

amplifier to interface the DAC voltage signal (±2.4V) with the EBW antenna system. Each channel is capable of operating relative to an input reference voltage or a common ground signal and can be gain adjusted from 1 to 6. Figure 6 is a photo of the unit (with the cover removed) which contains two power supplies and eight individual op-amp circuits. This design exceeds the needs of the EBW open-loop application, but is general enough to be used during Phase-II and on a variety of control applications.

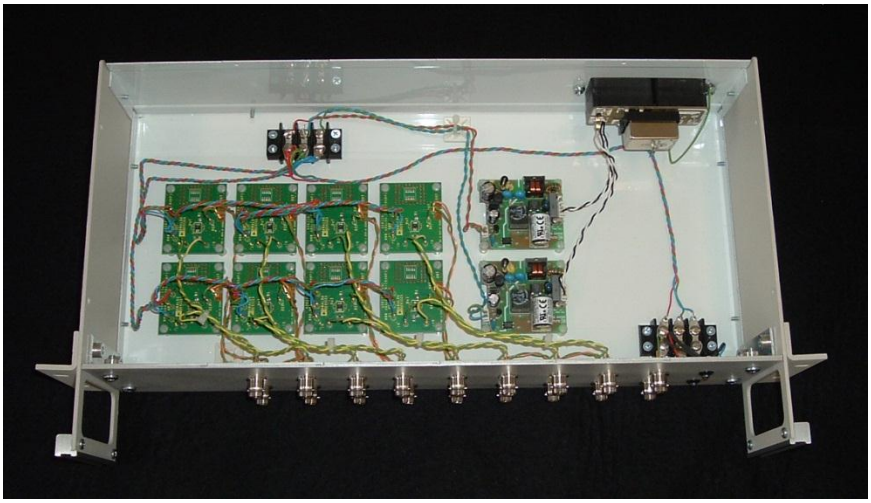

Fig. 6 Interfacing electronic module: 8–channel amplifier, ±15V output.

The electronics design is mindful of reliability, performance, and cost. Individual components (rather than multi-channel or interdependent units) were used to ensure modularity. A power entry module containing an RFI power line filter controls line-to-ground noise; high efficiency, compact form factor, medical grade power supplies provide regulated DC outputs; and amplifiers with a maximum gain of 1k are differential.

1.1.5 System Assembly and Validation

The microprocessor, software components, and interfacing electronics developed within this Phase-I effort have been integrated to produce an open-loop control system and used to drive the phase and amplitude inputs of the EBW antenna on MST. This is shown in the three panels of Figure 7; the upper left photo shows the laptop connected to the C8051F120; the outputs of the DACs are connected to the amplifier. The lower left panel is a photo of the full setup, and the lower right photo shows the synthesized signal generators tuned to 3.6 GHz. Waveforms produced by the C8051F120 and used to drive the RF circuitry were digitized by the MDS+ data system; use of this microprocessor for open and closed-loop control does not preclude digitization of the control or monitor signals by the laboratory's data system. This application was a successful demonstration of modular open-loop control.

Fig. 7 Open-loop modular suite controlling MST EBW system phase and attenuation. (upper) A laptop is connected to the C8051F120; the outputs of the two DACs are connected to the amplifier built during Phase-I. (lower left) A wider perspective showing the system with the full complement of EBW electronics. (lower right) The (EBW) synthesized signal generators tuned to 3.6 GHz.

The phase between wavefronts in the two arms of the antenna is a critical parameter in coupling RF power to the plasma. The optimum value for a particular set of edge plasma conditions is found by continuously scanning the phase and monitoring the reflected signal. The control voltage - Figure 8a - is the output of the DAC, which is amplified and sent to an electronic phase shifter. The signal is ramped in time to cover a full 360 degrees in 10 milliseconds. Figure 8b is the measured phase between the two arms. This demonstrates successful control over the full range of phase.

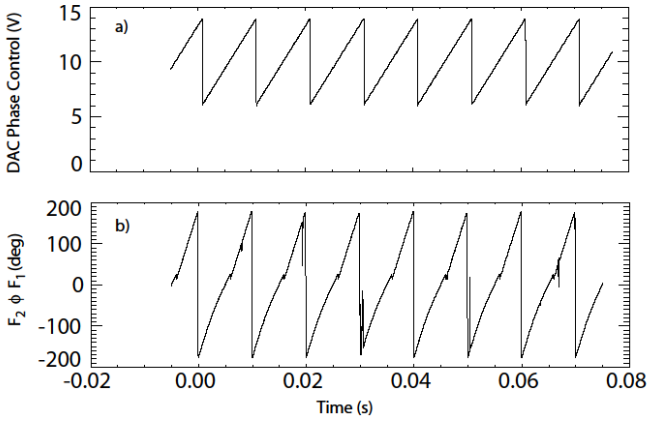

Fig. 8 (a) Voltage waveform produced by the micro-controller, amplified via the modular electronics, and input to the phase shifter. (b) The resultant measured phase shift illustrates a full 360 degree phase scan each 10 ms.

The control of the amplitude of the RF signal is demonstrated in Figure 9. Here a simple power scan is performed by applying a sawtooth waveform (generated by the microcontroller and shown in Figure 9a) to a variable attenuator. Figure 9b is the measured power in dBm. It is worth noting that the linear waveform applied to the attenuator leads to a logarithmic decrease in power. Phase-II applications will utilize fast feedback of the measured power to control several of these variable attenuators; the logarithmic change of power is easily incorporated into the logic.

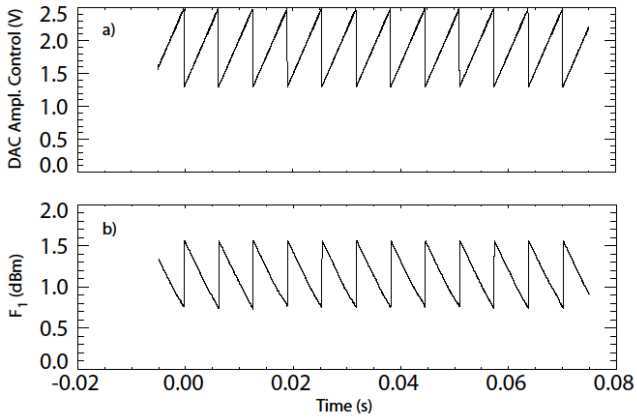

Fig. 9 (a) Voltage waveform produced by the micro-controller and input to the variable attenuator. (b) The measured power in dBm.

1.2 Brief Summary

The success of the Phase-I development demonstrated the feasibility of progressing with Phase-II. The open-loop control modules (software and interfacing electronics) prove flexible enough to drive considerably different hardware devices (e.g. the 2-30 V phase shifter and the 0-5 V variable attenuator). The usefulness of, and scientific benefits realized with the control-suite will be significantly increased by the development of closed-loop control. The specifications needed for closed-loop control of several possible applications (the logical next step that would have been achieved by advancing to a Phase-II) have been identified and are compatible with the attributes (speed, memory, and I/O) of the microprocessor.