PREPARATION AND CHARACTERIZATION OF THIN ZrO_2 LAYERS FOR GATE INSULATION IN MOSFET

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1. Introduction

Present rapid downscaling of metal-oxide-semiconductor (MOS) devices gives rise to a number of issues. The most important is the high gate leakage current [1], which is due to an exponential increase of direct tunneling through the gate dielectric for oxide thickness below ~1.3 nm. Gate leakage reduction in ultrathin gate dielectrics is the main motivation for the searching of high permittivity ("high-κ") materials such as ZrO_2, TiO_2, Al_2O_3 and HfO_2 in order to replace conventional SiO_2 [2]. The quality of the high-*k* oxides is strongly dependent on the manufacturing process. Therefore the deposition techniques are continuously modified and optimized.

The issues of the insulator-to-semiconductor interface have recently received lots of attention, particularly in conjunction with introducing alternative materials of the new generation of high-*k* MOS structures [3]. There are quite a few methods allowing to determine the trap density D_{it} at the insulator-to-semiconductor interface. Nicollian and Goetzberger designed a conductance method [4] that is considered to be the most precise and sensitive. The method is based on measuring the equivalent parallel conductance G_p of the MOS structure in dependence on the applied voltage and frequency.

In this paper, we present the results of our study on the electrical properties of ZrO_2 dielectric material prepared by MOCVD (Metal Organic Chemical Vapor Deposition). We also determined value of interface trap density.

2. Experiment

As substrates, we have used a p-type (100) oriented homogeneous silicon. Before the deposition of dielectric, the native oxide was removed by cleaning Si substrate in HF solution (ratio 1:40) for 5 minutes. The ZrO_2 dielectric was deposited by MOCVD method at deposition temperature and pressure 600 °C and 1.5 Torr, respectively. The thicknesses of the ZrO_2 dielectric layers measured by XRR (X-ray Reflectivity) are shown in Tab. 1. The gate electrodes were prepared by evaporating Au/Ni bilayer and patterned photolitographically by lift-off technology. The ohmic contact was created by sputtering a thin layer of Al on the back side. Finally, samples were annealed in forming gas (FGA, $90\%N_2+10\%H_2$), N_2 or O_2 ambient atmosphere (Tab. 2).

Tab. 1. *Overview of thickness for different samples.*

Annealing	FGA, 380 °C, 30 min.						
Sample	Zr3d	Zr4d	Zr5d	Zr6d	Zr7d	Zr8d	Zr18
t_{ox} (nm)	20	25	9.6	13	8.81	6.36	10

Tab. 2. *Overview of annealing treatment conditions for various samples.*

Sample	Zr18a	Zr18c	Zr18d	Zr18e	Zr18f
Annealing	–	FGA, 500 °C, 30 min.	FGA, 700 °C, 30 min.	N_2, 500 °C, 60 min.	O_2, 500 °C, 60 min.

3. Results and discussion

Typical sets of *C-V* curves of Au-Ni/ZrO_2/Si(p) MOS structures with different thicknesses of dielectric layers are shown in Fig. 1(a). The *C-V* curves prove good capacitance properties of the MOS structures. One observes a small dispersion of the values of V_{FB}, which confirms a uniform distribution of the defect charge. Plots of EOT in dependence on the thickness, EOT=$f(t_{ox})$, are shown in Fig. 1(b) along with least square linear fit [5]. From the plot EOT vs. t_{ox} we were able to determine a value of dielectric constant. Also the thin interfacial layer of SiO_2 at ZrO_2/Si(p) interface was detected [6]. The value of dielectric constant and thickness of SiO_2 interfacial layer is ~16 and ~1.7 nm, respectively. The presence of such a SiO_2 layer at ZrO_2/Si interfaces had been confirmed by secondary ion mass spectrometry (SIMS).

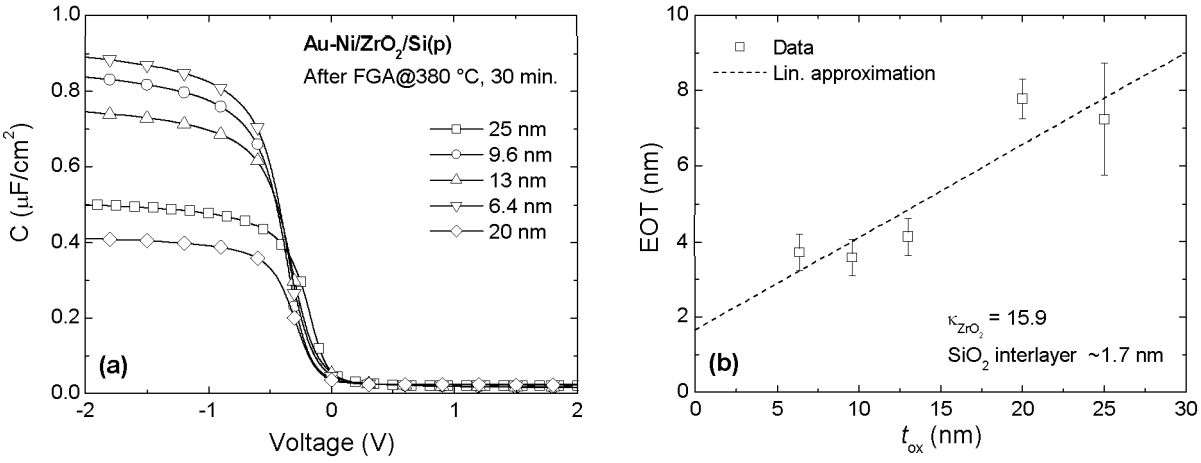

Fig. 1: *(a) Typical sets of C-V curves (1 MHz) of Au-Ni/ZrO_2/Si(p) MOS structures. (b) Extraction of dielectric constant from EOT vs. t_{ox} plot.*

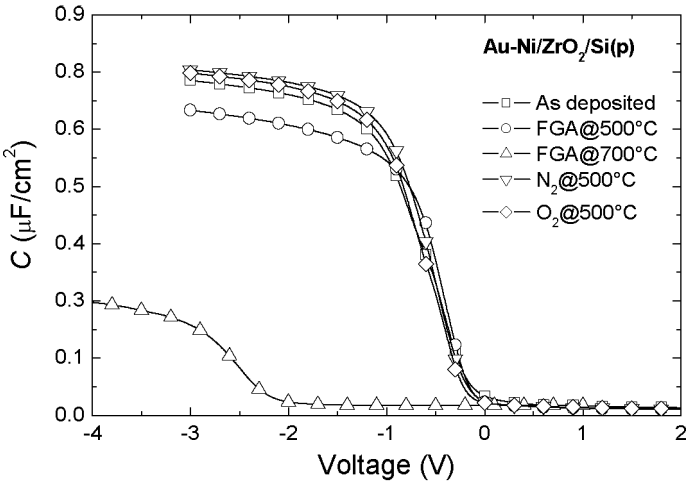

Fig. 2: *Typical sets of C-V curves (1 MHz) of Au-Ni/ZrO_2/Si(p) MOS structures before and after FGA, N_2 and O_2 annealing.*

Typical sets of *C-V* curves of Au-Ni/ZrO_2/Si(p) MOS structures before and after FGA, N_2 and O_2 annealing are shown in Fig. 2. The sample before and after FGA at 700 °C annealing was chosen for comparison of interface trap density [4]. The effect of FGA upon the trap density for sample before and after FGA is shown in Fig. 3(a). After FGA, D_{it} increase by as much as half orders of magnitude, exhibiting a pronounced maximum at the energy E_f–$E_i \cong 0.2$ eV. The effect of FGA annealing is observable on the measured dependence of the equivalent conductance G_p/ω for selected energy levels E_f–E_i (Fig. 3(b).). In that case one can see a increasing of conductance and marked maximum on the curves.

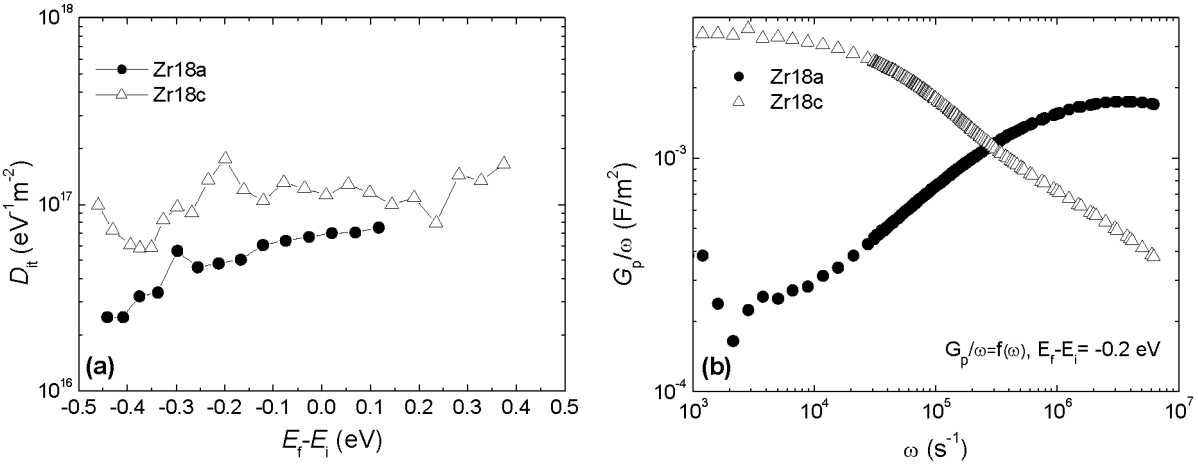

Fig. 3: (a) *Comparison of the Au-Ni/ZrO_2/Si(p) interface trap density D_{it} for samples before and after FGA and (b) comparison of G_p/ω versus ω curves of the Au-Ni/ ZrO_2/Si(p) structure at energy levels E_f–E_i=-0.2 eV.*

4. Conclusion

The value of dielectric constant for ZrO_2 dielectrics layer prepared by MOCVD is ~16. From EOT vs. t_{ox} plot, the SiO_2 interfacial layer was detected at the ZrO_2/Si(p) interface. The presence of such a SiO_2 layer had been confirmed by SIMS.

The value of interface trap density for sample Zr18c is slightly higher as for sample Zr18a (Fig. 3(a)). Therefore, the FGA annealing at 700 °C is improper operation for post treatment of Au-Ni/ZrO_2/Si(p) structures.

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