0.5-V Input Digital LDO with 98.7% Current Efficiency and 2.7-µA Quiescent Current in 65nm CMOS

Yasuyuki Okuma[1], Koichi Ishida[2], Yoshikatsu Ryu[1], Xin Zhang[2], Po-Hung Chen[2], Kazunori Watanabe[1], Makoto Takamiya[2], and Takayasu Sakurai[2]

[1]Semiconductor Technology Academic Research Center (STARC), 3-17-2 Shin Yokohama, Kohoku-ku, Yokohama 222-0033, Japan

[2]The University of Tokyo, 4-6-1 Komaba, Meguro-ku, Tokyo 153-8505, Japan

***Abstract*- Digital LDO is proposed to provide the low noise and tunable power supply voltage to the 0.5-V near-threshold logic circuits. Because the conventional LDO feedback-controlled by the operational amplifier fail to operate at 0.5V, the digital LDO eliminates all analog circuits and is controlled by digital circuits, which enables the 0.5-V operation. The developed digital LDO in 65nm CMOS achieved the 0.5-V input voltage and 0.45-V output voltage with 98.7% current efficiency and 2.7-µA quiescent current at 200-µA load current. Both the input voltage and the quiescent current are the lowest values in the published LDO's, which indicates the good energy efficiency of the digital LDO at 0.5-V operation.**

I. INTRODUCTION

Very low-voltage operation of VLSI's is effective in reducing both dynamic and leakage power and the maximum energy efficiency is achieved at low power supply voltage (V_{DD}) below 0.5V (e.g., 340 mV [1] and 320 mV [2]). Thus, many works have been carried out on the sub/near-threshold logic circuits [1-5]. Stable and tunable V_{DD} (e.g., 320 mV$\pm$ 50mV [2]) is required in the near-threshold logic circuits, because the gate delay in the near-threshold logic circuits is very sensitive to V_{DD} and the process variations. Therefore, a 0.5-V LDO enabling the low ripple and tunable V_{DD} is strongly required. The conventional analog LDO, however, fails to operate at 0.5V. In order to solve the problem, the digital LDO enabling the 0.5-V operation is proposed and demonstrated in this paper. The concept and the circuit implementation of the proposed digital LDO is shown in Section II. Measurement results from 65-nm CMOS test chips are described in Section III.

II. PROPOSED DIGITAL LDO

In order to explain the concept of the proposed digital LDO, Fig. 1 shows the circuit schematic of the digital LDO in contrast with the conventional analog LDO. The conventional analog LDO shown in Fig. 1(a) consists of an operational amplifier and a power transistor. The conventional LDO fails to operate at 0.5V, because the operational amplifier does not operate at 0.5V and can not control the analog gate voltage of the power transistor. In order to solve the problem, the digital LDO shown in Fig. 1(b) is proposed. The digital LDO includes a switch array, a comparator, and a digital controller. The analog controlled power transistor is replaced with the switch array and the number of turned-on switches is changed digitally by the controller. The output voltage (V_{OUT}) is monitored by the comparator instead of the operational amplifier. Thus, the digital LDO eliminates all analog circuits and is controlled by digital circuits, which enables the 0.5-V LDO operation, because the digital circuits including the comparator can operate at 0.5V.

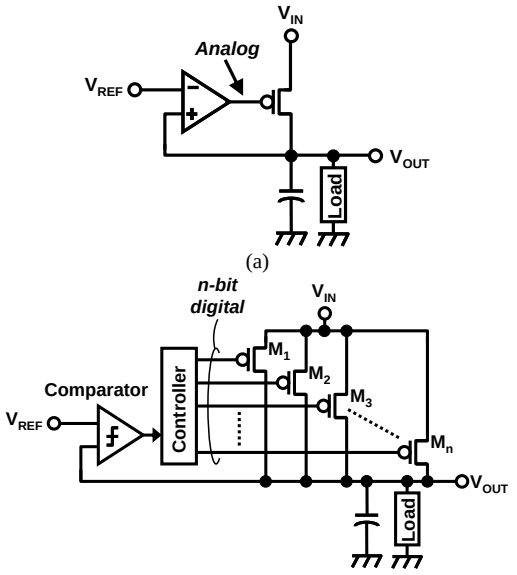

Fig. 1. (a) Conventional analog LDO. (b) Proposed digital LDO.

Fig. 2 shows is the circuit schematic of the fabricated digital LDO. The digital LDO consists of a comparator, a serial-in parallel-out bi-directional shift register, and switch array of 256 pMOS FET's. In order to reduce the ripple due to the switching of the switches, in this implementation, the shift register is used as the controller, because the number of switching in the switch array is only one at each clock edge. The typical input voltage (V_{IN}) and V_{OUT} are 0.5V and 0.45V, respectively. The typical clock frequency of the comparator and the shift register is 1MHz. The off-chip decoupling

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capacitor is 100nF and the typical load current (I_{LOAD}) is 200µA.

Fig. 3 shows the circuit schematic of the clocked comparator used in the digital LDO. In the design of LDO with I_{LOAD} of 200µA, low quiescent current is very important, because the large quiescent current degrades the current efficiency of LDO. In order to reduce the quiescent current, the clocked comparator is used in the digital LDO, because the clocked comparator can operate at 0.5V and consumes no DC-power.

Fig. 4(a) shows the operation of the bi-directional shift register. At first, all 256 bits are set to "1" in order to turn off all pMOS switches. After that, when the comparator output (Compout) is low, which means V_{OUT} is lower than the reference voltage (V_{REF}), all 256 bits are shifted toward right in order to increase the number of turned-on switches. In contrast, when Compout is high, which means V_{OUT} is higher than V_{REF}, all 256 bits are shifted toward left in order to decrease the number of turned-on switches.

Fig. 4(b) shows the circuit implementation of the serial-in parallel-out bi-directional shift register. The bi-directional shift register consists of selectors and D-FF's. The shift-right or the shift-left operation of the bi-directional shift register is determined by Compout. When Compout is low, each Q_K except Q_1 moves to Q_{K+1}, and Q_1 is set to "0", which achieves the shift-right operation. In contrast, when Compout is high, each Q_K except Q_{256} moves to Q_{K-1}, and Q_{256} is set to "1", which achieves the shift-left operation.

Fig. 5 shows the schematic of the transient of the number of turned-on switches in order to explain the feedback control of the digital LDO. The digital LDO controls the number of turned-on switches at each clock edge depending on Compout. When V_{OUT} equals to V_{REF}, the number of turned-on switches changes up and down by 1-bit, which determines the ripple of the digital LDO.

III. Measurement Results and Discussion

To demonstrate the advantage of the proposed digital LDO, a test chip is fabricated in 65nm CMOS. Fig. 6 shows the chip microphotograph and the layout. The total chip area including pads is $0.9\times0.8mm^2$ and the active area of the digital LDO is $0.042mm^2$.

Fig. 7(a) shows measured $V_{OUT} - V_{IN}$ characteristics at I_{LOAD} of 200µA. V_{REF} is varied from 0.35V to 0.55V by 0.05-V step. The digital LDO successfully regulates V_{OUT} from 0.35 to 0.45V at V_{IN} of 0.5V. At the design target of V_{IN} of 0.5V and V_{OUT} of 0.45V, the dropout voltage is 50mV and the measured line regulation is 3.1mV/V. Fig. 7(b) shows measured $V_{OUT} - V_{IN}$ characteristics at V_{REF} of 0.45V. I_{LOAD} is varied from 20µA to 200µA. The LDO achieves a successful load regulation of 0.65mV/mA with V_{IN} from 0.5V to 1.2V.

Fig. 8 shows the measured I_{LOAD} dependence of the current efficiency and the quiescent currents at 1-MHz and 10-MHz clock. Thanks to the digital LDO architecture, the measured quiescent current does not depend on I_{LOAD}, though the quiescent current increases with I_{LOAD} in the conventional analog LDO. At 1-MHz clock, the measured quiescent current

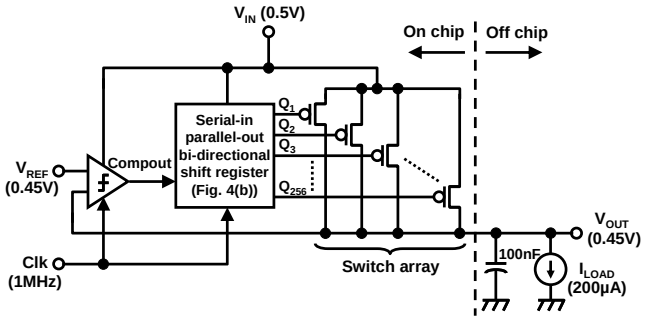

Fig. 2. Circuit schematic of the fabricated digital LDO.

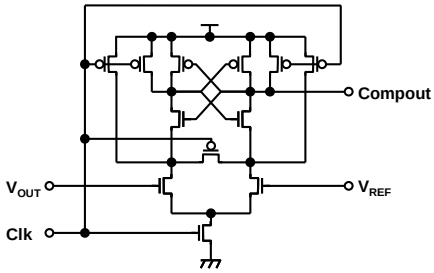

Fig. 3. Circuit schematic of clocked comparator used in digital LDO.

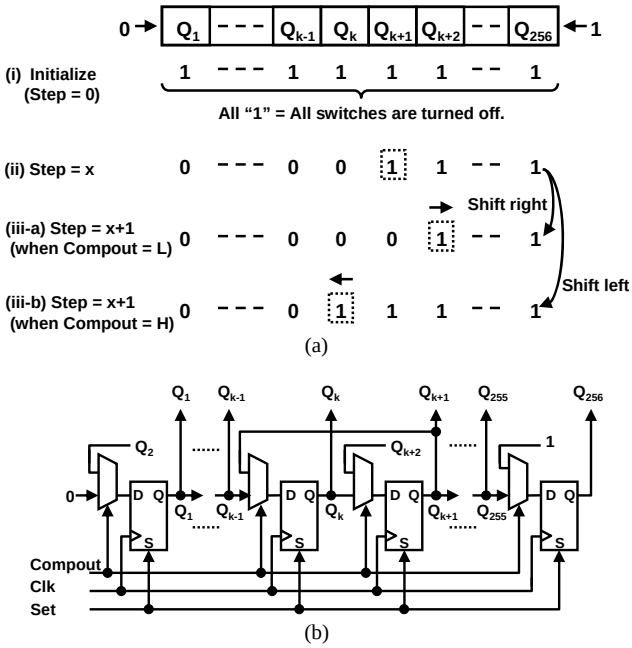

Fig. 4. (a) Operation of bi-directional shift register. (b) Circuit implementation of serial-in parallel-out bi-directional shift register.

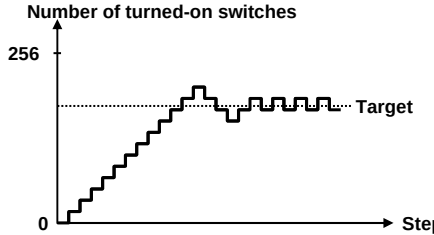

Fig. 5. Schematic of the transient of the number of turned-on switches in order to explain feedback control of digital LDO.

is 2.7µA, which is the smallest quiescent current in LDO's to the author's knowledge. The current efficiency is 98.7% at I_{LOAD} of 200µA.

Fig. 9 shows the measured transient waveform of V_{OUT} when V_{REF} changes from 0V to 0.45V at 1-MHz and 10-MHz clock and I_{LOAD} of 200µA. The settling time of V_{OUT} at 1-MHz clock is 590µs. By increasing the clock frequency from 1MHz to 10-MHz, the settling time can be reduced by 60% from 590µs to 240µs at the cost of increasing quiescent current from 2.7µA to 15µA and the corresponding degradation of the current efficiency by 5% at I_{LOAD} of 200µA as shown in Fig. 8. The tunable performance by changing the clock frequency is the advantage of the digital LDO.

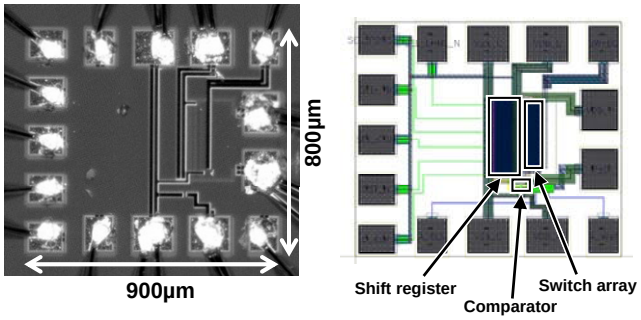

Fig. 6. Chip microphotograph and layout.

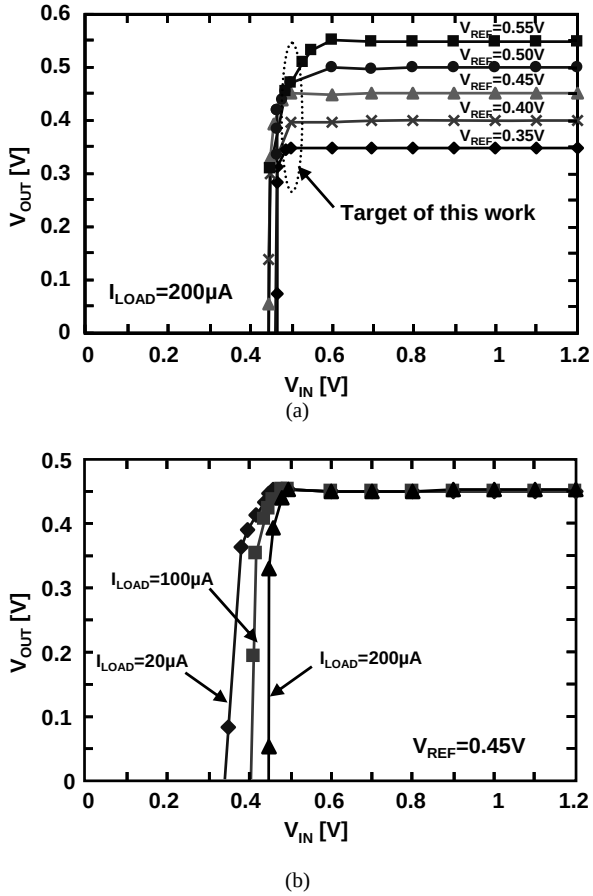

Fig. 7. Measured $V_{OUT} - V_{IN}$ characteristics. (a) V_{REF} is varied from 0.35V to 0.55V at I_{LOAD} of 200µA. (b) I_{LOAD} is varied from 10µA to 200µA at V_{REF} of 0.45V.

Fig. 10 shows the measured transient waveform of V_{OUT} when V_{REF} changes between 0.4V to 0.45V at 100Hz. The clock frequency is 1MHz and I_{LOAD} is 200µA. Fig. 11 shows the measured transient waveform of V_{OUT} when I_{LOAD} changes between 0A to 200µA at 100Hz. V_{OUT} is 0.45V and the clock frequency is 1MHz. The measured undershoot and overshoot of V_{OUT} are 40mV and 30mV, respectively. As shown in Figs. 10 and 11, these results show reasonable performance of the digital LDO to be applied to the power supply for near-threshold logic circuit.

Since the switch array in the digital LDO is switched

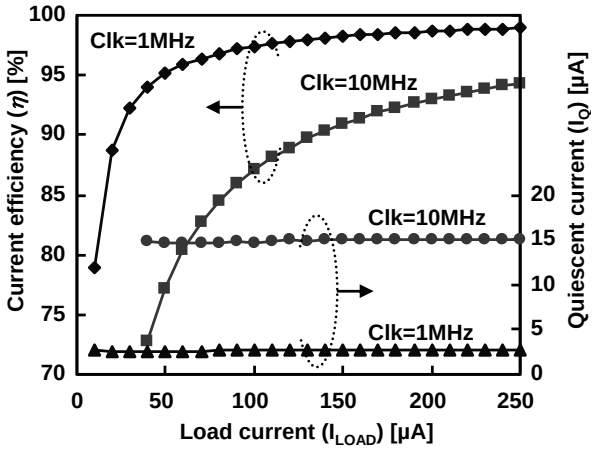

Fig. 8. Measured I_{LOAD} dependence of the current efficiency and the quiescent currents at 1-MHz and 10-MHz clock.

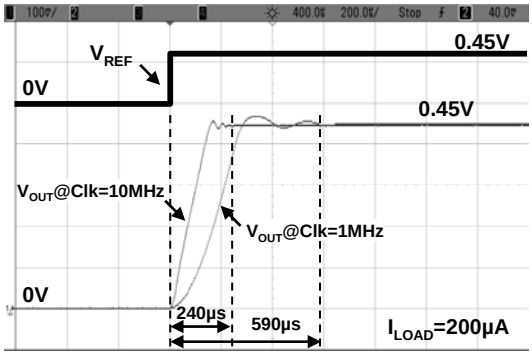

Fig. 9. Measured transient waveform of V_{OUT} when V_{REF} changes from 0V to 0.45V at 1-MHz and 10-MHz clock and I_{LOAD} of 200µA.

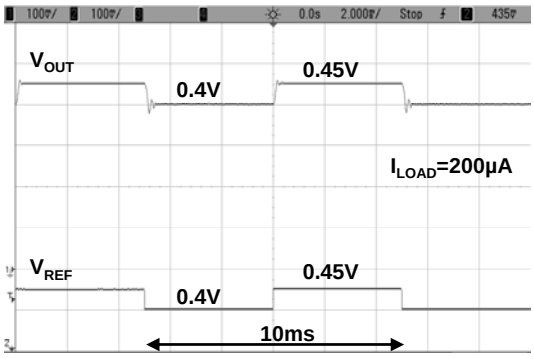

Fig. 10. Measured transient waveform of V_{OUT} when V_{REF} changes between 0.4V to 0.45V at 100Hz. The clock frequency is 1MHz and I_{LOAD} is 200µA.

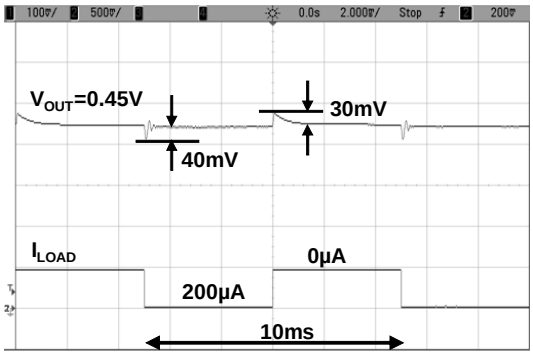

Fig. 11. Measured transient waveform of V_{OUT} when I_{LOAD} changes between 0A to 200µA at 100Hz. V_{OUT} is 0.45V and the clock frequency is 1MHz.

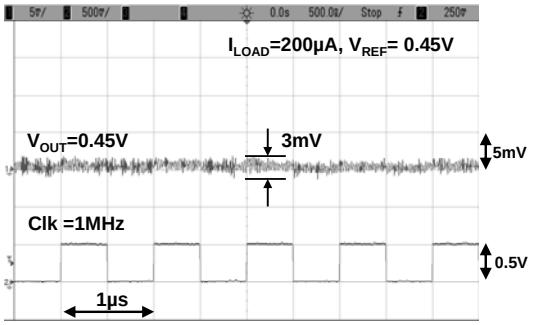

Fig. 12. Measured waveforms of V_{OUT} and 1-MHz clock. V_{OUT} is 0.45V and I_{LOAD} is 200µA.

digitally, the clock-related digital noise may cause LDO output ripple. To evaluate the ripple caused by the digital noise, output ripple is measured as shown in Fig. 12. V_{OUT} is 0.45V and the clock frequency is 1MHz. The ripple of V_{OUT} is less than 3mV. The measured V_{OUT} shows no significant ripple at clock edges and its harmonic tones, which indicates that the clock-related digital noise does not affect the LDO output ripple in the developed digital LDO.

The key performance summary of the proposed digital LDO and comparison with some previous regulators are listed in Table I. The digital control is proposed in [6]. The regulator in [6], however, is not LDO but a half V_{DD} generator. In this paper, both the digital LDO and 0.5-V LDO are demonstrated for the first time. The developed digital LDO achieved the 0.5-V input voltage and 0.45-V output voltage with 98.7% current efficiency and 2.7-µA quiescent current at 200-µA load current. Both the input voltage and the quiescent current are the lowest values in the published LDO's.

IV. Conclusion

In this paper, the digital LDO enabling the 0.5-V operation is proposed and demonstrated for the first time. The developed digital LDO in 65nm CMOS achieved the 0.5-V input voltage and 0.45-V output voltage with 98.7% current efficiency and 2.7-µA quiescent current at 200-µA load current. Both the input voltage and the quiescent current are the lowest values in the published LDO's, which indicates the good energy efficiency of the digital LDO at 0.5-V operation.

TABLE I
KEY PERFORMANCE SUMMARY OF THE PROPOSED DIGITAL LDO AND COMPARISON WITH PREVIOUS REGULATORS

	Unit	[6]	[7]	[8]	[9]	This work
Type of regulator	-	Half V_{DD} generator	LDO	LDO	LDO	LDO
Control	-	Digital	Analog	Analog	Analog	Digital
CMOS Technology	-	90nm	90nm	350nm	350nm	65nm
Active area	mm^2	0.03	0.008	0.264	0.053	0.042
Minimum input voltage	V	2.4	1.2	2	1.05	0.5
Nominal output voltage	V	1.2	0.9	1.8	0.9	0.45
Maximum load current	mA	1000	100	200	50	0.2
Line regulation	mV/V	-	-	2	1.1	3.1
Load regulation	mV/mA	-	1	0.17	0.06	0.65
Decoupling capacitor	µF	0.0024 (on-chip)	0.0006 (on-chip)	1 (off-chip)	1 (off-chip)	0.1 (off-chip)
Quiescent current	µA	25700	6000	20 to 320	4.02 to 164	2.7
Current efficiency	%	97.5	94.3	99.8	99.7	98.7

Acknowledgments

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